

IRF3709ZCSPbF
IRF3709ZCLPbF

Applications

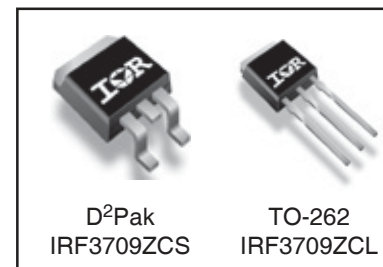
- High Frequency Synchronous Buck Converters for Computer Processor Power
- Lead-Free

HEXFET® Power MOSFET

| V_{DSS} | $R_{DS(on)}$ max | Qg |
|------------|--------------------------------|-------------|
| 30V | 6.3mΩ | 17nC |

Benefits

- Low $R_{DS(on)}$ at 4.5V V_{GS}
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|-----------------------------------|--|-----------------------|---------------------|
| V_{DS} | Drain-to-Source Voltage | 30 | V |
| V_{GS} | Gate-to-Source Voltage | ± 20 | |
| I_D @ $T_C = 25^\circ\text{C}$ | Continuous Drain Current, V_{GS} @ 10V | 87 [Ⓞ] | A |
| I_D @ $T_C = 100^\circ\text{C}$ | Continuous Drain Current, V_{GS} @ 10V | 62 [Ⓞ] | |
| I_{DM} | Pulsed Drain Current [Ⓛ] | 350 | |
| P_D @ $T_C = 25^\circ\text{C}$ | Maximum Power Dissipation | 79 | W |
| P_D @ $T_C = 100^\circ\text{C}$ | Maximum Power Dissipation | 40 | |
| | Linear Derating Factor | 0.53 | W/ $^\circ\text{C}$ |
| T_J | Operating Junction and | -55 to + 175 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|--|------|------|---------------------------|
| $R_{\theta JC}$ | Junction-to-Case [Ⓢ] | — | 1.89 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) [Ⓢ] | — | 40 | |

Notes [Ⓛ] through [Ⓢ] are on page 11

IRF3709ZCS/LPbF

International
IR Rectifier

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

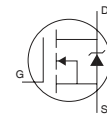
| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--------------------------------|--------------------------------------|------|-------|------|-------|--|
| BV_{DSS} | Drain-to-Source Breakdown Voltage | 30 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.021 | — | mV/°C | Reference to $25^\circ\text{C}, I_D = 1mA$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 5.0 | 6.3 | mΩ | $V_{GS} = 10V, I_D = 21A$ ③ |
| | | — | 6.2 | 7.8 | | $V_{GS} = 4.5V, I_D = 17A$ ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.35 | — | 2.25 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Coefficient | — | -5.5 | — | mV/°C | |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 1.0 | μA | $V_{DS} = 24V, V_{GS} = 0V$ |
| | | — | — | 150 | | $V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -20V$ |
| g_{fs} | Forward Transconductance | 88 | — | — | S | $V_{DS} = 15V, I_D = 17A$ |
| Q_g | Total Gate Charge | — | 17 | 26 | nC | $V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 17A$ See Fig. 14a&b |
| Q_{gs1} | Pre-Vth Gate-to-Source Charge | — | 4.4 | — | | |
| Q_{gs2} | Post-Vth Gate-to-Source Charge | — | 1.7 | — | | |
| Q_{gd} | Gate-to-Drain Charge | — | 6.0 | — | | |
| Q_{godr} | Gate Charge Overdrive | — | 4.9 | — | | |
| Q_{sw} | Switch Charge ($Q_{gs2} + Q_{gd}$) | — | 7.7 | — | | |
| Q_{oss} | Output Charge | — | 11 | — | nC | $V_{DS} = 16V, V_{GS} = 0V$ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 13 | — | ns | $V_{DD} = 15V, V_{GS} = 4.5V$ ③ $I_D = 17A$ Clamped Inductive Load |
| t_r | Rise Time | — | 41 | — | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 16 | — | | |
| t_f | Fall Time | — | 4.7 | — | | |
| C_{iss} | Input Capacitance | — | 2130 | — | pF | $V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0MHz$ |
| C_{oss} | Output Capacitance | — | 450 | — | | |
| C_{rss} | Reverse Transfer Capacitance | — | 220 | — | | |

Avalanche Characteristics

| | Parameter | Typ. | Max. | Units |
|----------|---------------------------------|------|------|-------|
| E_{AS} | Single Pulse Avalanche Energy ② | — | 60 | mJ |
| I_{AR} | Avalanche Current ① | — | 17 | A |
| E_{AR} | Repetitive Avalanche Energy ① | — | 7.9 | mJ |

Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|------|------|------|-------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 87 ⑥ | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 350 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.0 | V | $T_J = 25^\circ\text{C}, I_S = 17A, V_{GS} = 0V$ ③ |
| t_{rr} | Reverse Recovery Time | — | 16 | 24 | ns | $T_J = 25^\circ\text{C}, I_F = 17A, V_{DD} = 15V$ |
| Q_{rr} | Reverse Recovery Charge | — | 6.2 | 9.3 | nC | $di/dt = 100A/\mu s$ ③ |



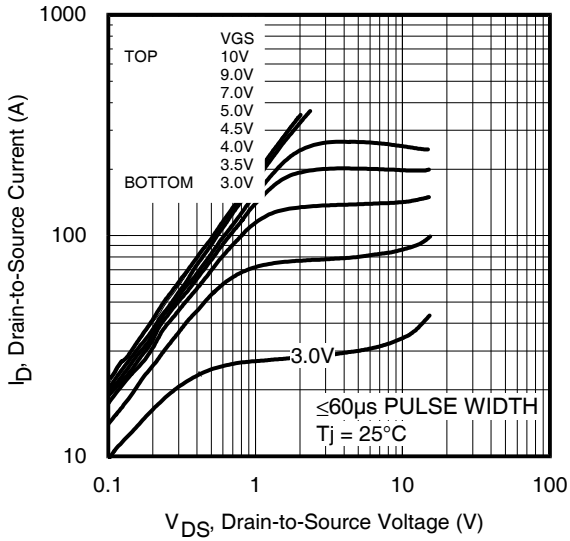


Fig 1. Typical Output Characteristics

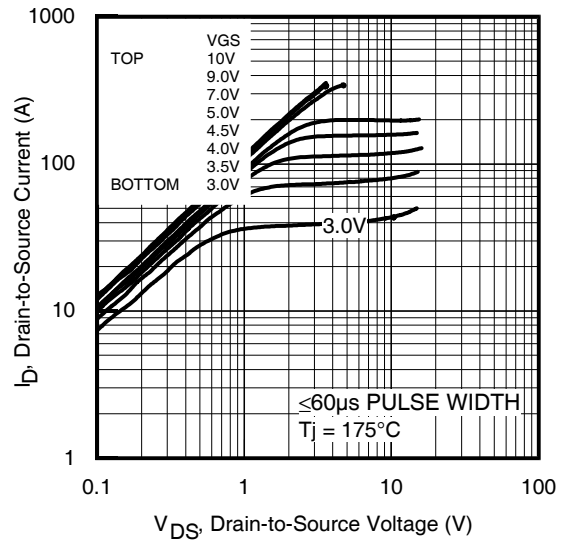


Fig 2. Typical Output Characteristics

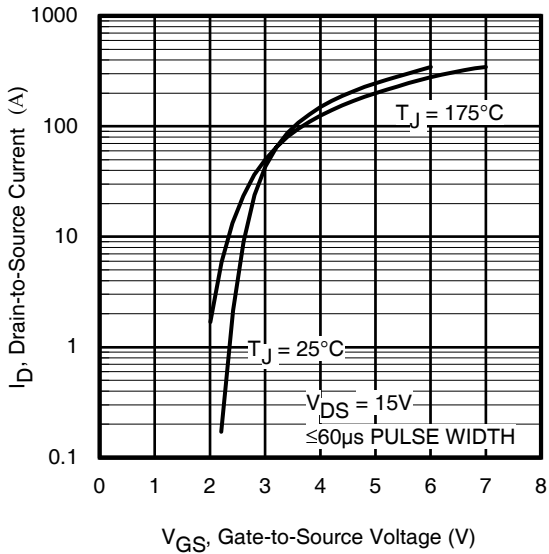


Fig 3. Typical Transfer Characteristics

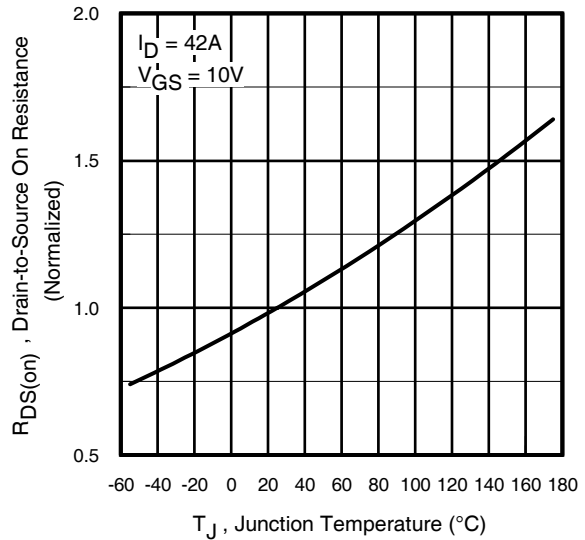


Fig 4. Normalized On-Resistance vs. Temperature

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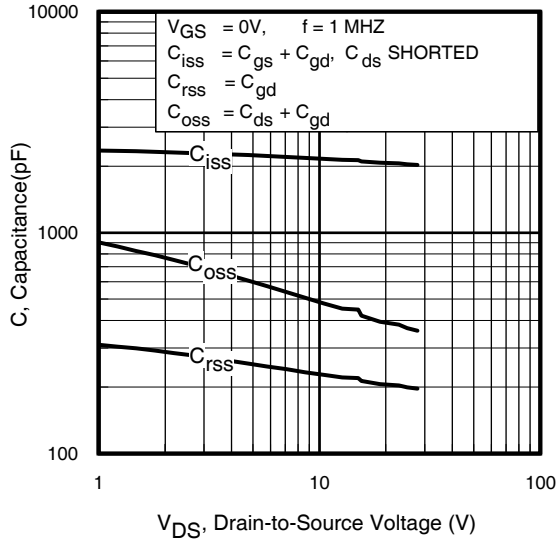


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

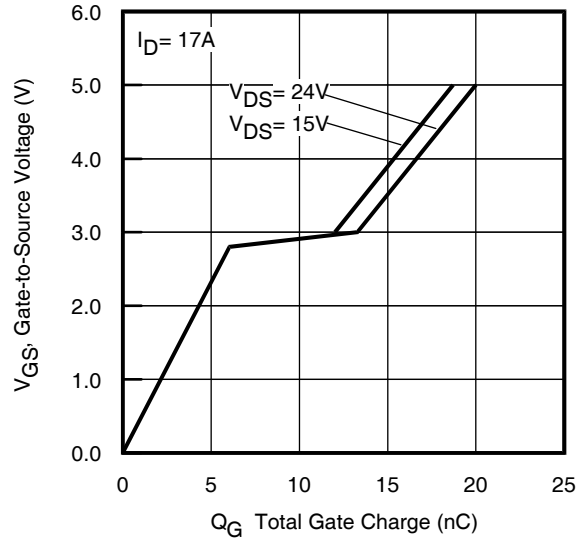


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

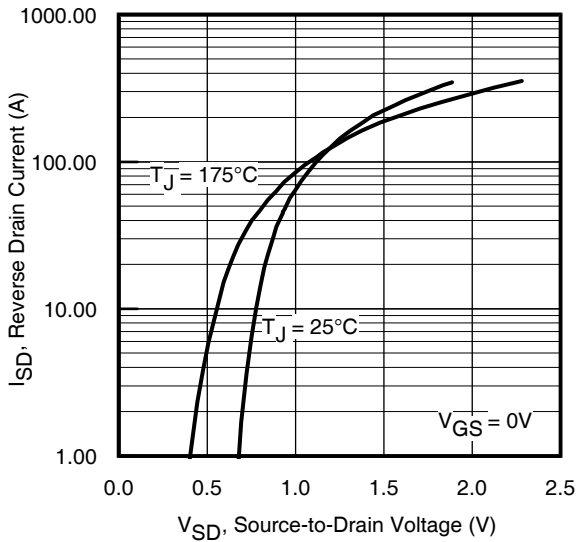


Fig 7. Typical Source-Drain Diode Forward Voltage

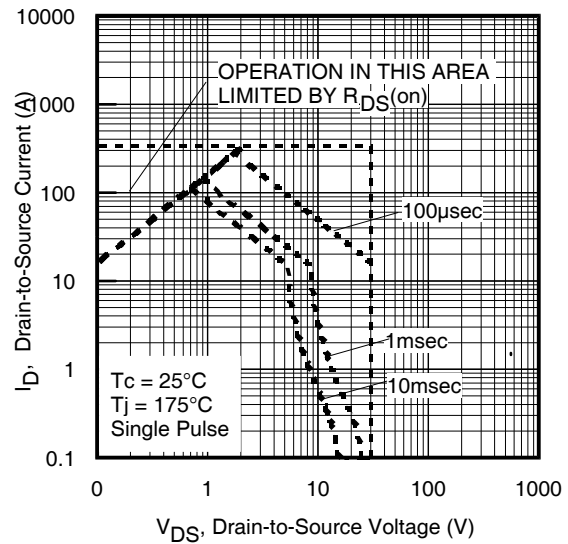


Fig 8. Maximum Safe Operating Area

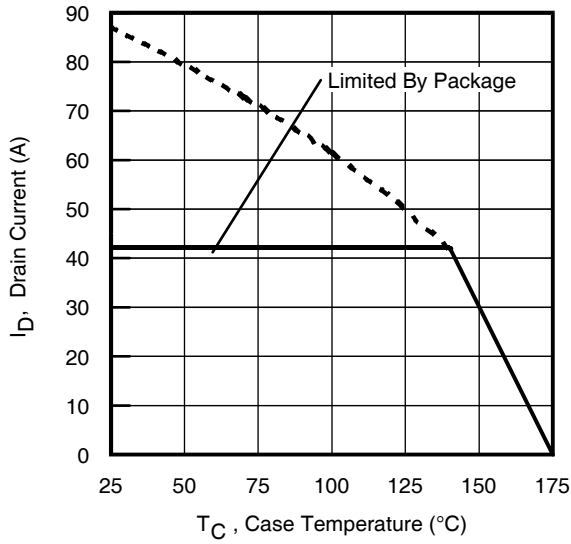


Fig 9. Maximum Drain Current vs. Case Temperature

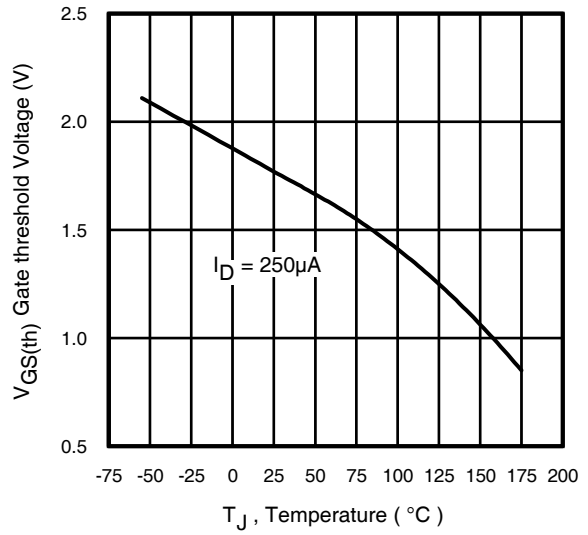


Fig 10. Threshold Voltage vs. Temperature

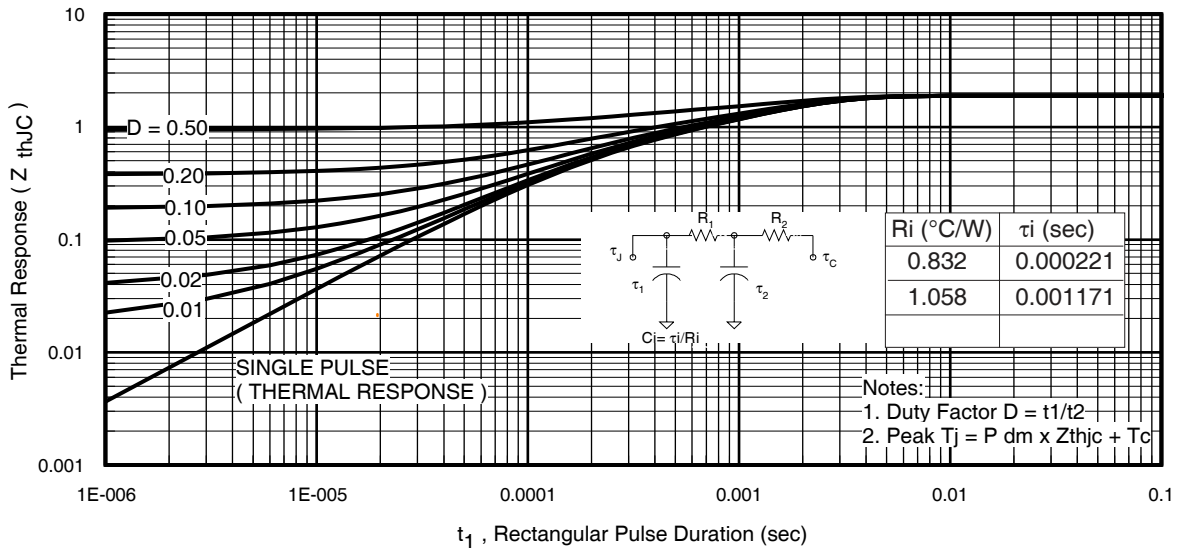


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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International
IR Rectifier

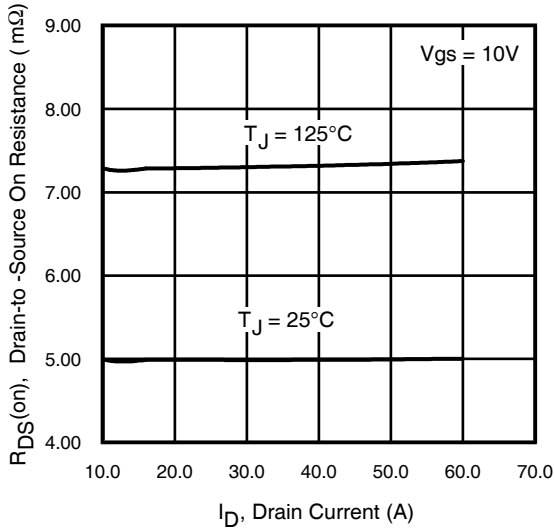


Fig 12. On-Resistance vs. Drain Current

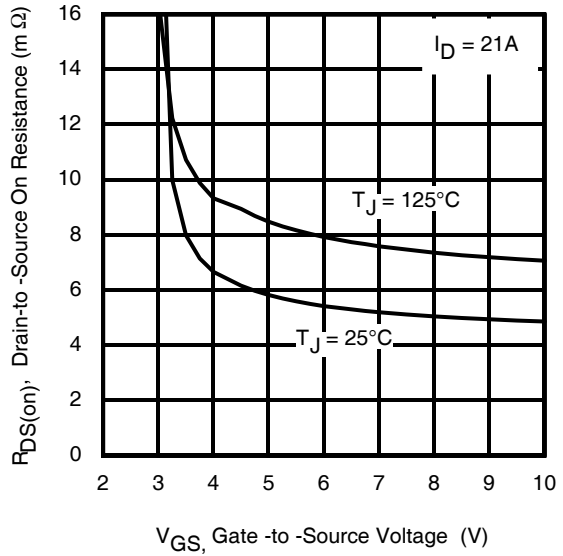


Fig 13. On-Resistance vs. Gate Voltage

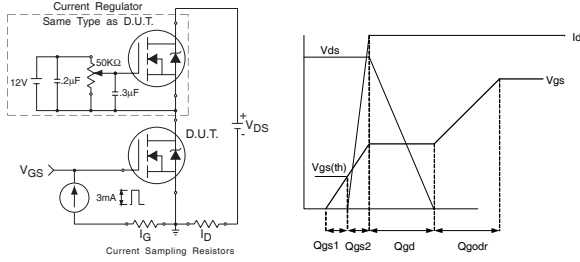


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

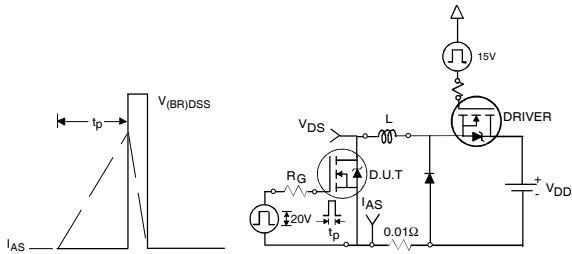


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

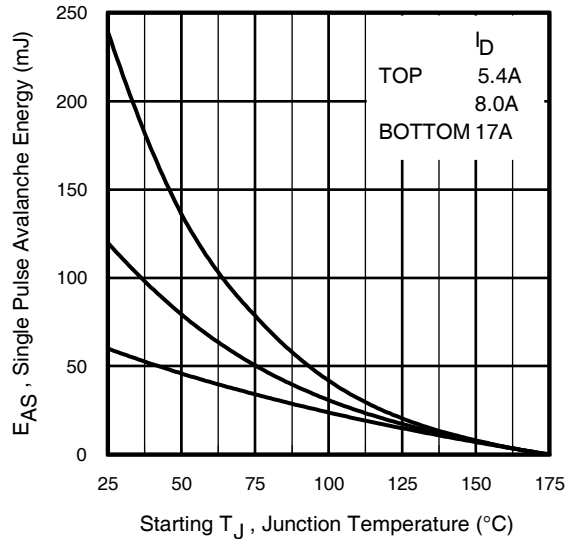


Fig 16. Maximum Avalanche Energy vs. Drain Current

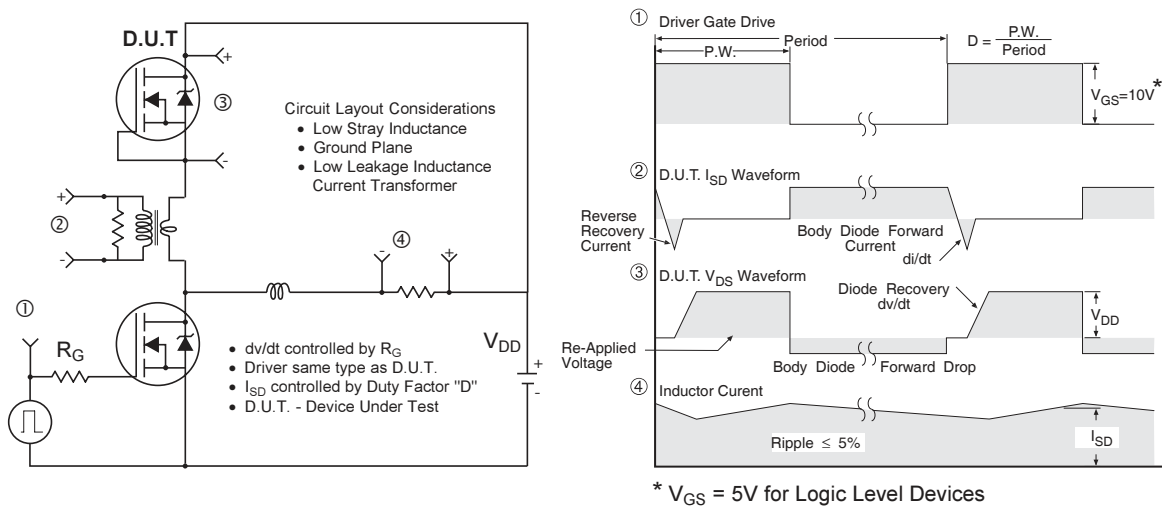


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

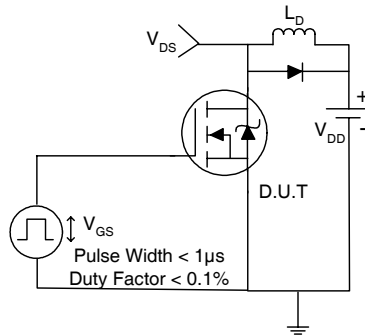


Fig 18a. Switching Time Test Circuit

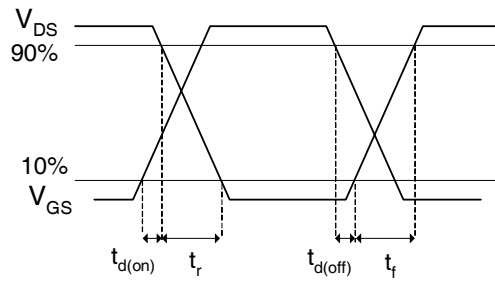


Fig 18b. Switching Time Waveforms

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + (Q_g \times V_g \times f) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2} , can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$

$$P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + (Q_g \times V_g \times f) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + (Q_{rr} \times V_{in} \times f)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in} . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

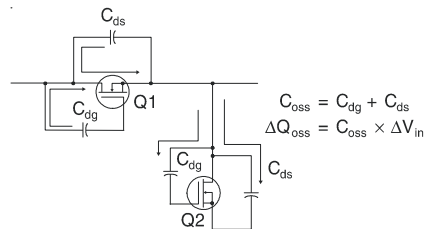
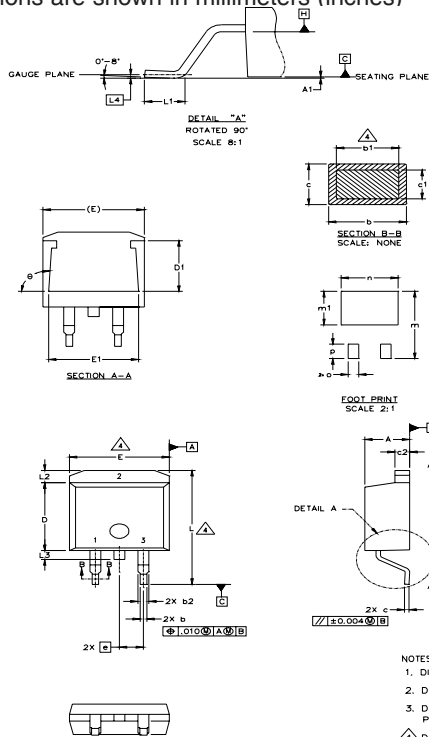


Figure A: Q_{oss} Characteristic

D²Pak Package Outline

Dimensions are shown in millimeters (inches)



| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | | 0.127 | | .005 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 4 |
| b2 | 1.14 | 1.40 | .045 | .055 | |
| c | 0.43 | 0.63 | .017 | .025 | |
| c1 | 0.38 | 0.74 | .015 | .029 | 4 |
| c2 | 1.14 | 1.40 | .045 | .055 | |
| D | 8.51 | 9.65 | .335 | .380 | 3 |
| D1 | 5.33 | | .210 | | |
| E | 9.65 | 10.67 | .380 | .420 | 3 |
| E1 | 6.22 | | .245 | | |
| e | 2.54 BSC | | .100 BSC | | |
| L | 14.61 | 15.88 | .575 | .625 | |
| L1 | 1.78 | 2.79 | .070 | .110 | |
| L2 | | 1.65 | | .065 | |
| L3 | 1.27 | 1.78 | .050 | .070 | |
| L4 | 0.25 BSC | | .010 BSC | | |
| m | 17.78 | | .700 | | |
| m1 | 8.89 | | .350 | | |
| n | 11.43 | | .450 | | |
| o | 2.08 | | .082 | | |
| p | 3.81 | | .150 | | |
| θ | 90° | 93° | 90° | 93° | |

LEAD ASSIGNMENTS

| | | |
|---------------|----------------------|---------------|
| HEXFET | IGBTs, CoPACK | DIODES |
| 1 - GATE | 1 - GATE | 1 - ANODE * |
| 2 - DRAIN | 2 - COLLECTOR | 2 - CATHODE |
| 3 - SOURCE | 3 - EMITTER | 3 - ANODE |

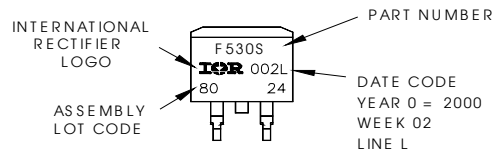
* PART DEPENDENT.

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

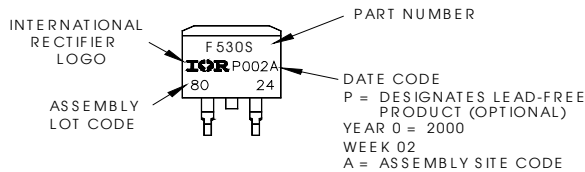
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"

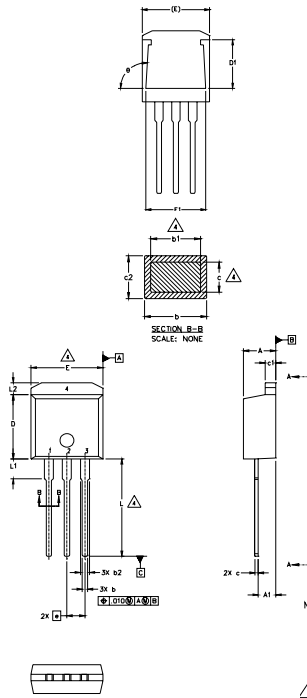


OR



IRF3709ZCS/LPbF

TO-262 Package Outline



| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | 4 |
| A1 | 2.03 | 2.92 | .080 | .115 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | |
| b2 | 1.14 | 1.40 | .045 | .055 | 4 |
| c | 0.38 | 0.63 | .015 | .025 | |
| c1 | 1.14 | 1.40 | .045 | .055 | 3 |
| c2 | 0.43 | .063 | .017 | .029 | |
| D | 8.51 | 9.65 | .335 | .380 | |
| D1 | 5.33 | | .210 | | 3 |
| E | 9.65 | 10.67 | .380 | .420 | |
| E1 | 6.22 | | .245 | | |
| e | 2.54 BSC | | .100 BSC | | |
| L | 13.46 | 14.09 | .530 | .555 | |
| L1 | 3.56 | 3.71 | .140 | .146 | |
| L2 | | 1.65 | | .065 | |

LEAD ASSIGNMENTS

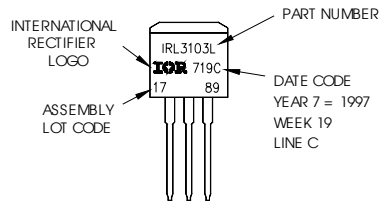
| HEXFET | IGBT |
|------------|--------------|
| 1.- GATE | 1- GATE |
| 2.- DRAIN | 2- COLLECTOR |
| 3.- SOURCE | 3- EMITTER |
| 4.- DRAIN | |

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 5. CONTROLLING DIMENSION: INCH.

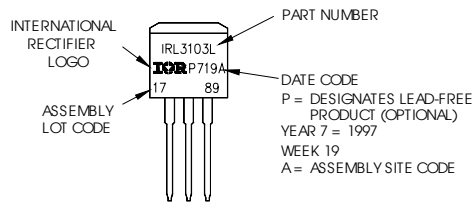
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

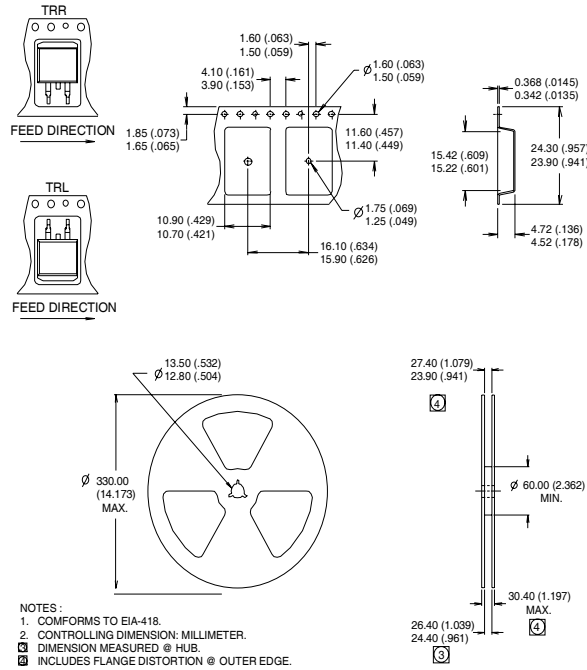
Note: "P" in assembly line position indicates "Lead-Free"



OR



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.42\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 17\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.
- ⑦ R_{θ} is measured at T_J of approximately 90°C .

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Consumer market.
 Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>