

GaAs MMIC 5-BIT DIGITAL PHASE SHIFTER, 15 - 18.5 GHz

Typical Applications

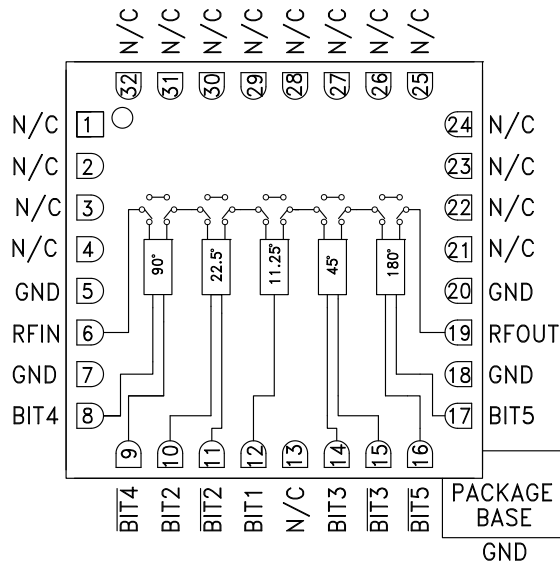
The HMC644ALC5 is ideal for:

- EW Receivers
- Weather & Military Radar
- Satellite Communications
- Beamforming Modules
- Phase Cancellation

Features

- Low RMS Phase Error: 3.5°
- Low Insertion Loss: 7.5 dB
- High Linearity: +40 dBm
- 360° Coverage, LSB = 11.25°
- 32 Lead Ceramic SMT Package: 25mm²

Functional Diagram



General Description

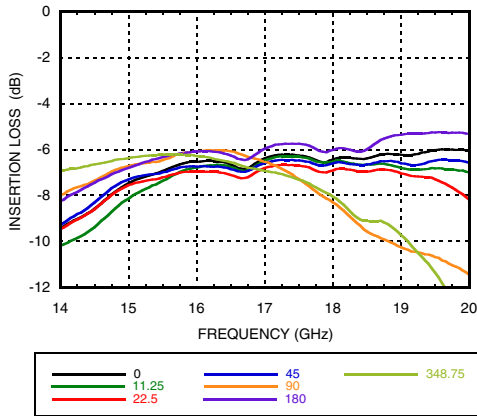
The HMC644ALC5 is a 5-bit digital phase shifter which is rated from 15 to 18.5 GHz, providing 360 degrees of phase coverage, with a LSB of 11.25 degrees. The HMC644ALC5 features very low RMS phase error of 3.5 degrees and extremely low insertion loss variation of ± 0.5 dB across all phase states. This high accuracy phase shifter is controlled with complementary logic of 0/-3V, and requires no fixed bias voltage. The HMC644ALC5 is housed in a compact 5x5 mm ceramic leadless SMT package and is internally matched to 50 Ohms with no external components. Simple external level shifting circuitry can be used to convert a positive CMOS control voltage into complementary negative control signals.

Electrical Specifications, $T_A = +25^\circ\text{C}$, 50 Ohm System, Control Voltage = 0/-3V

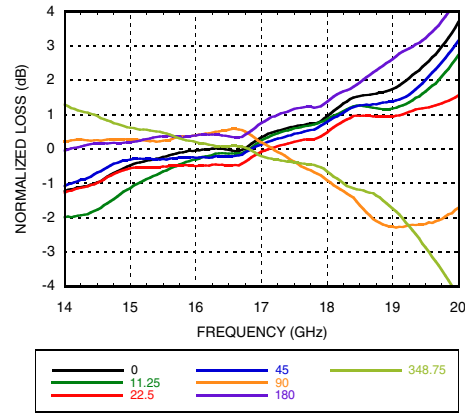
| Parameter | Min. | Typ. | Max. | Units |
|----------------------------------|------|-----------|-----------|-------|
| Frequency Range | 15 | | 18.5 | GHz |
| Insertion Loss | | 7.5 | 10 | dB |
| Input Return Loss | | 10 | | dB |
| Output Return Loss | | 12 | | dB |
| Phase Error | | ± 5 | +20 / -10 | deg |
| RMS Phase Error | | 3.5 | | deg |
| Insertion Loss Variation | | ± 0.5 | | dB |
| Input Power for 1 dB Compression | | 23 | | dBm |
| Input Third Order Intercept | | 40 | | dBm |
| Control Voltage Current | | <1 | | mA |

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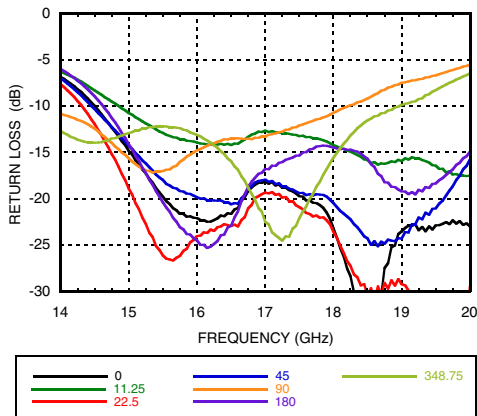
Insertion Loss, Major States Only



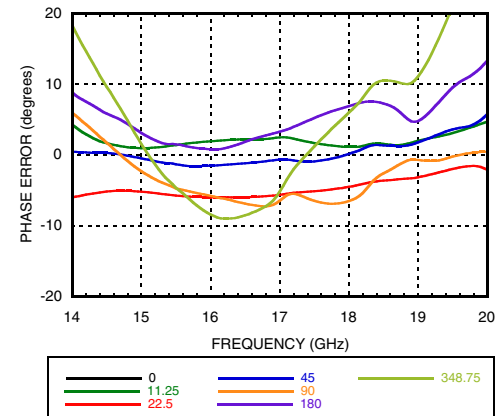
Normalized Loss, Major States Only



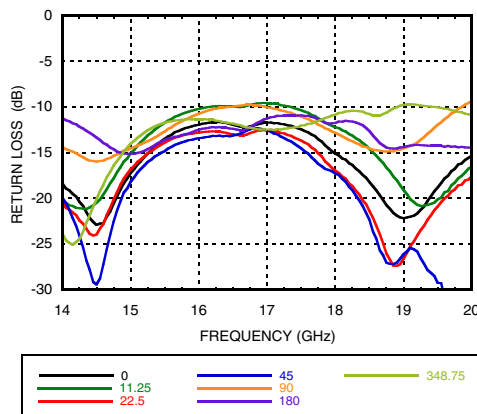
Input Return Loss, Major States Only



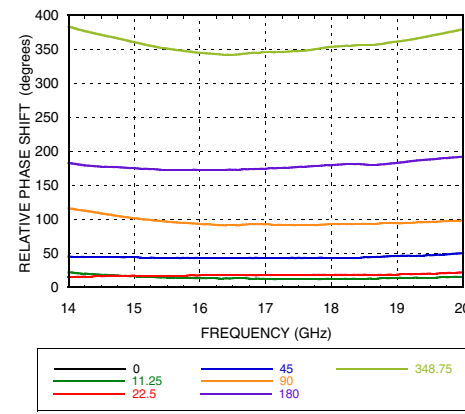
Phase Error, Major States Only



Output Return Loss, Major States Only

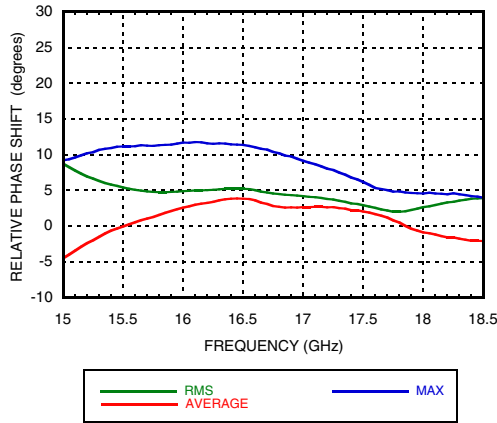


Relative Phase Shift Major States Including All Bits

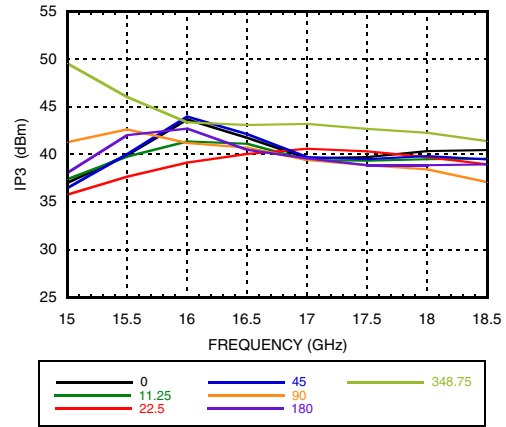


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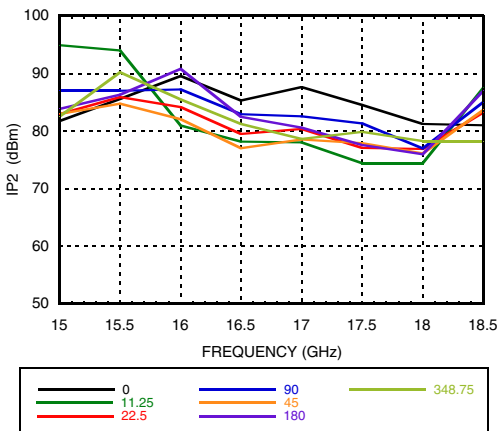
**Relative Phase Shift,
RMS, Average, Max, All States**



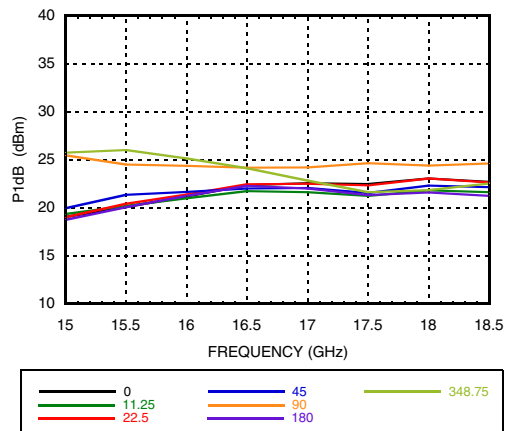
Input IP3, Major States Only



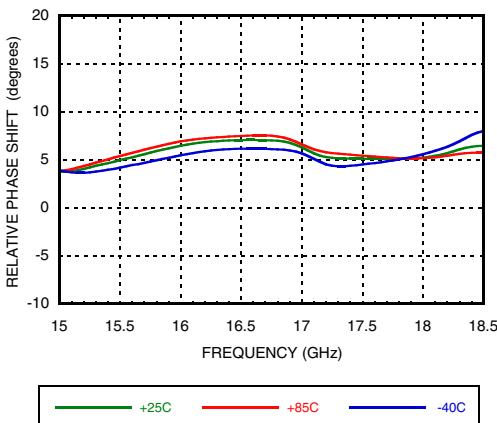
Input IP2, Major States Only



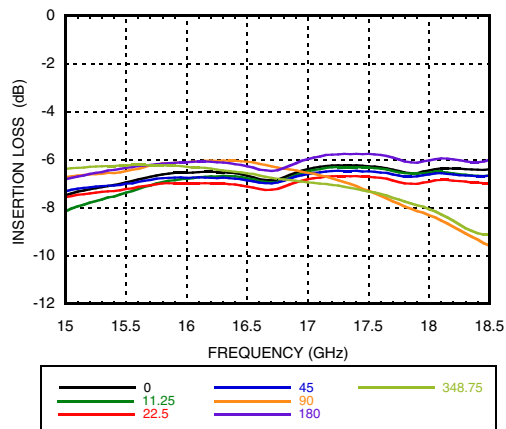
Input P1dB, Major States Only



RMS Phase Error vs. Temperature

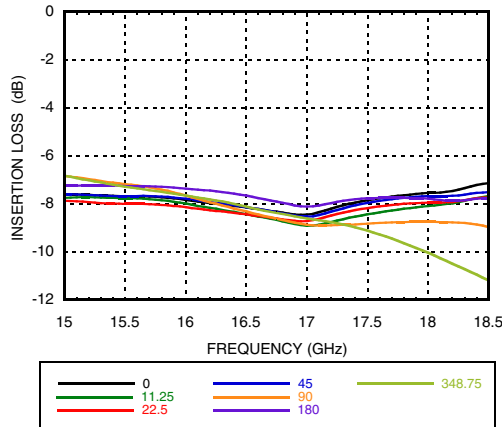


Insertion Loss +25C, Major States Only

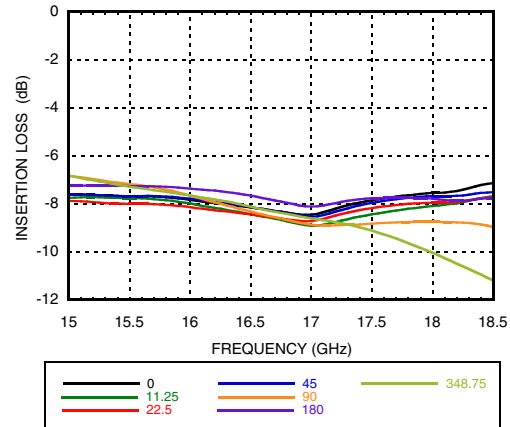


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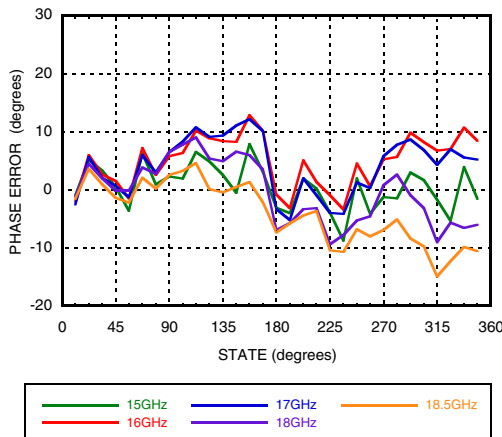
Insertion Loss +85C, Major States Only



Insertion Loss -40C, Major States Only



Phase Error vs. State, Major States Only



Absolute Maximum Ratings

| | |
|---|---------------------|
| Input Power (RFIN) | 26 dBm (T= +85 °C) |
| Channel Temperature (Tc) | 150 °C |
| Thermal Resistance (channel to ground paddle) | 150 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD sensitivity(HBM) | Class 0 Passed 100V |

Control Voltage

| State | Bias Condition |
|----------|-----------------------------|
| Low (0) | -2.5 to -3.5V @ 0.4 μA Typ. |
| High (1) | 0 to +0.3V @ 0.4 μA Typ. |



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Truth Table

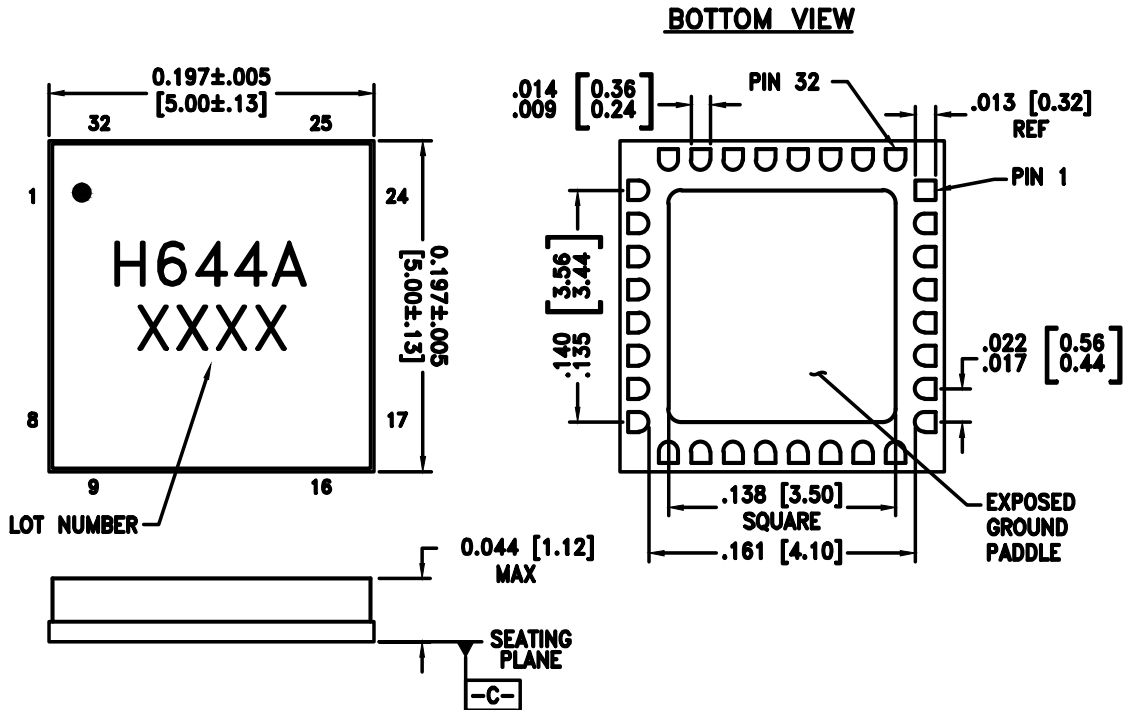
| Control Voltage Input | | | | | | | | | Phase Shift (Degrees) RFIN - RFOUT |
|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------------------------------|
| Bit 1 | Bit 2 | Bit 2 | Bit 3 | Bit 3 | Bit 4 | Bit 4 | Bit 5 | Bit 5 | |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | Reference* |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 11.25 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 22.5 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 45.0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 90.0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 180.0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 348.75 |

Any combination of the above states will provide a phase shift approximately equal to the sum of the bits selected.

***Reference corresponds to monotonic setting**

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Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER
50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.


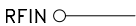

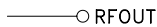
Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[2] |
|-------------|-----------------------|------------------|---------------------|--------------------------------|
| HMC644ALC5 | Alumina, White | Gold over Nickel | MSL3 ^[1] | H644A XXXX |

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX

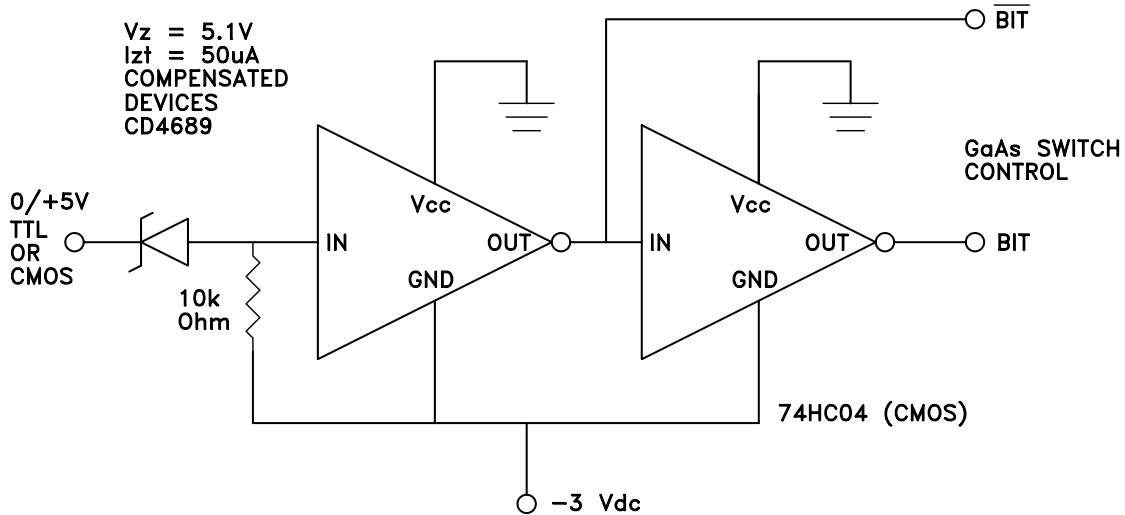
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Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|----------------------|--|--|---|
| 1 - 4, 13 21 - 32 | N/C | No connection required. These pins may be connected to RF/DC ground without affecting performance. | |
| 5, 7, 18, 20 | GND | These pins and exposed ground paddle must be connected to RF/DC ground. |  |
| 6 | RFIN | This port is DC coupled and matched to 50 Ohms. |  |
| 8, 10, 12, 14, 17 | BIT4, BIT2, BIT1, BIT3, BIT5 | Non-Inverted Control Input. See truth table and control voltage tables. |  |
| 9, 11, 15, 16 | $\overline{\text{BIT4}}$, $\overline{\text{BIT2}}$ $\overline{\text{BIT3}}$, $\overline{\text{BIT5}}$ | Inverted Control Input. See truth table and control voltage tables. | |
| 19 | RFOUT | This port is DC coupled and matched to 50 Ohms. |  |

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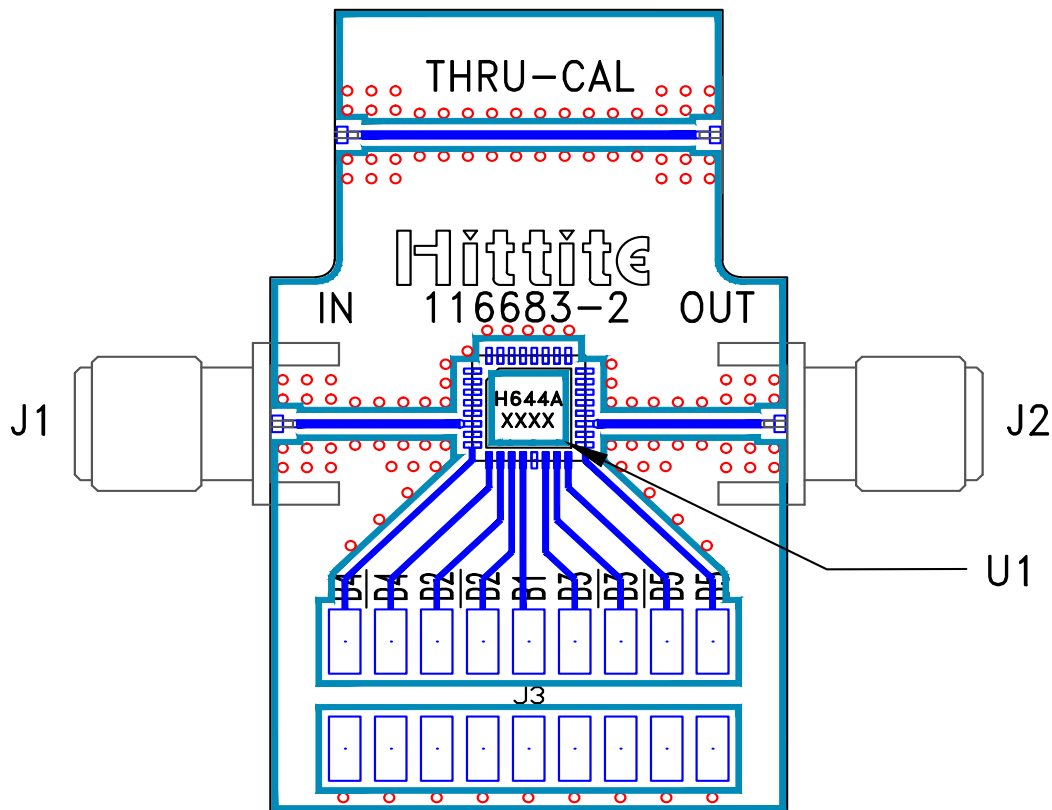
Application Circuit

This circuit converts a single line positive (0/+5V) control signal to complementary negative (0/-3V) control signals.



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Evaluation PCB



List of Materials for Evaluation PCB 116685 [1][3]

| Item | Description |
|---------|--|
| J1 - J2 | PCB Mount SMA RF Connector |
| J3 | Molex Header 2mm |
| U1 | HMC644ALC5 5-Bit Digital Phase Shifter |
| PCB [2] | 116683 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

[3] Please refer to part's pin description and functional diagram for pin out assignments on evaluation board.

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.