

# BLC8G24LS-241AV

Power LDMOS transistor

Rev. 2 — 2 December 2016

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

240 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2300 MHz to 2400 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty production test circuit.

$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 500\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.30\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2300 to 2400	28	56	15	44	-29 <a href="#">[1]</a>

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01% probability on CCDF per carrier.

### 1.2 Features and benefits

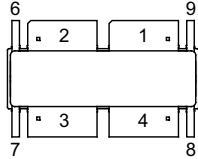
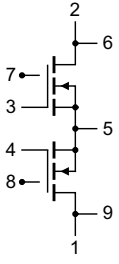
- Excellent ruggedness
- High-efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (2300 MHz to 2400 MHz)
- Asymmetric design to achieve optimum efficiency across the band
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2300 MHz to 2400 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		 <p style="text-align: right; font-size: small;">aaa-009150</p>
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source <a href="#">[1]</a>		
6	video decoupling (main)		
7	n.c.		
8	n.c.		
9	video decoupling (peak)		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC8G24LS-241AV	-	air cavity plastic earless flanged package; 8 leads	SOT1252-1

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-0.5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 28\text{ V}$ ; $I_{Dq} = 500\text{ mA}$ (main); $V_{GS(amp)peak} = 0.30\text{ V}$ ; $T_{case} = 80\text{ °C}$ ; $P_L = 56\text{ W}$	0.26	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.44\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 144\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	27	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 144\text{ mA}$	-	1.27	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 5.04\text{ A}$	-	100	166	$\text{m}\Omega$
<b>Peak device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	41	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	-	1.94	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 7.7\text{ A}$	-	69	112	$\text{m}\Omega$

**Table 7. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH;  $f_1 = 2300\text{ MHz}; f_2 = 2400\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 500\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.30\text{ V}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in an asymmetrical Doherty production test circuit in 2300 MHz to 2400 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 56\text{ W}$	13.3	14.5	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 56\text{ W}$	-	-10	-6	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 56\text{ W}$	38	43	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 56\text{ W}$	-	-29	-25	dBc

**Table 8. RF characteristics**

Test signal: pulsed CW;  $t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ %}; f = 2400\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 500\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.30\text{ V}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; tested in an asymmetrical Doherty production test circuit in 2300 MHz to 2400 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression		255	290	-	W

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLC8G24LS-241AV is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 500\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.30\text{ V}$ ;  $P_L = 240\text{ W}$  (CW);  $f = 2300\text{ MHz}$ .

### 7.2 Impedance information

**Table 9. Typical impedance of main device**

Measured load-pull data of main device;  $I_{Dq} = 1000\text{ mA}$ ;  $V_{DS} = 28\text{ V}$ . Typical values unless otherwise specified.

f	Z <sub>S</sub> <sup>[1]</sup>	Z <sub>L</sub> <sup>[1]</sup>	P <sub>L</sub> <sup>[2]</sup>	η <sub>D</sub> <sup>[2]</sup>	G <sub>p</sub> <sup>[2]</sup>
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
<b>Maximum power load</b>					
2300	1.1 – j3.5	1.6 – j4.4	171	56.20	15.2
2350	1.6 – j3.6	1.7 – j4.5	178	57.60	15.3
2400	1.9 – j4.5	1.5 – j4.6	175	55.10	16.0
<b>Maximum drain efficiency load</b>					
2300	1.1 – j3.5	3.1 – j3.5	127	65.50	17.1
2350	1.6 – j3.6	2.7 – j3.3	130	65.30	17.4
2400	1.9 – j4.5	2.4 – j3.5	131	64.70	18.1

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.

**Table 10. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{Dq} = 1230\text{ mA}$ ;  $V_{DS} = 28\text{ V}$ . Typical values unless otherwise specified.

f	Z <sub>S</sub> <sup>[1]</sup>	Z <sub>L</sub> <sup>[1]</sup>	P <sub>L</sub> <sup>[2]</sup>	η <sub>D</sub> <sup>[2]</sup>	G <sub>p</sub> <sup>[2]</sup>
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
<b>Maximum power load</b>					
2300	1.0 – j5.3	4.0 – j4.5	252	55.30	16.5
2350	1.9 – j5.4	3.9 – j4.5	248	55.00	16.1
2400	2.1 – j6.5	4.6 – j4.5	245	53.80	16.8
<b>Maximum drain efficiency load</b>					
2300	1.0 – j5.3	2.7 – j2.4	190	63.90	18.3
2350	1.9 – j5.4	2.2 – j2.5	175	63.70	18.1
2400	2.1 – j6.5	2.3 – j2.7	176	63.00	18.8

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.

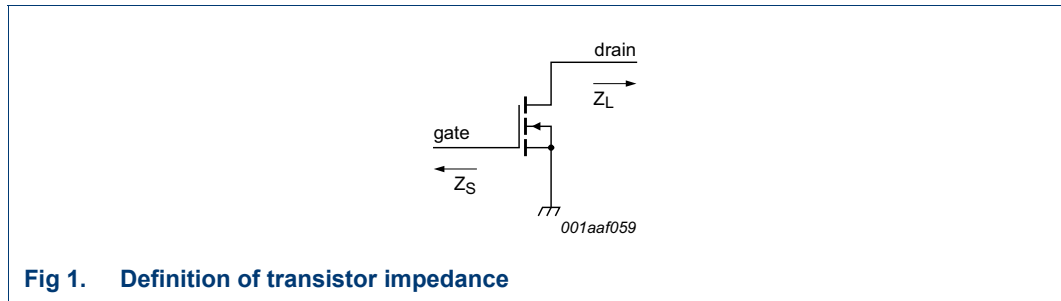
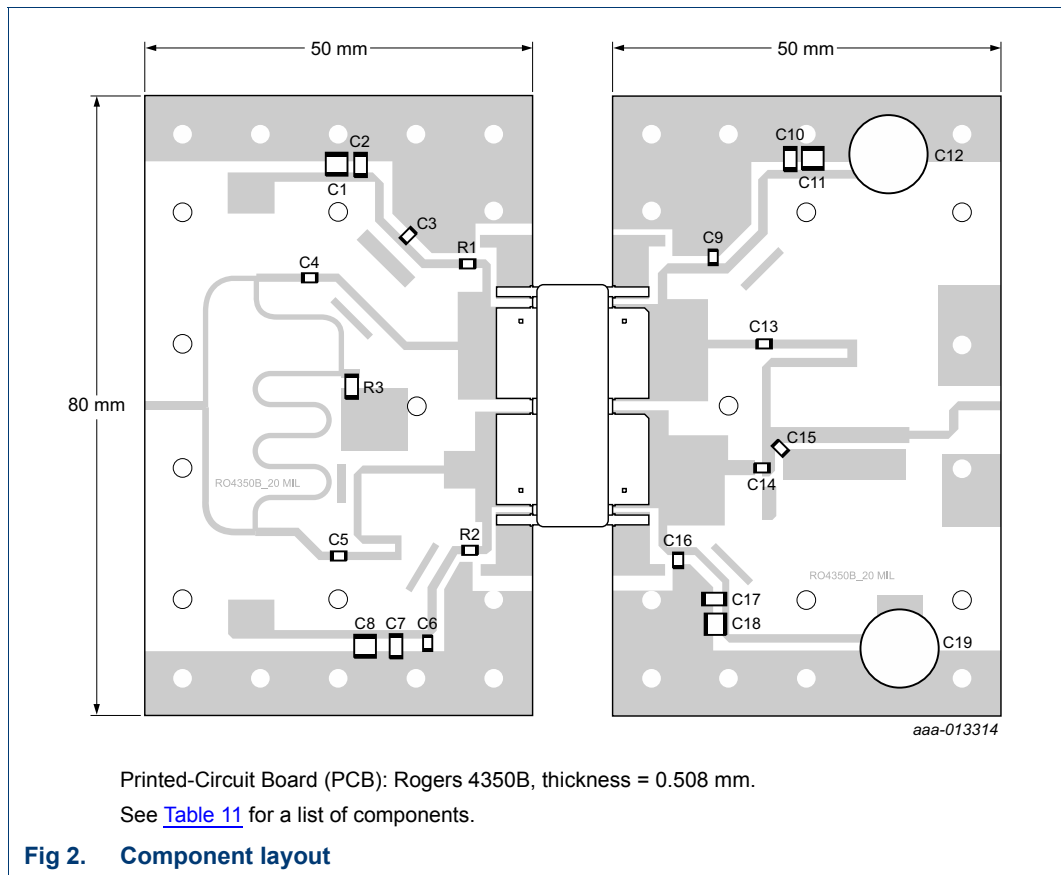


Fig 1. Definition of transistor impedance

### 7.3 VBW in Doherty operation

The BLC8G24LS-241AV shows 80 MHz (typical) video bandwidth in Doherty test circuit in 2.35 GHz at  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 500\text{ mA}$  and  $V_{GS(amp)peak} = 0.30\text{ V}$ .

### 7.4 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B, thickness = 0.508 mm.  
See [Table 11](#) for a list of components.

Fig 2. Component layout

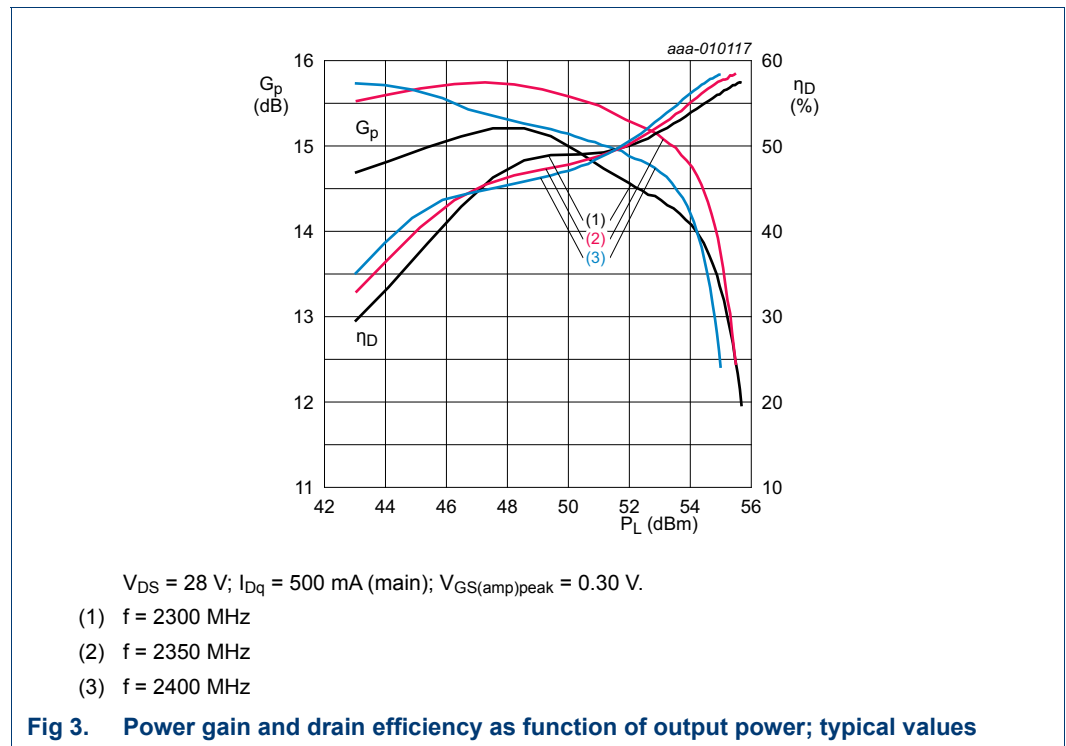
**Table 11. List of components**

For test circuit see [Figure 2](#).

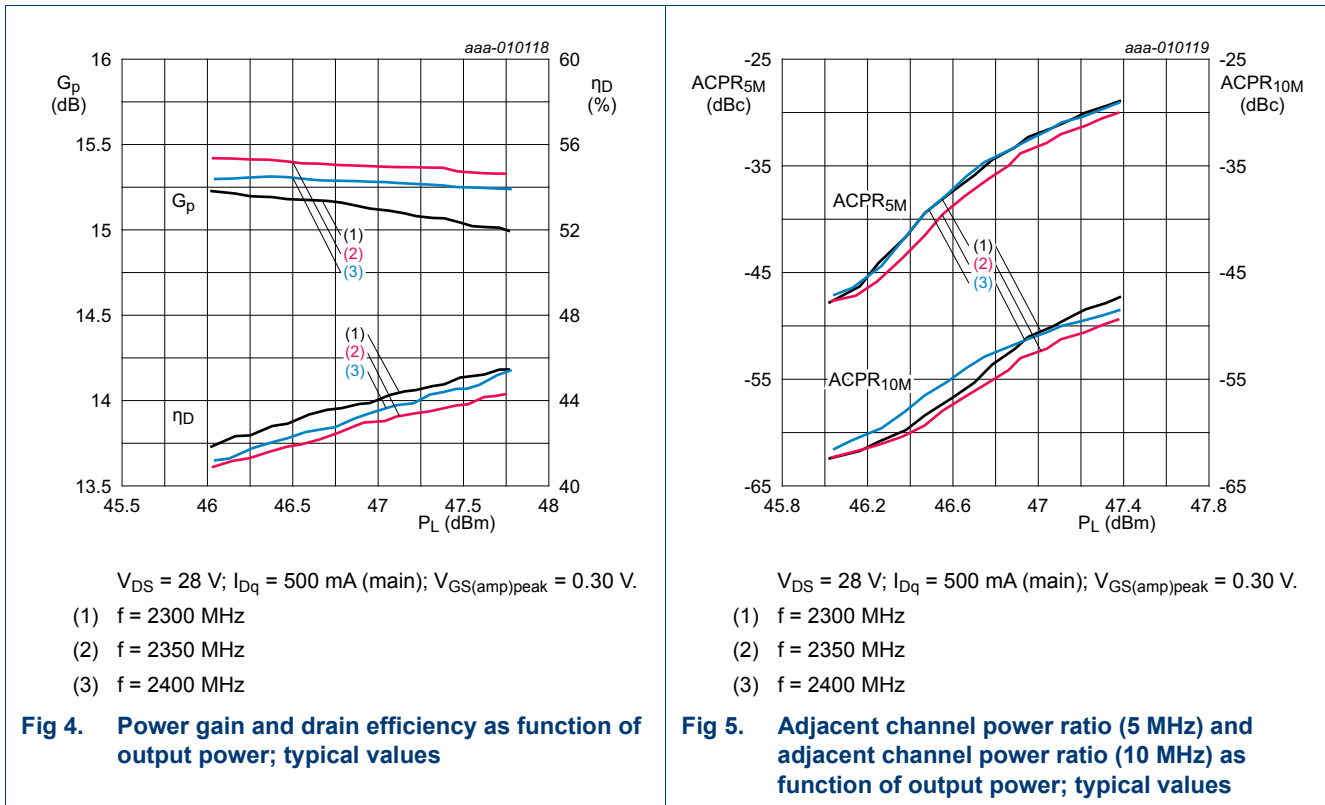
Component	Description	Value	Remarks
C1, C8, C11, C18	multilayer ceramic chip capacitor	10 $\mu$ F	Murata
C2, C7, C10, C17	multilayer ceramic chip capacitor	1 $\mu$ F	Murata
C3, C4, C5, C6, C9, C13, C14, C16	multilayer ceramic chip capacitor	12 pF	ATC 800B
C12, C19	electrolytic capacitor	2200 $\mu$ F, 50 V	
C15	multilayer ceramic chip capacitor	0.8 pF	ATC 600F
R1, R2	resistor	9.1 $\Omega$	Vishay Dale: SMD 0805
R3	resistor	50 $\Omega$	Vishay Dale: SMD 0805

## 7.5 Graphical data

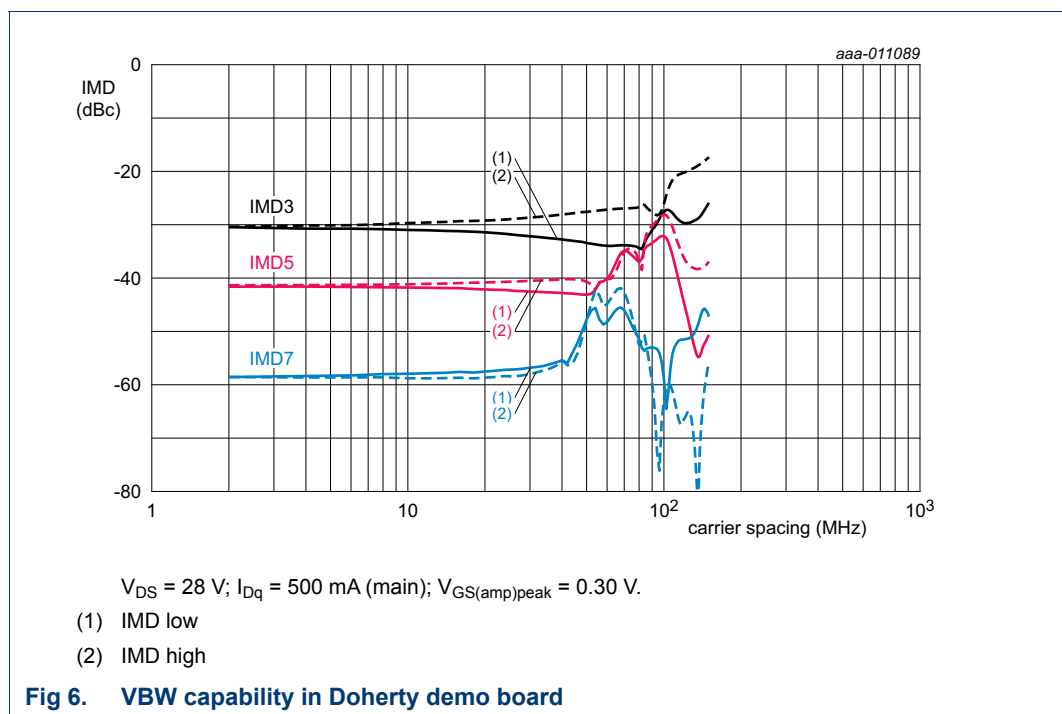
### 7.5.1 Pulsed CW



7.5.2 1-Carrier W-CDMA



7.5.3 2-Tone VBW



8. Package outline

Air cavity plastic earless flanged package; 8 leads

SOT1252-1

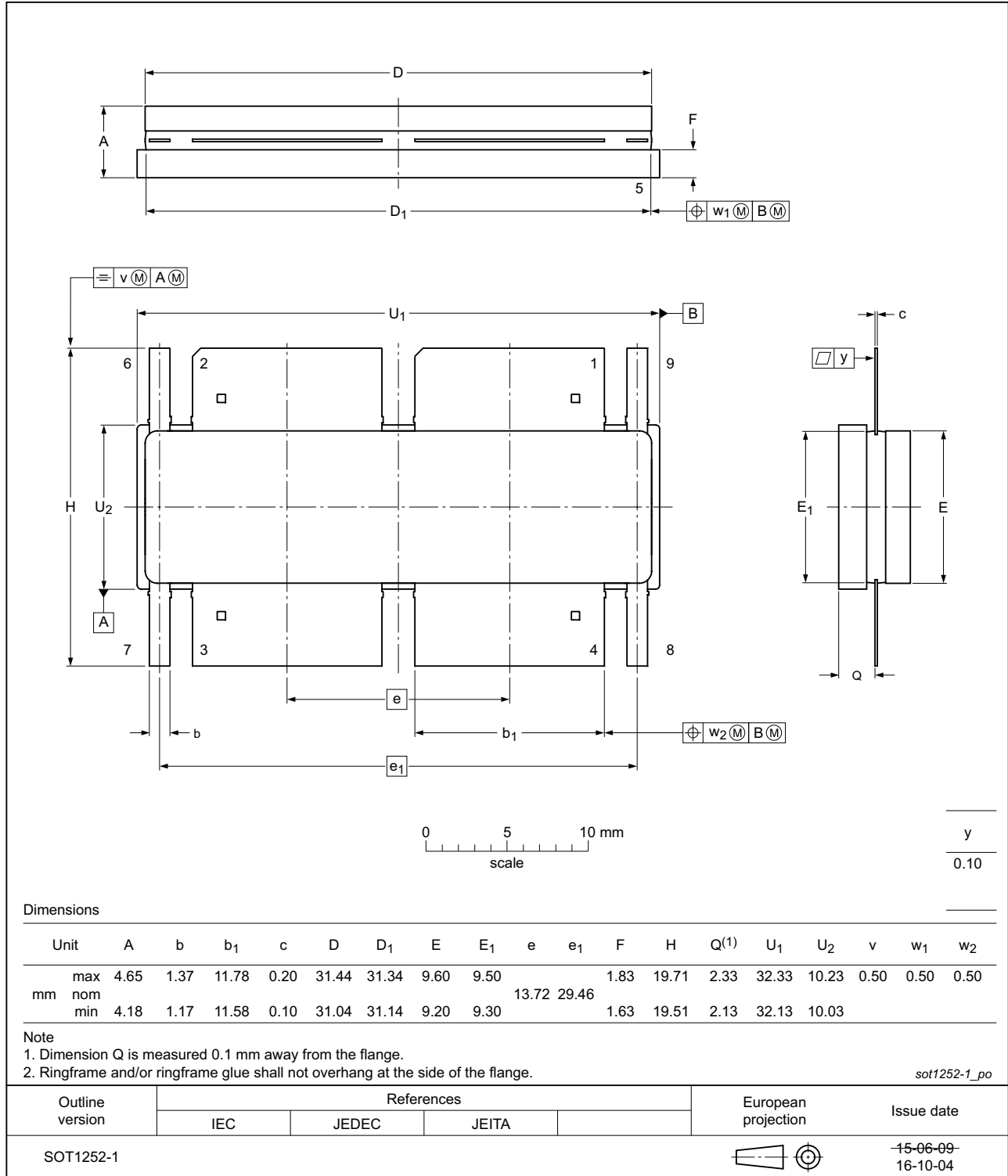



Fig 7. Package outline SOT1252-1



## 9. Handling information

CAUTION	
	<p>This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.</p> <p>Such precautions are described in the <i>ANSI/ESD S20.20</i>, <i>IEC/ST 61340-5</i>, <i>JESD625-A</i> or equivalent standards.</p>

**Table 12. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

- [1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.
- [2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

**Table 13. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video Bandwidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 14. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC8G24LS-241AV v.2	20161202	Product data sheet	-	BLC8G24LS-241AV v.1
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Figure 7 on page 8</a>: updated package outline drawing SOT1252-1</li> <li>• <a href="#">Section 9 on page 9</a>: updated Handling information</li> </ul>			
BLC8G24LS-241AV v.1	20160209	Product data sheet	-	-

## 12. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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