

# **General Purpose CMOS Logic IC**

# **Automotive Single 2-input OR gate**

## BD7LS32G-C

# **General Description**

The BD7LS32G-C is a Single 2-input OR gate and qualified for automotive applications. This is designed for 1.65 V to 5.5 V power supply voltage operation. When it is power down, the Output Tolerant circuit protects the output circuit from the back flow current through the connected system.

#### **Features**

- AEC-Q100 Qualified<sup>(Note 1)</sup>
  - > 4000 V Human-body Model
  - > 1000 V Charged-device Model
- Low Power Consumption
- 5.5 V Tolerant Inputs
- Output Tolerant Supports Partial Power Down Mode Operation
- Package SSOP5 is Similar to SOT-23-5(JEDEC) (Note 1) Grade 1

# **Applications**

Automotive

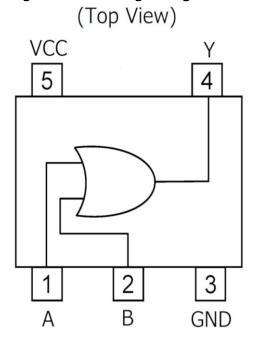
## **Key Specifications**

■ Supply Voltage Range: 1.65 V to 5.5 V ■ Low Current Consumption ( $I_{CC}$ ): 10  $\mu$ A (Max) ■ Operating Temperature Range: -40 °C to +125 °C ■ Max Propagation Delay Time: 12.0 ns (@3.0 V) ■ Output Drive Capability:  $\pm 24$  mA (@3.0 V)

Package W(Typ) x D (Typ) x H (Max) SSOP5 2.9 mm x 2.8 mm x 1.25 mm



## **Pin Configuration and Logic Diagram**



## **Pin Descriptions**

Pin No.	Pin Name	Function	I/O
1	Α	Input	I
2	В	Input	I
3	GND	Ground	-
4	Υ	Output	0
5	VCC	Power supply	72

## **Truth Table**

Inp	Output				
Α	A B				
L	L	L			
L	Н	Н			
Н	L	Н			
Н	Н	Н			

# Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage Range	V <sub>CC</sub>	-0.5 to +6.5	V
Input Voltage Range	V <sub>IN</sub>	-0.5 to +6.5	V
Input Diode Current (V <sub>IN</sub> < 0)	${ m I}_{ m IK}$	-50	mA
Output Diode Current (V <sub>0</sub> < 0)	$I_{OK}$	-50	mA
Output Current	Io	±50	mA
VCC-GND Current	$I_{CC}$	±50	mA
Maximum Junction Temperature	Tjmax	+150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance (Note 1)

110000000000000000000000000000000000000					
Davagachou	Cymahal	Thermal Re	1.126		
Parameter	Symbol	1s <sup>(Note 3)</sup>	2s2p <sup>(Note 4)</sup>	Unit	
SSOP5					
Junction to Ambient	$\theta_{JA}$	376.5	185.4	°C/W	
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	Ψ <sub>JT</sub>	40	30	°C/W	

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt
Тор		

Thickness
70 µm

Layer Number of	Material	Board Size			
Measurement Board	Material	Doard Size			
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt			

Тор		2 Internal Laye	ers	Bottom		
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness	
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm	

<sup>(</sup>Note 1) Based on JESD51-2A (Still-Air).

# **Recommended Operating Conditions**

necommended operating conditions									
Parameter	Symbol	Min	Тур	Max	Unit	Conditions			
Supply Voltage	V	1.65	-	5.5	V	Operating			
Supply Voltage	V <sub>CC</sub>	1.5	-	5.5	V	Data Retention Only			
Input Voltage	$V_{IN}$	0	-	5.5	V	-			
Output Voltage	Vo	0	-	V <sub>CC</sub>	V	-			
	Δt/Δv	-	-	20	ns /\/	V <sub>CC</sub> = 1.65 V to 1.95 V			
Input Transition Rise or Fall						V <sub>CC</sub> = 2.3 V to 2.7 V			
Rate		-	-	10	ns/V	V <sub>CC</sub> = 3.0 V to 3.6 V			
		-	-	5		V <sub>CC</sub> = 4.5 V to 5.5 V			
Operating Temperature	Topr	-40	-	+125	°C	-			

<sup>(</sup>Note) The recommended operating conditions are the range where operation is guaranteed. If this ranges are exceeded, operation is not guaranteed even within the absolute maximum ratings. Unused inputs must be tied to either  $V_{CC}$  or GND.

<sup>(</sup>Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

<sup>(</sup>Note 3) Using a PCB board based on JESD51-3. (Note 4) Using a PCB board based on JESD51-7.

# **Electrical Characteristics**

# (Unless otherwise specified $V_{CC}$ = 1.65 V to 5.5 V and Ta = -40 °C to +125 °C)

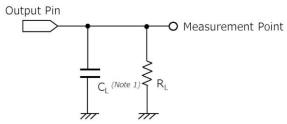
Darameter	Cumbal	Min	Tura	Max	Unit	Conditions		
Parameter	Symbol	Min	Тур	Max	Unit	V <sub>CC</sub>		
Input "H" Voltage	V <sub>IH</sub>	$V_{CC} \times 0.7$	-	-	V	1.65 V to 5.5 V	-	
Input "L" Voltage	V <sub>IL</sub>	-	-	$V_{CC} \times 0.3$	V	1.65 V to 5.5 V	-	
		V <sub>CC</sub> - 0.1	-	-		1.65 V to 5.5 V	$I_{OH} = -100 \ \mu A$	
		1.2	-	-		1.65 V	$I_{OH} = -4 \text{ mA}$	
Output "H" Voltage	V <sub>OH</sub>	1.8	-	-	V	2.3 V	$I_{OH} = -8 \text{ mA}$	
Output 11 Voltage	VOH	2.3	ı	-	•	3.0 V	$I_{OH} = -16 \text{ mA}$	
		2.1	-	-		3.0 V	$I_{OH} = -24 \text{ mA}$	
		3.4	ı	-		4.5 V	$I_{OH} = -32 \text{ mA}$	
	V <sub>OL</sub>	-	-	0.10		1.65 V to 5.5 V	$I_{OL} = 100 \mu A$	
		-	-	0.45		1.65 V	$I_{OL} = 4 \text{ mA}$	
Output "L" Voltage		-	-	0.40	V	2.3 V	$I_{OL} = 8 \text{ mA}$	
Output L voitage		-	-	0.60	\ \ \	3.0 V	$I_{OL} = 16 \text{ mA}$	
		-	-	0.90		3.0 V	$I_{OL} = 24 \text{ mA}$	
		-	1	1.00		4.5 V	$I_{OL} = 32 \text{ mA}$	
Input Current	I <sub>IN</sub>	-	-	±2	μΑ	0 V to 5.5 V	$V_{IN} = 5.5 \text{ V or GND}$	
Power Off Output Pin Current	I <sub>OFF</sub>	-	1	10	μΑ	0 V	$V_{IN}$ or $V_O = 5.5 \text{ V}$	
Quiescent Supply Current	$I_{CC}$	-	ı	10	μΑ	1.65 V to 5.5 V	-	
Supply Current Increase	$\Delta I_{\sf CC}$	-	ı	600	μA	3.0 V to 5.5 V	One Input: V <sub>CC</sub> - 0.6 V Other Inputs: V <sub>CC</sub> or GND	
Input Capacitance	CI	-	4	-	pF	3.3 V	$V_{IN} = V_{CC}$ or GND Ta = 25 °C	

# **Switching Characteristics**

(Unless otherwise specified  $V_{CC}$  = 1.65 V to 5.5 V and Ta = -40 °C to +125 °C)

Parameter	arameter Symbol FROM TO Min		Тур	Max	Unit	Conditions										
rarameter	Syllibol	(Input)	(Output)	141111	тур	Max	Max Offic	V <sub>CC</sub>								
				1.4	-	15.0		1.65 V to 1.95 V	-							
Propagation	t <sub>PLH</sub>	A or B	Y	0.6	-	13.0	nc	2.3 V to 2.7 V	-							
Delay Time		t <sub>PHL</sub> A OI B	AUID	AUID	AUD	A 01 D	AUID	AUID	AUID	1010	0.5	-	12.0	ns	3.0 V to 3.6 V	-
				0.5	-	10.0		4.5 V to 5.5 V	-							
Power		-	-	-	25	-	pF	3.3 V	f = 10 MHz, Ta = 25 °C							
Dissipation Capacitance	C <sub>PD</sub>	-	-	-	32	-	pF	5.0 V	f = 10 MHz, Ta = 25 °C							

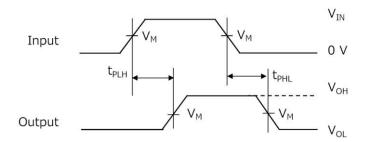
## **Parameter Measurement Conditions**



Measurement circuit for  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$ 

Vcc	V <sub>IN</sub>	V <sub>M</sub>	C <sub>L</sub> (Note 1)	R∟	tr/tf (Inputs)
1.65 V to 1.95 V	Vcc	0.5 × V <sub>CC</sub>	30 pF	1k Ω	≤ 2 ns
2.3 V to 2.7 V	Vcc	0.5 × V <sub>CC</sub>	30 pF	500 Ω	≤ 2 ns
3.0 V to 3.6 V	3.0 V	1.5 V	50 pF	500 Ω	≤ 2.5 ns
4.5 V to 5.5 V	Vcc	0.5 × V <sub>CC</sub>	50 pF	500 Ω	≤ 2.5 ns

(Note 1)  $C_L$  includes probe and test board capacitance.



Measurement Circuit and Timing Chart

## **Typical Performance Curves**

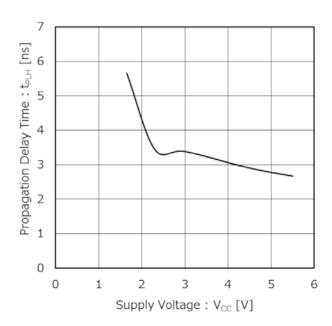


Figure 1. Propagation Delay Time:  $t_{PLH}$  vs Supply Voltage:  $V_{CC}$  (Ta = 25 °C)

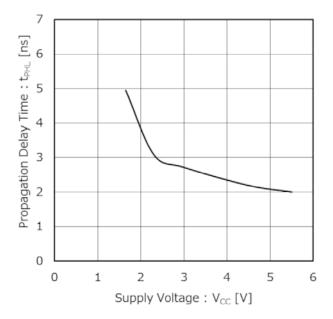


Figure 3. Propagation Delay Time:  $t_{PHL}$  vs Supply Voltage:  $V_{CC}$  (Ta = 25 °C)

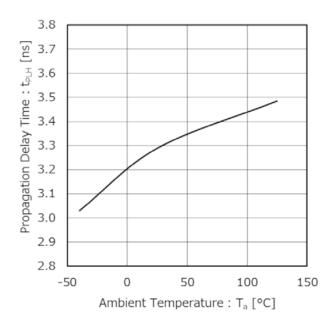


Figure 2. Propagation Delay Time:  $t_{PLH}$  vs Ambient Temperature: Ta  $(V_{CC} = 3.3 \text{ V})$ 

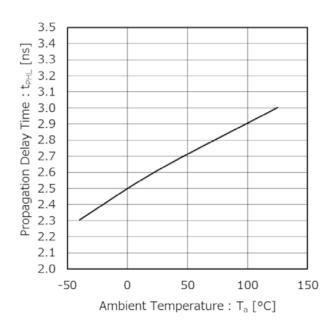


Figure 4. Propagation Delay Time:  $t_{PHL}$  vs Ambient Temperature: Ta  $(V_{CC} = 3.3 \text{ V})$ 

# **Operational Notes**

#### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

## 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

#### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

#### **4.** Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

#### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

#### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

#### 7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

# 8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

#### 10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

# **Operational Notes - continued**

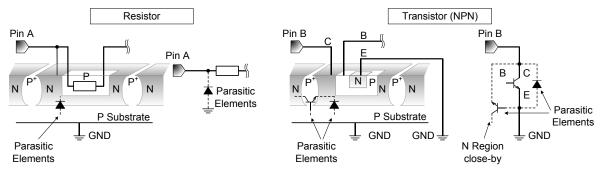
## 11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these



diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

#### Example of Monolithic IC Structure

#### 12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

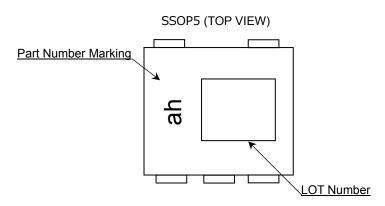
**Ordering Information** 

B D 7 L S 3 2 G - CTL

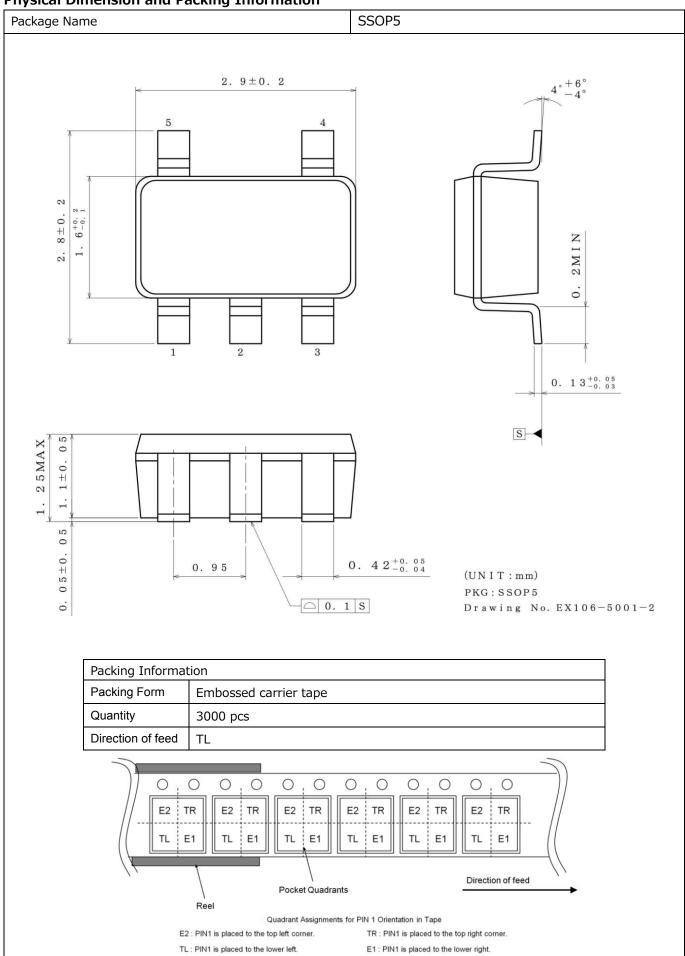
Package G: SSOP5 Product Rank
C: for Automotive
Packaging and forming specification

TL: Embossed tape and reel

# **Marking Diagram**



# **Physical Dimension and Packing Information**



# **Revision History**

Date	Revision	Changes
21.Apr.2020	001	New Release

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JÁPAN	USA	EU	CHINA
CLASSII	CLASSII	CLASS II b	CLASSIII
CLASSIV		CLASSⅢ	

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- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
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- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
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For details, please refer to ROHM Mounting specification

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  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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