

Switch-Mode Single Cell Li-Ion Charger with USB-OTG

General Description

The RT9469 is a switch-mode single cell Li-Ion/Li-Polymer battery charger for portable applications. It integrates a synchronous PWM controller, power MOSFETs, input current sensing and regulation, and high accuracy voltage regulation and charge termination circuits. Besides, the charging current is regulated through the integrated sensing resistors. The RT9469 also features USB On-The-Go (OTG) support.

The RT9469 optimizes the charging task by using a control algorithm to vary the charge rate via different modes, including pre-charge mode, fast charge mode, and constant voltage mode. The key charge parameters are programmable via the I²C interface. The RT9469 resumes the charge cycle whenever the battery voltage falls below an internal recharge threshold, and automatically enters sleep mode when the input power supply is removed.

Other features include under-voltage protection, over-voltage protection, thermal regulation and reverse leakage protection.

The RT9469 is available in the small WL-CSP-25B 2.52x2.52 packages.

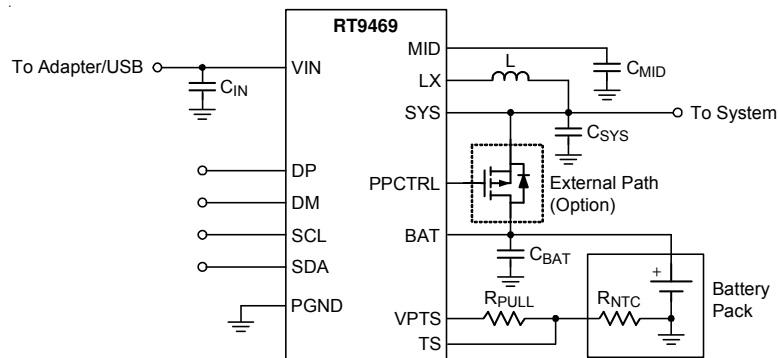
Applications

- Cellular Telephones
- Personal Information Appliances
- Tablet PC, Power Bank
- Portable Instruments

Features

- High Accuracy Voltage/Current Regulation
- Average Input Current Regulation (AICR) : 0.1/0.15/0.5/ to 3A per 0.1A
- Minimum Input Voltage Regulation
 - ▶ For 5V Adapter : 4V/4.25V/4.5V/4.75V
 - ▶ For 9V Adapter : 7V/7.5V/8V/8.5V
- Charge Current Regulation Accuracy : ±5%
- Charge Voltage Regulation Accuracy : ±1% (0 to 85°C)
- Integrated Power MOSFETS for up to 2.275A Charge Rate
- Support USB Charging Detection
- Battery Temperature Sensing
- Synchronous 0.75/1.5MHz Fixed Frequency PWM Controller with Up to 95% Duty Cycle
- Reverse Leakage Protection to Prevent Battery Drainage
- Thermal Regulation and Protection
- Over-Temperature Protection
- Input Over-Voltage Protection
- IRQ Output for Communication with I²C
- Automatic Charging
- RoHS Compliant and Halogen Free

Simplified Application Circuit



Ordering Information

RT9469

Package Type

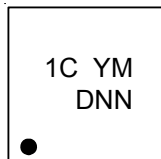
WSC : WL-CSP-25B 2.52x2.52 (BSC)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

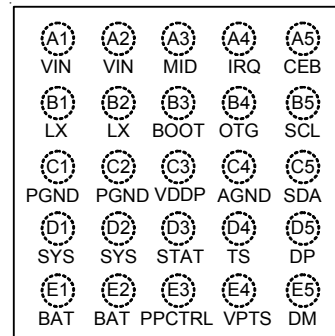


1C : Product Code

YMDNN : Date Code

Pin Configuration

(TOP VIEW)

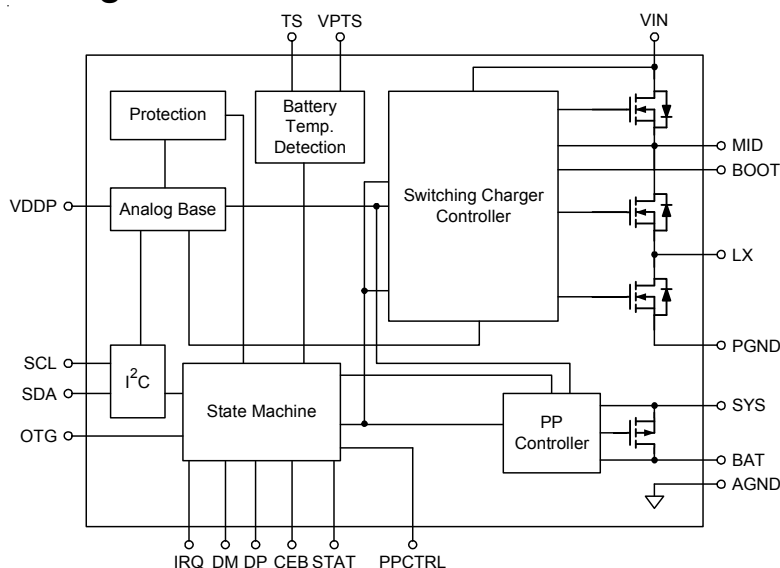


WL-CSP-25B 2.52x2.52 (BSC)

Functional Pin Description

| Pin No. | Pin Name | Pin Description |
|---------|----------|---|
| A1, A2 | VIN | Power input. |
| A3 | MID | Connection point between reverse blocking MOSFET and high-side switching MOSFET. |
| A4 | IRQ | IRQ output node. |
| A5 | CEB | Enable control input. Low active. With internal 102kΩ pull low resistor. |
| B1, B2 | LX | Switch node. Connect to an external inductor. |
| B3 | BOOT | Bootstrap supply for high-side MOSFET. Connect a capacitor between BOOT and LX. |
| B4 | OTG | Setting input pin OTG boost mode. With internal 102kΩ pull low resistor. |
| B5 | SCL | Clock input for I ² C. Open-drain output. Connect a pull-up resistor. |
| C1, C2 | PGND | Power ground for switching charger. |
| C3 | VDDP | Internal power for power stage. |
| C4 | AGND | Analog ground. |
| C5 | SDA | Data input for I ² C. Open drain output. Connect a pull-up Resistor. |
| D1, D2 | SYS | System voltage regulator node. |
| D3 | STAT | Charge status indicator (Open drain). |
| D4 | TS | Battery temperature detection pin. |
| D5 | DP | USB charger type detection pin. |
| E1, E2 | BAT | Charging current output node. Battery charging voltage regulation feedback pin with power Path. |
| E3 | PPCTRL | Power path control pin (Connect to external P-MOSFET gate). |
| E4 | VPTS | Supply voltage for battery temperature detection. |
| E5 | DM | USB charger type detection pin. |

Functional Block Diagram



Operation

The RT9469 is an integrated single cell Li-ion battery switching charger with power path controller.

Base Circuits

Base circuits provide the internal power, VDDP and reference voltage and bias current.

Protection Circuits

The protection circuits include the VINOVP, VINUVLO, BATOVP and OTP circuits. The protection circuits turn off the charging when the input power or die temperature is in abnormal level.

Buck Regulator for charging and Boost Regulator as OTG

The multi-loop controller controls the operation of charging process and current supply to the system. It also controls the circuits as a Boost converter for OTG applications.

Battery Detection

The RT9469 is capable of doing the battery absence detection. The detection protects the charger when battery is removed accidentally.

Adapter Detection

If the poor input power source is connected to the RT9469, the operation is shut down by the adapter detection.

Power Path Management and Control

Once the battery voltage increase to a defined system minimum regulation voltage, the internal path between SYS and BAT will be fully turned on (Cool PPM operation). That is, a better charging efficiency can be derived. When end of charge occurs, the charging stops and the internal path will be off.

USB Charger Detection

The RT9469 detects and distinguishes SONY, APPLE NIKON and USB Charger (Standard Charger Port, Charging Downstream Port and Dedicated Charger Port) via DP and DM pins.

TS Detection

The RT9469 detects the temperature of the battery pack via TS and VPTS pins. The VPTS pin provides a constant voltage source used to drive the voltage divider composed of a pulled-high resistor and a NTC resistor. The RT9469 reports the sensing results via IRQ and status bits for COLD, COOL, WARM and HOT.

I²C Controller

The key parameters of charging and OTG are programmable through I²C commands.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ----- -0.3V to 28V
- MID, BOOT ----- -0.3V to 28V
- LX ----- -0.3V to 20V
- MID – VIN, BOOT – LX ----- -0.3V to 6V
- Other Pins ----- -0.3V to 6V
- Power Dissipation, $P_D @ T_A = 25^\circ\text{C}$
 WL-CSP-25B 2.52x2.52 (BSC) ----- 3.11W
- Package Thermal Resistance (Note 2)
 WL-CSP-25B 2.52x2.52 (BSC), θ_{JA} ----- 32.1°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ----- 4.3V to 9V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN} = 5V$, $V_{BAT} = 4.2V$, $L = 2.2\mu\text{H}$, $C_{IN} = 2.2\mu\text{F}$, $C_{BATS} = 10\mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|----------------|--|-----|------|-----|------|
| Protection | | | | | | |
| V_{IN} OVP Threshold Voltage | | | 10 | 11 | 12 | V |
| V_{IN} OVP Hysteresis | | | -- | 200 | -- | mV |
| Battery OVP | | | 110 | 117 | 124 | % |
| Battery OVP Hysteresis | | | -- | 10 | -- | % |
| Over-Temperature Protection | OTP | | -- | 165 | -- | °C |
| OTP Hysteresis | | | -- | 10 | -- | °C |
| Thermal Regulation Threshold | | Charge current begins to reduce | -- | 120 | -- | °C |
| System UVP Threshold Voltage | V_{SYS_UVP} | | -- | 2.4 | -- | V |
| Sleep Mode Comparator | | | | | | |
| Sleep Mode Entry Threshold $V_{IN} - V_{BATS}$ | V_{SLP} | $2.5V < V_{BATx} < V_{BATREG}$, V_{IN} falling | 0 | 0.04 | 0.1 | V |
| Sleep Mode Exit Hysteresis $V_{IN} - V_{BATS}$ | $V_{SLPEXIT}$ | $2.5V < V_{BATx} < V_{BATREG}$ | 40 | 100 | 200 | mV |
| Sleep Mode Deglitch Time | t_{SLP} | V_{IN} rising above $V_{SLP} + V_{SLPEXIT}$ | -- | 128 | -- | ms |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|--------------------|--|------|-----|-------|------|
| Under-Voltage Lockout Threshold | | | | | | |
| IC Active Threshold Voltage | V _{UVLO} | V _{IN} rising | 3.05 | 3.3 | 3.55 | V |
| IC Active Hysteresis | ΔV _{UVLO} | V _{IN} falling from UVLO | -- | 150 | -- | mV |
| Input Currents | | | | | | |
| VIN Supply Current | I _Q | PWM switching, I _{CHG} = I _{BAT} = 0mA | -- | 10 | -- | mA |
| | | PWM is not switching. I _{CHG} = I _{BAT} = 0mA | -- | -- | 5 | mA |
| | | High impedance mode | -- | -- | 150 | μA |
| Leakage Current from Battery | I _{BAT} | V _{IN} = 0V, charger off. | -- | -- | 25 | μA |
| Input Power Regulation | | | | | | |
| Input Voltage Regulation | V _{MIVR} | I ² C Programmable refer to Reg0x21[3:0] | 4 | -- | 8.5 | V |
| VMIVR Accuracy | | VMIVR = 4.5V | -5 | -- | 5 | % |
| Average Input Current Regulation Accuracy | I _{AICR} | USB charge mode, I _{AICR} = 100mA | 80 | -- | 100 | mA |
| | | USB charge mode, I _{AICR} = 500mA | 400 | -- | 500 | |
| | | USB charge mode, I _{AICR} = 1A | 800 | -- | 1000 | |
| Battery Voltage Regulation | | | | | | |
| Battery Voltage Regulation | V _{OREG} | I ² C programmable per 20mV. | 3.5 | -- | 4.62 | V |
| VBATREG Accuracy | | 0 to 85°C | -1 | -- | 1 | % |
| Re-Charge Threshold | V _{RECH} | V _{BATx} falling, below V _{BATREG} | -- | 125 | -- | mV |
| Re-Charge Deglitch | t _{RECH} | | -- | 128 | -- | ms |
| System Minimum Regulation Voltage | | | | | | |
| System Minimum Regulation Voltage | V _{SYS} | I ² C programmable per 0.1V | 3.5 | -- | 3.8 | V |
| Charging Current Regulation | | | | | | |
| Output Charging Current | I _{CHG} | I ² C programmable per 0.125A | 0.4 | -- | 2.275 | A |
| ICHG Accuracy | | AICR is disabled | -5 | -- | 5 | % |
| Pre-Charge Threshold | V _{PREC} | I ² C programmable per 0.2V | 2 | -- | 3 | V |
| VPREC Accuracy | | | -5 | -- | 5 | % |
| Pre-Charge Current | I _{PREC} | I ² C programmable per 50mA | 100 | -- | 850 | mA |
| IPREC Accuracy | | | -30 | -- | 30 | % |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------------|---------------------|---|------|------|-----|------|
| Charge Termination Detection | | | | | | |
| End of Charge Current | I _{EOC} | I ² C programmable per 50mA | 100 | -- | 450 | mA |
| Fixed IEOC | | As I _{AICR} = 100mA | -- | 50 | -- | mA |
| IEOC Accuracy | | | -100 | -- | 100 | mA |
| Deglitch Time for EOC | t _{EOC} | I _{CHG} < I _{EOC} , V _{BAT} > V _{REC} | -- | 2 | -- | ms |
| PWM | | | | | | |
| High-Side On-Resistance | | From VIN to LX, exclude I _{AICR} = 100mA | -- | 90 | 150 | mΩ |
| Low-Side On-Resistance | | From LX to PGND | -- | 60 | 100 | mΩ |
| Charging Efficiency | | V _{BATx} = 4V, and I _{CHG} = 2.025A | -- | 85 | -- | % |
| Oscillator Frequency | OSC | I ² C programmable 0.75/1.5 MHz | -- | 1.5 | -- | MHz |
| Frequency Accuracy | | | -10 | -- | 10 | % |
| Maximum Duty Cycle | | At minimum voltage input | -- | 95 | -- | % |
| Minimum Duty Cycle | | | 0 | -- | -- | % |
| Peak OCP as Charger Mode | I _{CHGOCP} | | -- | 4.5 | -- | A |
| Power Path On-Resistance | | From SYS to VBAT | -- | 35 | 60 | mΩ |
| Boost Mode Operation | | | | | | |
| Output Voltage Level | V _{OTG} | To VIN | -- | 5.05 | -- | V |
| Output Voltage Accuracy | | | -3 | -- | 3 | % |
| Efficiency | | V _{BATx} = 4V, and I _{IN} = 0.8A, | -- | 85 | -- | % |
| Maximum Output Current | | I ² C programmable, 0.5A/1A | 1 | -- | -- | A |
| Peak Over-Current Protection | | | -- | 4.5 | -- | A |
| VIN OVP as OTG Boost | | | -- | 6 | -- | V |
| VIN OVP Hysteresis | | | -- | 250 | -- | mV |
| Minimum Battery Voltage for Boost | V _{BATMIN} | As boost start-up | -- | 2.9 | -- | V |
| Minimum Battery Voltage Hysteresis | | | -- | 400 | -- | mV |
| I²C Characteristics | | | | | | |
| Output Low Voltage | V _{OL} | I _{DS} = 10mA | -- | -- | 0.4 | V |
| SCL, SDA Input Threshold Voltage | Logic-High | V _{IH} | 1.3 | -- | -- | V |
| | Logic-Low | V _{IL} | -- | -- | 0.4 | |
| SCL Clock | | | -- | -- | 400 | kHz |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|----------------------------------|-----------------------|--|-----|-----|-----|-------|
| DP DM Detection | | | | | | |
| D+ Voltage Source | V _{DP_SCR} | | 0.5 | 0.6 | 0.7 | V |
| D+ Voltage Source Output Current | | | 200 | -- | -- | μA |
| D- Current Sink | I _{DM_SINK} | | 50 | 100 | 150 | μA |
| Input Capacitance | C _i | DM pin, switch open | -- | 4.5 | 5 | pF |
| | | DP pin, switch open | -- | 4.5 | 5 | |
| Input leakage | I _l | DM pin, switch open | -1 | -- | 1 | μA |
| | | DP pin, switch open | -1 | -- | 1 | |
| DP Low Comparator Threshold | V _{DP_LOW} | | 0.8 | -- | -- | V |
| DM High Comparator Threshold | V _{DM_HIGH} | | 0.8 | -- | -- | V |
| DM Low Comparator Threshold | V _{DM_LOW} | | -- | -- | 475 | mV |
| NTC Monitor | | | | | | |
| HOT Threshold | V _{VTS_HOT} | VTS falling, the ratio of VPTS, V _{IN} > V _{IN(MIN)} | 29 | 30 | 31 | %VPTS |
| WARM Threshold | V _{VTS_WARM} | VTS falling, the ratio of VPTS, V _{IN} > V _{IN(MIN)} | 37 | 38 | 39 | %VPTS |
| COOL Threshold | V _{VTS_COOL} | VTS rising, the ratio of VPTS, V _{IN} > V _{IN(MIN)} | 55 | 56 | 57 | %VPTS |
| COLD Threshold | V _{VTS_COLD} | VTS rising, the ratio of VPTS, V _{IN} > V _{IN(MIN)} | 59 | 60 | 61 | %VPTS |
| Low Temperature Hysteresis | ΔV _{VTS} | | -- | 1 | -- | %VPTS |
| Disable Threshold | V _{VTS_OFF} | TS function disable | 2 | 3 | 4 | %VPTS |
| Control I/O Pin | | | | | | |
| Output Low Voltage for STAT | V _{OL} | I _{DS} = 10mA | -- | -- | 0.4 | V |
| CE Input Threshold Voltage | Logic-High | V _{IH} | 1.3 | -- | -- | V |
| | Logic-Low | V _{IL} | -- | -- | 0.4 | |

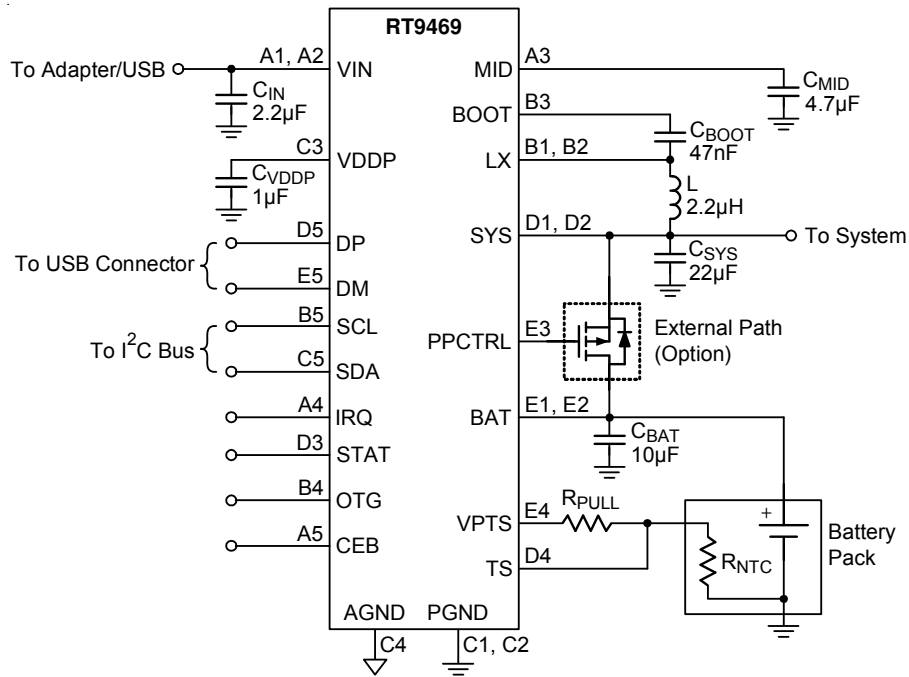
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

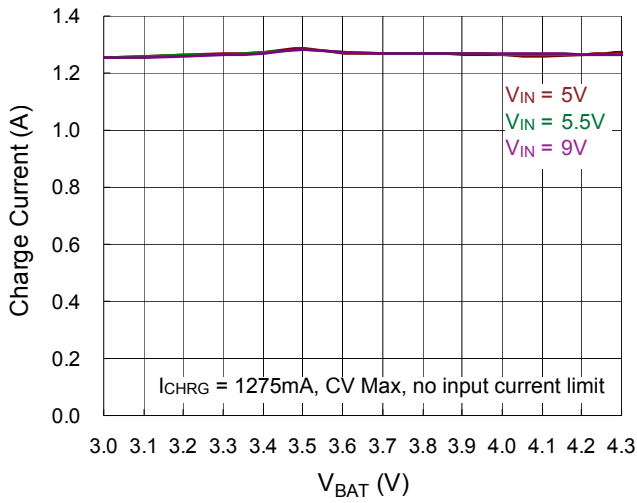
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

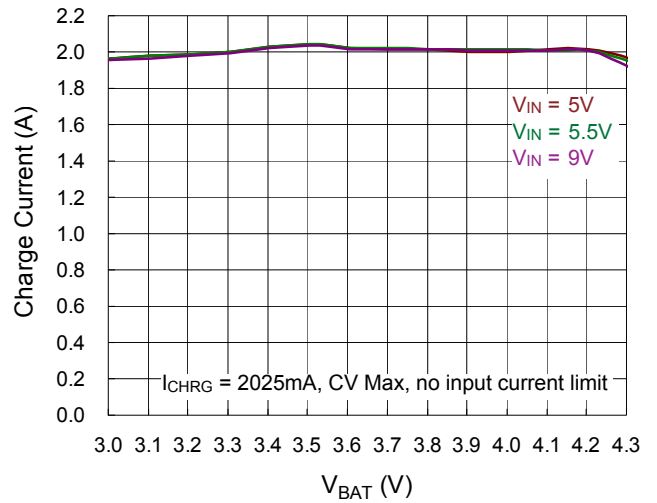


Typical Operating Characteristics

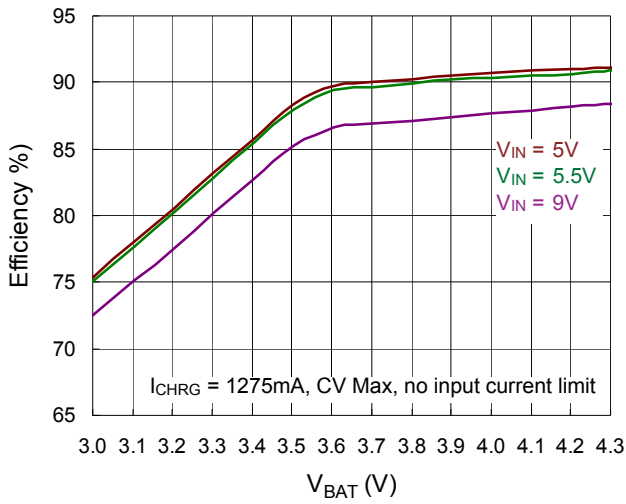
Charge Current vs. V_{BAT}



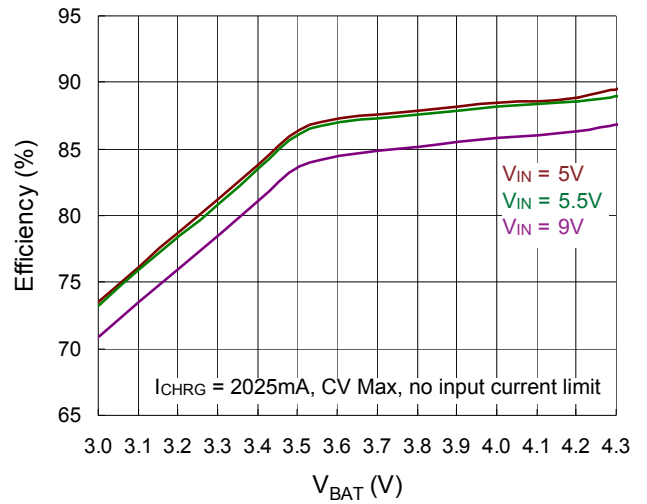
Charge Current vs. V_{BAT}



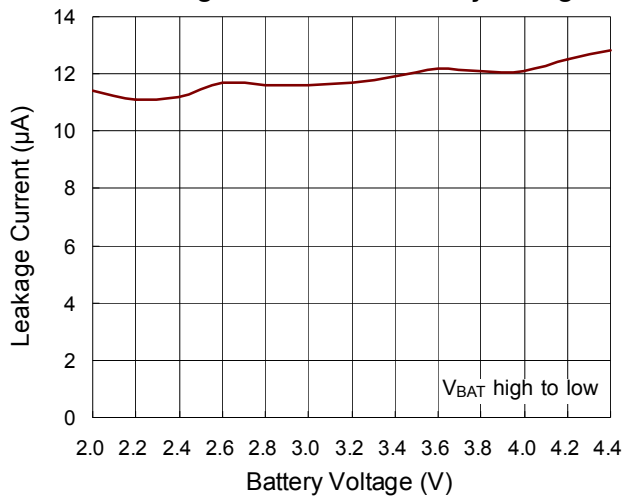
Efficiency vs. V_{BAT}



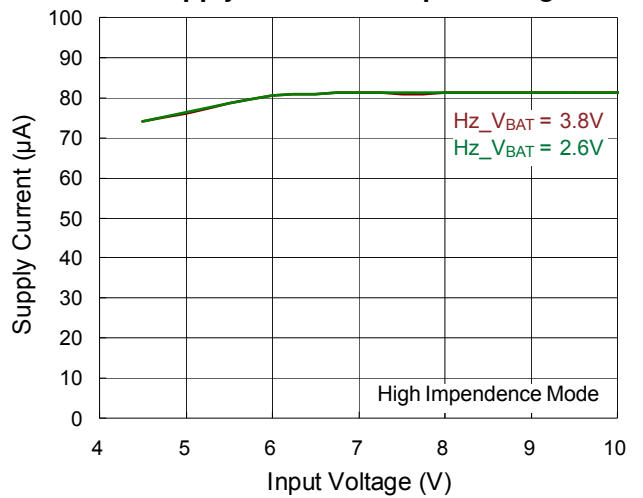
Efficiency vs. V_{BAT}

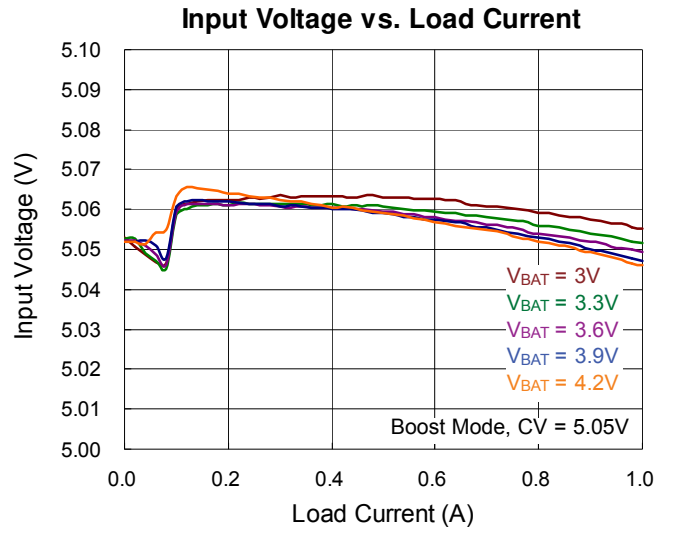
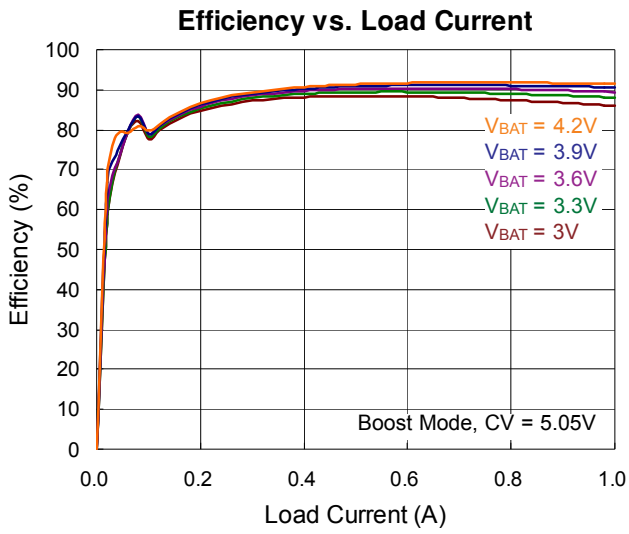


Leakage Current vs. Battery Voltage



Supply Current vs. Input Voltage





Applications Information

The RT9469 switching charger integrates a synchronous PWM controller with power MOSFETs to provide input voltage MIVR (Minimum Input Voltage Regulation), input current AICR (Active Input Current Regulation), high accuracy current and voltage regulation, and charge termination. The charger also features USB OTG (On-The-Go).

The RT9469 has three operation modes : charge mode, boost mode (USB OTG), and high impedance mode. In charge mode, the RT9469 supports a precision charging system for single cell. In boost mode, the RT9469 works as the boost converter and boosts the voltage from battery to VIN pin for sourcing the OTG devices. In high impedance mode, the RT9469 stops charging or boosting and operates in a mode with low current from VIN or battery to reduce the power consumption when the portable device is in standby mode.

Notice that the RT9469 integrate input power source (AC adapter or USB input) detection. Thus, the RT9469 can automatically set the charge current by option. The charge current needs to be set via I²C interface by the host. The RT9469 application mechanism and I²C compatible interface are introduced in later sections.

Charge Mode Operation

Minimum Input Voltage Regulation (MIVR)

The RT9469 features input voltage MIVR function to prevent input voltage drop due to insufficient current provided by the adapter or USB input. If MIVR function is enabled, the input voltage decreases when the over-current of the input power source occurs. VIN is regulated at a predetermined voltage level which can be set as 4V to 8.5V by I²C interface. At this time, the current drawn by the RT9469 equals to the maximum current value that the input power can provide at the predetermined voltage level, instead of the set value.

Charge Profile

The RT9469 provides a precision Li-ion or Li-polymer charging solution for single-cell applications. Input current limit, charge current, termination current, charge voltage

and input voltage MIVR are all programmable via the I²C interface. In charge mode, the RT9469 has five control loops to regulate input current (AICR), charge current, charge voltage, input voltage (MIVR) and device junction temperature. During the charging process, all five loops (if MIVR is enabled) are enabled and the dominant one will take over the control.

For normal charging process, the Li-ion or Li-polymer battery is charged in three charging modes depending on the battery voltage. At the beginning of the charging process, the RT9469 is in pre-charge mode. When the battery voltage rises above pre-charge threshold voltage (V_{PREC}), the RT9469 enters fast-charge mode. Once the battery voltage is close to the regulation voltage (V_{OREG}), the RT9469 enters constant voltage mode.

Pre-Charge Mode

For life-cycle consideration, the battery can not be charged with large current under low battery condition. When the BATS pin voltage is below pre-charge threshold voltage (V_{PREC}), the charger is in pre-charge mode with a weak charge current which equals to the pre-charge current (I_{PREC}). There are two control loops in Pre-charge mode. One is the ICC and the other is the MIN_SYS. If the battery voltage is lower than the SYS voltage, the MOSFET won't fully turn-on to prevent the battery voltage to influence the SYS voltage. It features that the charger can also provide the current to the load from SYS even the battery voltage is too low. In pre-charge mode, the charger basically works as an LDO. The pre-charge current also acts as the current limit when the BATS pin is shorted. The Pre-Charge current levels are 100mA - 850mA programmed by I²C.

Fast-Charge Mode and Settings

As the BAT pin rises above V_{PREC} , the charger enters fast-charge mode and starts charging. Notice that the MUIC integrates input power source (AC adapter or USB input) detection. Thus, the switching charger can set the charge current by option automatically. Unlike the linear charger (LDO), the switching charger (Buck converter) is a current amplifier. The current drawn by the switching

charger is different from the current into the battery.

The user can set the Average Input Current Regulation (AICR) and output charge current (I_{CHRG}) respectively.

Cycle-by-Cycle Current Limit

The charger of the RT9469 has an embedded cycle-by-cycle current limit for inductor. Once the inductor current touches the threshold (4.5A typ.), the charger stops charging immediately to prevent over-current from damaging the device. Notice that, the mechanism can not be disabled by any way.

Average Input Current Regulation (AICR)

The AICR setting is controlled by I²C. The AICR100 mode limits the input current to 100mA. The AICR500 mode limits the input current to 500mA. If the application does not need input current limit, it can be disabled also. The AICR levels programmed by I²C and suitable for USB port and several TA types

Charge Current (I_{CHG})

The charge current into the battery is determined by the power path sensing R_{ON} and ICC setting by I²C. The voltage between the SYS and BAT pins is regulated to the voltage control by ICC setting. ($I_{CC} \times R_{ON}$, R_{ON} : power path R_{ON})

At the RT9469, the R_{ON} is 35m Ω and the Fast-Charge currents is set by the I²C interface from 0.4A to 2.275A per 125mA.

Constant Voltage Mode and Settings

The RT9469 enters constant voltage mode when the BATS voltage is close to the output-charge voltage (V_{OREG}). In this mode, the charge current begins to decrease. For default settings (charge current termination is disabled), the RT9469 does not turn off and always regulates the battery voltage at V_{OREG} . However, once the charge current termination is enabled, the charger terminates if the charge current is below termination current (I_{EOC}) in constant-voltage mode. The charge current termination function is controlled by the I²C interface.

After termination, a new charge cycle restarts when one of the following conditions is detected :

- The BATS pin voltage falls below the $V_{OREG} - V_{RECH}$ threshold.
- VIN Power On Reset (POR).
- CHG_EN bit toggle or RST bit is set (via I²C interface).

Output Charge Voltage (V_{OREG})

The output-charge voltage is set by the I²C interface from 3.5V to 4.62V per 25mV. The default value is 4V (011001).

Termination Current (I_{EOC})

If the charger current termination is enabled (TE bit = "1" of REG0x01[3]), the end-of-charge current is determined by both termination current sense voltage (V_{EOC}) and power path sense resistor (R_{ON}). General R_{ON} is 35m Ω , I_{EOC} is set by the I²C interface from 100mA to 450mA per 50mA.

Input Voltage Protection in Charge Mode

During charge mode, there are two protection mechanisms against if input power source capability is less than the charging current setting. One is AICR and the other is minimum input voltage regulation. A suitable level of AICR can prevent VBUS drop by the insufficient capability. As the AICR setting is not suitable, MIVR will regulate the VBUS in the setting level and sink the maximum current of power source.

Sleep Mode ($V_{IN} - V_{BATS} < V_{SLP}$)

The RT9469 enters sleep mode if the voltage drop between the VIN and BATS pins falls below V_{SLP} . In sleep mode, the reverse blocking switch and PWM are all turned off. This function prevents battery drain during poor or no input power source.

Input Over-Voltage Protection

When VBUS rises above the input over-voltage threshold, the switching charger stops charging and sets the fault status bits. The condition is released when VBUS falls below OVP threshold. The switching charger then resumes charging operation.

Boost Mode Operation (OTG)

Trigger and Operation

The RT9469 features USB OTG support. When OTG function is enabled, the synchronous boost control loop takes over the power MOSFETs and reverses the power flow from the battery to the VIN pin. In normal boost mode, the VIN pin is regulated to the level controlled by VOREG[5:0] from 4.425V to 5.825 per 25mV. The boost provides up to 1A current to support other OTG devices connected to the USB connector.

Output Over-Voltage Protection

In boost mode, the output over-voltage protection is triggered when the VIN voltage is above the output OVP threshold. When OVP occurs, the boost converter stops switching and turns off immediately.

Output Overload Protection

The RT9469 provides an overload protection to prevent the device and battery from damage when VIN is overload. Once overload condition is detected, the reverse blocking switch operates in linear region to limit the output current while the MID voltage remains in voltage regulation. If the overload condition lasts for more than 32ms, the RT9469 will recognize the overload fault condition and resets registers to the default settings.

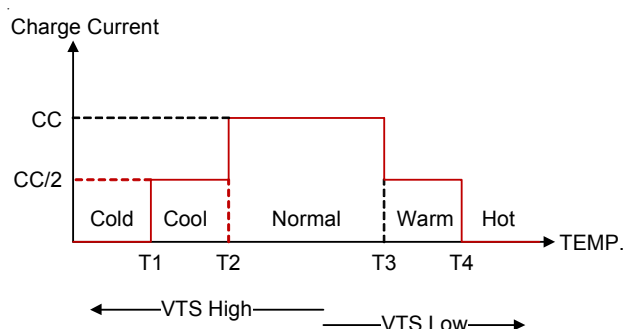
Battery Detection During Normal Charging

The RT9469 provides a battery absent detection scheme to detect insertion or removal of the battery pack. The battery detection scheme is valid only when both TE = 1 and BATD_EN = 1.

During normal charging process, once the charge done condition is satisfied ($V_{BATS} > V_{OREG} - V_{RECH}$ and termination current is detected), the RT9469 turns off the PWM converter and initiates a discharge current (detection current) for a detection time period. After that, the RT9469 checks the BATS voltage. If it is still above the recharge threshold, the battery is present and charge done is detected. If the BATS voltage is below the recharge threshold, the battery is absent. Thus, the RT9469 stops charging and the charge parameters are reset to the default values. The charge resumes after a period of tDET (2sec. typ.).

JEITA Protection

To enhance thermal protection of battery, JEITA function is implemented in the RT9469. JEITA guideline was released in 2007. It includes Warm and cool protection (cool section is between T1 and T2; warm section is between T3 and T4, see the figure as below). When battery's temperature is in warm or cool section, the RT9469 will reduce charging current (by a half of CC mode current). RT9469 stop charging if temperature is lower than T1 or is higher than T4.

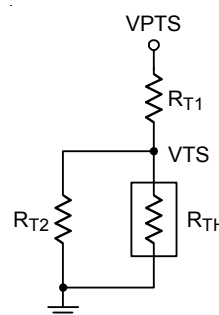


Thermal of battery can be monitored by TS PIN. There are 4 sections should be implemented in JEITA function. Base on R_{hot} and R_{cold} , R_{T1} and R_{T2} can be determined by equation (1) and equation (2).

(R_{hot} mean that system trigger battery OTP, R_{cold} mean that system trigger battery low temperature protection.)

$$R_{T1} = V_{PTS} \times [(1 / V_{T1} - 1 / V_{T4}) / (1 / R_{Cold} - 1 / R_{Hot})] \quad (1)$$

$$R_{T2} = R_{T1} \times [1 / (V_{PTS} / V_{T1} - R_{T1} / R_{Cold} - 1)] \quad (2)$$



Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WL-CSP-25B 2.52x2.52 package, the thermal resistance, θ_{JA} , is 32.1°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (32.1^\circ\text{C}/\text{W}) = 3.11\text{W for a WL-CSP-25B 2.52x2.52 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

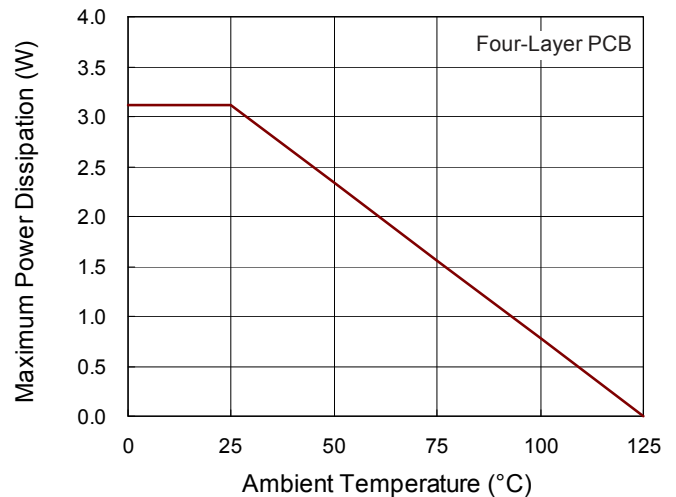


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

- ▶ For AGND noise reduction, PGND and AGND should connect directly at top layer.
- ▶ For AGND noise reduction, PGND and AGND should be connected by ground plane at inner layer1. And this ground plane should be connected to system ground plane by via.
- ▶ VBUS and VMID (capacitor GND) should be connected to IC PGND directly at top layer.
- ▶ The output inductor and bootstrap capacitor should be placed close to the RT9469 and LX pins.

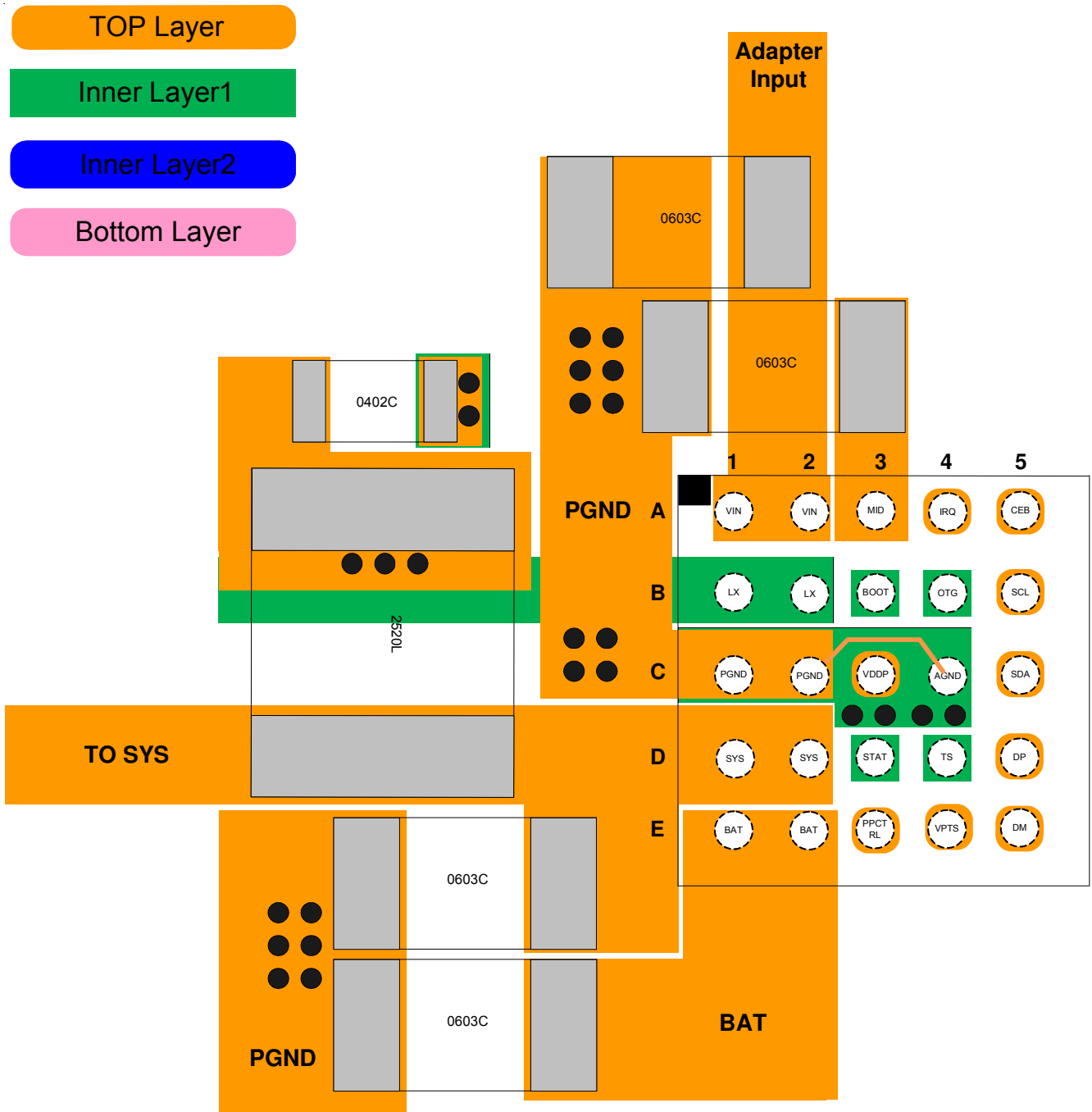


Figure 2. PCB Layout Guide

Control Register (Control)

I²C Slave Address : 0100101

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------------|---------------|----------|--------------|------------|------------|-------------------|----------|------------|
| 0x03 | Device ID | VENDOR_ID | | | | CHIP_REV | | | |
| | Reset Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| 0x00 | Control1 | Sel_SWFreq | EN_STAT | STAT | | BOOST | PWR_Rdy | OTG_PinP | MIVR |
| | Reset Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R | R | R | R | R | R |
| 0x01 | Control2 | IEOC[2:0] | | | Higher_OCP | TE | IIN_INT | HZ | OPA_MODE |
| | Reset Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0x02 | Control3 | VOREG[5:0] | | | | | | OTG_PL | OTG_EN |
| | Reset Value | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0x04 | Control4 | RST | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0x05 | Control5 | SYSUVP_HW_SEL | OTG_OC | SYS_Min[1:0] | | IPREC[3:0] | | | |
| | Reset Value | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0x06 | Control6 | ICHRG[3:0] | | | | EN_OSCSS | VPREC[2:0] | | |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0x07 | Control7 | CC_JEITA | BATD_EN | Chip_EN | CHG_EN | TS_HOT | TS_WARM | TS_COOL | TS_COLD |
| | Reset Value | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0x1C | Control8 | Reserved | Reserved | Reserved | Reserved | Reserved | PPSenseNode [2:0] | | |
| | Reset Value | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0x08 | IRQ1 | TSDI | VINOVP | WakeUpI | WatchDogI | Reserved | CHTERM_TMRI | SYSUVP | BATAB |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| 0x09 | IRQ2 | CHRVPI | CHBADI | CHBATОВI | CHTERMI | CHRCHGI | CHTMRI | CHTREGI | SYSWAKEUPI |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|---------|--------------|----------------|--------------|-------------------|----------------|---------------|--------------|-----------|------------|--|
| 0x0A | IRQ3 | BSTVINOV | BSTOLI | BSTLOWV | Reserved | Reserved | Reserved | Reserved | Reserved | |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Read/Write | R | R | R | R | R | R | R | R | |
| 0x0B | Mask 1 | TSDIM | VINOVPIM | WakeUpIM | WatchDogIM | Reserved | CHTERM_TMRIM | SYSUVPIM | BATABM | |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| 0x0C | Mask 2 | CHRVPI | CHBADIM | CHBATOVIM | CHTERMIM | CHRCHGIM | CHTMRIM | CHTREGIM | SYSWAKEUPI | |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| 0x0D | Mask 3 | BSTVINOVIM | BSTOLIM | BSTLOWVIM | Reserved | Reserved | Reserved | Reserved | Reserved | |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| 0x0E | Control-DPDM | CHG_TYP[2:0] | | | IINLMTSEL[1:0] | | CHG_2DET | CHG_1DET | CHGRUN | |
| | Reset Value | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | |
| | Read/Write | R | R | R | R/W | R/W | R/W | R/W | R | |
| 0x21 | Control 9 | Reserved | PPC_CTRL_SEL | EN_PPCTRL | MIVR_ENB | MIVR_LVL[3:0] | | | | |
| | Reset Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| 0x22 | Control 10 | CLR_DP | DP_STAT | WT_FC[2:0] | | | WT_PRC[1:0] | | TMR_Pause | |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Read/Write | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | |
| 0x23 | Control 11 | AICR[4:0] | | | | | Reserved | | | |
| | Reset Value | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| 0x24 | Control 12 | EOC_Timer[1:0] | | WakeUp_Timer[2:0] | | | WK_Timer_EN | IRQ_Pulse | IRQ_REZ | |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| 0x25 | Control 13 | WDT_EN | Reserved | Reserved | TWDTRST | Reserved | Reserved | TWDT[1:0] | | |
| | Reset Value | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|---------------|---------|----------|----------|-----------|-----------|--------|----------|----------|
| 0x26 | STAT IRQ | TSHOTI | TSWARMI | TSCOOI | TSCOLDI | PWR_Rdyl | MIVRI | Reserved | Reserved |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0x27 | STAT IRQ Mask | TSHOTIM | TSWARMIM | TSCOOI M | TSCOLDI M | PWR_RdyIM | MIVRIM | Reserved | Reserved |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------|-------------|--|---------|------|------------|-------|---------|----------|----------|
| 0x00 | Control 1 | Sel_SWFreq | EN_STAT | STAT | | BOOST | PWR_Rdy | OTG_PinP | MIVR |
| | Reset Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R | R | R | R | R | R |
| Sel_SWFreq | | The switching frequency selection bit (Charger/OTG) 0 : The switching frequency is 1.5MHz 1 : The switching frequency is 750kHz | | | | | | | |
| EN_STAT | | 0 : Disable STAT pin function 1 : Enable STAT pin function | | | | | | | |
| STAT | | Charger status bit 00 : Ready 01 : Charge in progress 10 : Charge done 11 : Fault | | | | | | | |
| BOOST | | 0 : Not in boost mode 1 : Boost mode | | | | | | | |
| PWR_Rdy | | Power status bit 0 : Input power is bad, VIN > VOVP or VIN < VUVLO or VIN < BATS + VSLP 1 : Input power is good, UVLO < VIN < VOVP & VIN > BATS + VSLP | | | | | | | |
| OTG_PinP | | OTG pin polarity 0 : OTG input pin is low 1 : OTG input pin is high | | | | | | | |
| MIVR | | MIVR status pin : 0 : MIVR regulation is inactive 1 : MIVR regulation is active | | | | | | | |
| 0x01 | Control 2 | IEOC[2:0] | | | Higher_OCP | TE | IIN_INT | HZ | OPA_MODE |
| | Reset Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| IEOC | | EOC current level setting 000 : 100mA 001 : 150mA 010 : 200mA 011 : 250mA 100 : 300mA 101 : 350mA 110 : 400mA 111 : 450mA | | | | | | | |
| Higher_OCP | | Charger/OTG OCP level selection 0 : OCP = 4.5A 1 : OCP = 6A | | | | | | | |
| TE | | Charge current termination detection and IRQ control 0 : Disable charge current termination 1 : Enable charge current termination | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------------|--|------|------|------|------|------|--------|--------|
| | IIN_INT | IAICR setting bit 0 : Decided by external OTG pin, 500mA current limit when OTG pin is low and 1A current limit when OTG pin is high 1 : Decided by I ² C IAICR[4:0] and DPDM results, refer to REG0x0E | | | | | | | |
| | HZ | 0 : Not high impedance mode 1 : High impedance mode | | | | | | | |
| | OPA_MODE | 0 : Charger mode 1 : Boost mode | | | | | | | |
| 0x02 | Control 3 | VOREG[5:0] | | | | | | OTG_PL | OTG_EN |
| | Reset Value | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | VOREG[5:0] | Battery regulation voltage / Boost output voltage. 00 0000 : 3.50V / 4.425V 00 0001 : 3.52V / 4.45V 00 0010 : 3.54V / 4.475V 01 1000 : 3.98V / 5.025 V 01 1001 : 4.00V / 5.05V 01 1010 : 4.02 / 5.075V 10 0111 : 4.28V / 5.4V 10 1000 : 4.30V / 5.425V 10 1001 : 4.32V / 5.45V 10 1110 : 4.42V / 5.575V 10 1111 : 4.44V / 5.6V 11 0110 : 4.58V / 5.775V 11 0111 : 4.60V / 5.8V 11 1000 : 4.62V / 5.825V 11 1111 : 4.62V / 5.825V | | | | | | | |
| | OTG_PL | 0 : Active at low level 1 : Active at High level | | | | | | | |
| | OTG_EN | 0 : Disable OTG Pin 1 : Enable OTG Pin | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------------|-------------|--|----------|--------------|----------|------------|----------|----------|----------|
| 0x03 | Device ID | VENDOR_ID | | | | CHIP_REV | | | |
| | Reset Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| VENDOR_ID | | Vendor Identification : Richtek : 0100b | | | | | | | |
| CHIP_REV | | Chip Revision | | | | | | | |
| 0x04 | Control 4 | RST | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RST | | Write : 1-Charger in reset mode, 0-No effect, Read : always get "0" | | | | | | | |
| 0x05 | Control 5 | SYSUVP_HW_SEL | OTG_OC | SYS_Min[1:0] | | IPREC[3:0] | | | |
| | Reset Value | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| SYSUVP_HW_SEL | | System UV protection selection bit 0 : Switching is not turned off when System UVP 1 : Switching is turned off when System UVP | | | | | | | |
| OTG_OC | | Over-current protection threshold 0 : 0.5A 1 : 1A | | | | | | | |
| SYS_Min[1:0] | | System minimum regulation voltage 00 : 3.5V 01 : 3.6V 10 : 3.7V 11 : 3.8V | | | | | | | |
| IPREC[3:0] | | 0000 : 100mA 0001 : 150mA 0010 : 200mA 0011 : 250mA 0100 : 300mA 0101 : 350mA 0110 : 400mA 0111 : 450mA 1000 : 500mA 1001 : 550mA 1010 : 600mA 1011 : 650mA 1100 : 700mA 1101 : 750mA 1110 : 800mA 1111 : 850mA | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------------|---|---------|---------|--------|----------|------------|---------|---------|
| 0x06 | Control 6 | ICHRG[3:0] | | | | EN_OSCSS | VPREC[2:0] | | |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | ICHRG[3:0] | Charging current setting (Recommended to set REG0x1C [2:0] = 111) 0000 : 0.4A 0001 : 0.525A 0010 : 0.65A 0110 : 1.15A 1010 : 1.65A 1110 : 2.15A 1111 : 2.275A | | | | | | | |
| | EN_OSCSS | Enable signal of oscillator spread spectrum 0 : Disable spread spectrum 1 : Enable spread spectrum | | | | | | | |
| | VPREC[2:0] | Pre-Charge voltage threshold 000 : 2V 001 : 2.2V 010 : 2.4V 011 : 2.6V 100 : 2.8V 101 : 3.0V 111 : 3.0V | | | | | | | |
| 0x07 | Control 7 | CC_JEITA | BATD_EN | CHIP_EN | CHG_EN | TS_HOT | TS_WARM | TS_COOL | TS_COLD |
| | Reset Value | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R | R | R | R |
| | CC_JEITA | Charging current setting bit 0 : ICHRG 1 : ICHRG/2 | | | | | | | |
| | BATD_EN | Battery detection when charge done 0 : Disable battery detection 1 : Enable battery detection | | | | | | | |
| | CHIP_EN | Chip enable bit 0 : Chip is disabled 1 : Chip is enabled | | | | | | | |
| | CHG_EN | Charger enable bit : 0 : Charger is disabled 1 : Charger is enabled | | | | | | | |
| | TS_HOIT | Temperature status read bit 0 : Normal temperature 1 : Temperature is hot | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------------------|--|----------|----------|-----------|----------|-------------------|---------|--------|
| | TS_WARM | Temperature status read bit 0 : Normal temperature 1 : Temperature is warm | | | | | | | |
| | TS_COOL | Temperature status read bit 0 : Normal temperature 1 : Temperature is cool | | | | | | | |
| | TS_COLD | Temperature status read bit 0 : Normal temperature 1 : Temperature is cold | | | | | | | |
| 0x1C | Control 8 | Reserved | Reserved | Reserved | Reserved | Reserved | PPSenseNode [2:0] | | |
| | Reset Value | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | PPSenseNode [2:0] | Power path current sensing adjustment 100 : default setting 111 : recommended setting | | | | | | | |
| 0x08 | IRQ 1 | TSDI | VINOVPI | WakeUpI | WatchDogI | Reserved | CHTERM_TMRI | SYSUVPI | BATABI |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| | TSDI | Thermal shutdown fault. Set if the die temperature exceeds the thermal shutdown threshold | | | | | | | |
| | VINOVPI | VIN over-voltage protection 0 : Normal 1 : VINOVP is detected | | | | | | | |
| | WakeUpI | WakeUp timer fault 0 : Normal 1 : WakeUp timer is expired | | | | | | | |
| | WatchDogI | WatchDog timer fault 0 : Normal 1 : WatchDog timer is expired | | | | | | | |
| | CHTERM_TMRI | EOC timer fault 0 : Normal 1 : EOC timer is expired | | | | | | | |
| | SYSUVPI | System UVP fault 0 : Normal 1 : SYSUVP is triggered | | | | | | | |
| | BATABI | Battery absence fault bit 0 : Normal 1 : Battery absence | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------------|-------------|---|----------|----------|------------|----------|--------------|----------|------------|
| 0x09 | IRQ 2 | CHRVPI | CHBADI | CHBATOVI | CHTERMI | CHRCHGI | CHTMRI | CHTREGI | SYSWAKEUPI |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| CHRVPI | | Charger fault. Reverse protection (VIN < BATS + VSLP) | | | | | | | |
| CHBADI | | Charger fault. Bad adapter (Poor Input source or VIN < VUVLO) | | | | | | | |
| CHBATOVI | | Charger fault. Battery OVP | | | | | | | |
| CHTERMI | | Charge terminated | | | | | | | |
| CHRCHGI | | Recharge request (VBATS < VOREG – VRECH) | | | | | | | |
| CHTMRI | | Charger fault. Timer time-out | | | | | | | |
| CHTREGI | | Charger warning. Thermal regulation loop active | | | | | | | |
| SYSWAKEUPI | | Battery voltage is high enough to wakeup system | | | | | | | |
| 0x0A | IRQ 3 | BSTVINOVI | BSTOLI | BSTLOWVI | Reserved | Reserved | Reserved | Reserved | Reserved |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| BSTVINOVI | | Boost fault. VIN OVP (VIN > VIN_BOVP) | | | | | | | |
| BSTOLI | | Boost fault. Over load | | | | | | | |
| BSTLOWVI | | Boost fault. Battery voltage is too low | | | | | | | |
| 0x0B | Mask 1 | TSDIM | VINOVPIM | WakeUpIM | WatchDogIM | Reserved | CHTERM_TMRIM | SYSUVPIM | BATABIM |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| TSDIM | | TSDI fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| VINOVPIM | | VIN OVP fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| WakeUpIM | | WakeUp timer interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| WatchDogIM | | WatchDog timer interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHTERM_TMRIM | | EOC timer interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-------------|---|-------------|---------------|--------------|--------------|-------------|--------------|-----------------|
| | SYSUVPIM | System UVP fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| | BATABIM | Battery absence fault interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| 0x0C | Mask 2 | CHRV IM | CHBAD IM | CHBATO VIM | CHTERM IM | CHRCH GIM | CHTMRI M | CHTREG IM | SYSWAK EUPIM |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| | CHRVIM | Charger reverse protection interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| | CHBADIM | Charger Bad adapter interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| | CHBATOVIM | Charger battery over-voltage interrupt mask 0 : Interrupt is not masked, 1 : Interrupt is masked | | | | | | | |
| | CHTERMIM | Charge terminated interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| | CHRCHGIM | Charger recharge request interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| | CHTMRIM | Charger timer timeout interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| | CHTREGIM | Charger thermal regulation loop active interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| | SYSWAKEUPIM | System wakeup interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------|--------------|--|-------------|---------------|----------------|----------|----------|----------|----------|
| 0x0D | Mask 3 | BSTVINO VIM | BSTOLI M | BSTLOW VIM | Reserved | Reserved | Reserved | Reserved | Reserved |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| BSTVINOVIM | | Boost VIN overvoltage interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| BSTOLIM | | Boost over load interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| BSTLOWVIM | | Boost low battery voltage interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| 0x0E | Control DPDM | CHG_TYP[2:0] | | | IINLMTSEL[1:0] | | CHG_2DET | CHG_1DET | CHGRUN |
| | Reset Value | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| | Read/Write | R | R | R | R/W | R/W | R/W | R/W | R |
| CHG_TYP[2:0] | | Charger type indication 000 : Standard USB Charger (SDP) 001 : Sony Charger -1 010 : Sony Charger -2 011 : Apple Charger (0.5A) 100 : Apple Charger (1A) 101 : Nikon Charger (1A) 110 : Charging Downstream Port (CDP) (High Current Host/Hub) 111 : Dedicated Charger (DCP) | | | | | | | |
| IINLMTSEL[1:0] | | Input current limit selection bit 00 : CHG_TYP[2:0] is applied and ignore IAICR[4:0] 01 : IAICR[4:0] is applied and ignore CHG_TYP[2:0] 10 : Input limit is set to the higher level of IAICR[4:0] and CHG_TYP[2:0] results 11 : Input limit is set to the lower level of IAICR[4:0] and CHG_TYP[2:0] results | | | | | | | |
| CHG_2DET | | The CHG_2DET bit is used to enable the secondary charger detection (to distinguish CDP and DCP). Set this bit to 1 in order to enable charger detection. 0 : Secondary Charger Detection is disabled 1 : Secondary Charger Detection is enabled | | | | | | | |
| CHG_1DET | | The CHG_1DET bit is used to enable the primary charger detection and auto-detect charger type when VIN plug in. Toggle this bit value (set to 0 and then set 1) to re-enable charger detection. 0 : Primary Charger Detection is disabled 1 : Primary Charger Detection is enabled | | | | | | | |
| CHGRUN | | The CHGRUN bit is the charger detector status bit. It means the charger detection is running or not. 0 : Charger Detection is not running 1 : Charger Detection is running | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------------|-------------|---|--------------|-----------|----------|---------------|------|------|------|
| 0x21 | Control 9 | Reserved | PPC_CTRL_SEL | EN_PPCTRL | MIVR_ENB | MIVR_LVL[3:0] | | | |
| | Reset Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| PPC_CTRL_SEL | | Pin-PPCTRL control by Software (SW) or Hardware (HW) 0 : Controlled by SW 1 : Controlled by HW | | | | | | | |
| EN_PPCTRL | | External power-path control signal. It works when PPC_CTRL_SEL = 0 0 : PPCTRL pin Internally pulled high to VSYS 1 : PPCTRL pin Internally pulled low to PGND | | | | | | | |
| MIVR_ENB | | Control the MIVR regulation 0 : MIVR regulation is enabled 1 : MIVR regulation is disabled | | | | | | | |
| MIVR_LVL[3:0] | | Control the MIVR regulation level 0000 : 4.0V 0001 : 4.25V 0010 : 4.5V 0011 : 4.75V 0100 : 7.0V 0101 : 7.5V 0110 : 8.0V 0111 : 8.5V | | | | | | | |

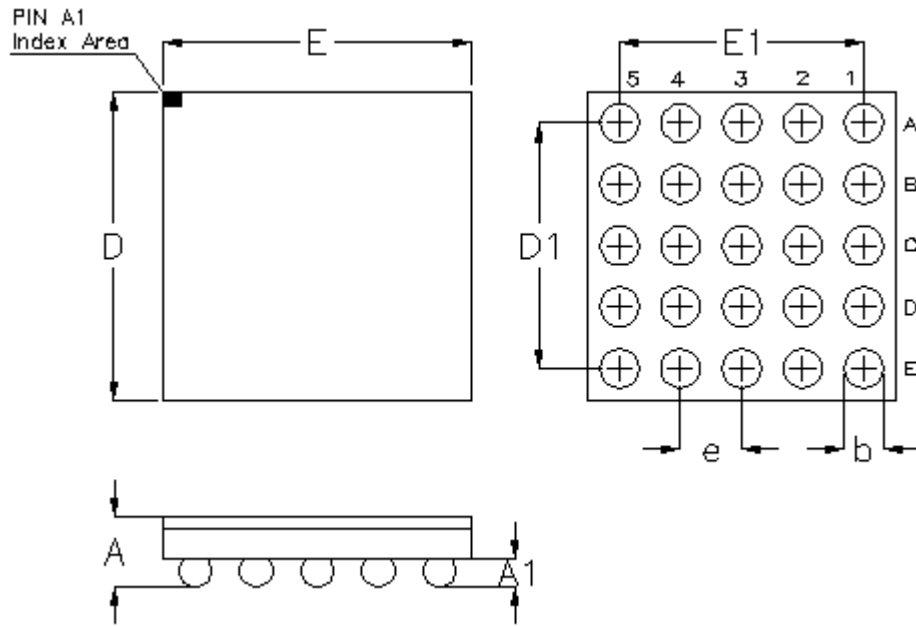
| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------|-------------|---|---------|------------|------|------|-------------|------|-----------|
| 0x22 | Control 10 | CLR_DP | DP_STAT | WT_FC[2:0] | | | WT_PRC[1:0] | | TMR_Pause |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W |
| CLR_DP | | Clear DP pin of 0.6V voltage source 0 : Don't care 1 : Release DP pin of 0.6V voltage source | | | | | | | |
| DP_STAT | | DP pin status indication 0 : DP pin is pulled to 0.6V 1 : DP pin is released | | | | | | | |
| WT_FC[2:0] | | Fast charge timer 000 : 4hrs 001 : 6hrs 010 : 8hrs 011 : 10hrs 100 : 12hrs 101 : 14hrs 110 : 16hrs 111 : Timer disabled | | | | | | | |
| WT_PRC[1:0] | | Pre charge timer 00 : 30min 01 : 45min 10 : 60min 11 : Timer disabled | | | | | | | |
| TMR_Pause | | Timer control bit 0 : Timer is active 1 : Timer is paused | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|---------|-------------|---|------|------|------|------|----------|------|------|--|
| 0x23 | Control 11 | IAICR[4:0] | | | | | Reserved | | | |
| | Reset Value | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| | IAICR[4:0] | Average Input Current Regulation (AICR) setting 0000X : 100mA 0001X : 150mA 0010X : 500mA 00110 : 600mA 00111 : 700mA 01010 : 1A 01011 : 1.1A 01111 : 1.5A 10100 : 2A 11110 : 3A 11111 : Disable | | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------------------|-------------|--|----------|--------------------|----------|----------|-------------|-----------|---------|
| 0x24 | Control 12 | EOC_Timer[1:0] | | Wake-up Timer[2:0] | | | WK_Timer_EN | IRQ_Pulse | IRQ_REZ |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| EOC_Timer[1:0] | | The timer of back-charging time 00 : 0min 01 : 30min 10 : 45min 11 : 60min | | | | | | | |
| Wake-up Timer[2:0] | | The periodically timer IRQ to awake 000 : 4s 001 : 8s 010 : 16s 011 : 32s 100 : 64s 101 : 2min 110 : 4min 111 : 8min | | | | | | | |
| WK_Timer_EN | | Control the wake-up timer 0 : Timer is disabled 1 : Timer is enabled | | | | | | | |
| IRQ_Pulse | | Control the IRQ remind function 0 : The IRQ reminding is disabled 1 : The IRQ reminding is enabled. If the IRQ is triggered and no check action, it will be released for 2ms and triggered again | | | | | | | |
| IRQ_REZ | | IRQ release control 0 : No action 1 : Release IRQ pin status. It is auto reset to 0 when release is done | | | | | | | |
| 0x25 | Control 13 | WDT_EN | Reserved | Reserved | TWD_TRST | Reserved | Reserved | TWDT[1:0] | |
| | Reset Value | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| WDT_EN | | Control watch dog timer 0 : Disable timer and reset 1 : Enable timer | | | | | | | |
| TWDTRST | | Waiting timer to reset I ² C setup after watchdog is asserted 0 : 200ms 1 : 500ms | | | | | | | |
| TWDT[1:0] | | Watch dog timer, from WDTEN is enabled to watchdog IRQ 00 : 1s 01 : 2s 10 : 4s 11 : 8s | | | | | | | |

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------------|-------------|--|--------------|--------------|--------------|---------------|--------|----------|----------|
| 0x26 | STAT IRQ | TSHOTI | TSWARMI | TSCOO LI | TSCOL DI | PWR_ Rdyl | MIVRI | Reserved | Reserved |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R | R | R | R | R | R | R | R |
| TSHOTI | | Status IRQ : Interrupt is triggered when TS is entering or exiting HOT region | | | | | | | |
| TSWARMI | | Status IRQ : Interrupt is triggered when TS is entering or exiting WARM region | | | | | | | |
| TSCOO LI | | Status IRQ : Interrupt is triggered when TS is entering or exiting COOL region | | | | | | | |
| TSCOL DI | | Status IRQ : Interrupt is triggered when TS is entering or exiting COLD region | | | | | | | |
| PWR_ Rdyl | | Status IRQ : Interrupt is triggered when PWR_Rdy is from bad to good or from good to bad | | | | | | | |
| MIVRI | | Status IRQ : Interrupt is triggered when MIVR loop is from inactive to activate or from active to inactive | | | | | | | |
| 0x27 | STAT Mask | TSHOTIM | TSWARM IM | TSCOO LIM | TSCOL DIM | PWR_ RdyIM | MIVRIM | Reserved | Reserved |
| | Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| TSHOTIM | | TS in HOT interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| TSWARMIM | | TS in WARM interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| TSCOO LIM | | TS in COOL interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| TSCOL DIM | | TS in COLD interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| PWR_ RdyIM | | PWR_Rdy interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| MIVRIM | | MIVR interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |

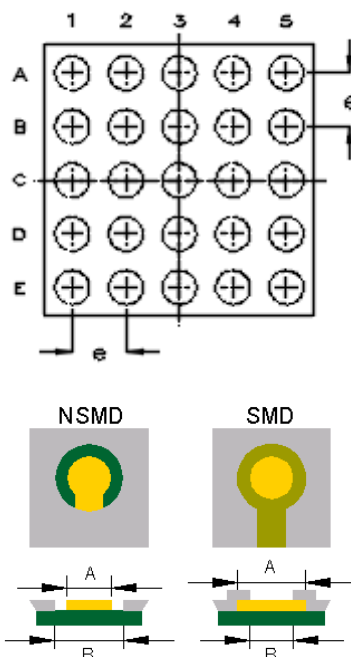
Outline Dimension



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.525 | 0.625 | 0.021 | 0.025 |
| A1 | 0.200 | 0.260 | 0.008 | 0.010 |
| b | 0.290 | 0.350 | 0.011 | 0.014 |
| D | 2.470 | 2.570 | 0.097 | 0.101 |
| D1 | 2.000 | | 0.079 | |
| E | 2.470 | 2.570 | 0.097 | 0.101 |
| E1 | 2.000 | | 0.079 | |
| e | 0.500 | | 0.020 | |

25B WL-CSP 2.52x2.52 Package (BSC)

Footprint Information



| Package | Number of Pin | Type | Footprint Dimension (mm) | | | Tolerance |
|-------------------------|---------------|------|--------------------------|-------|-------|-----------|
| | | | e | A | B | |
| WL-CSP2.52*2.52-25(BSC) | 25 | NSMD | 0.500 | 0.275 | 0.375 | ±0.025 |
| | | SMD | | 0.375 | 0.275 | |

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