High Speed CMOS 16-Bit Bus Register Transceiver (3-State)

QS74FCT16952T
QS74FCT162952T

FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <1 µW typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5 ns $t_{SK(O)}$
- Flow-through pinout for easy layout
- Power off disable allows hot plugging
- Extended commercial temperature: –40°C to +85°C
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise

FCT16952T

- High drive standard FCT-T outputs: I_{OL} = +64 mA, I_{OH} = –32 mA
- Incident switching for driving buses and large loads

FCT162952T

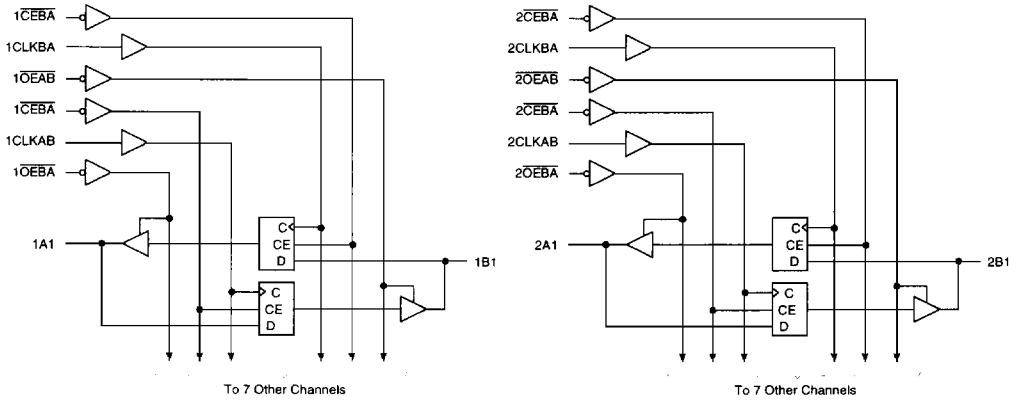
- Balanced output drivers: ±24 mA
- Reduced switching noise for point to point signals

4

DESCRIPTION

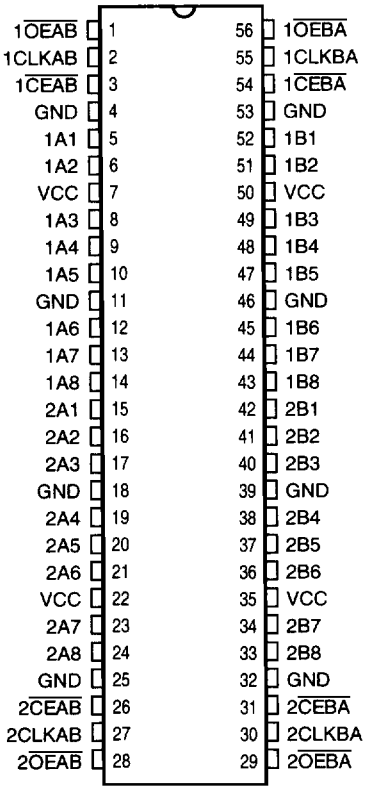
The FCT16952 family of products are 16-bit bus register transceivers with three-state outputs that are ideal for driving address and data buses. Two independent 8-bit registered transeivers are used to permit independent control of data flow in either direction. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01) and many power and ground pins provide low ground bounce. To accommodate hot-plug or live insertion applications, both versions of this product were designed not to load an active bus when Vcc is removed. In applications where bus signals are point-to-point or driving light capacitance loads, the balanced drive FCT162952 is recommended.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
(All Pins Top View)

SSOP, TSSOP



PIN DESCRIPTION

Name	Description
x$\overline{OEAB}$	A to B Output Enable Inputs (Active LOW)
x$\overline{OEBA}$	B to A Output Enable Inputs (Active LOW)
x$\overline{CEAB}$	A to B Enable Inputs (Active LOW)
x$\overline{CEBA}$	B to A Enable Inputs (Active LOW)
x$\overline{CLKAB}$	A to B Clock Inputs
x$\overline{CLKBA}$	B to A Clock Inputs
xAx	A to B Data Inputs or B to A 3 State Outputs
xBx	B to A Data Inputs or A to B 3 State Outputs