User's Guide

DP83561EVM User's Guide

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ABSTRACT

This User's Guide discusses how to properly operate and configure the DP83561EVM. For best layout practices, schematic files, and Bill of Materials, see the associated sections and support documents.

DP83561EVM consists of a main PCB and two breakout boards: DP83561-SP Ethernet board, MAC interface breakout board, and MAC interface back-to-back connector.

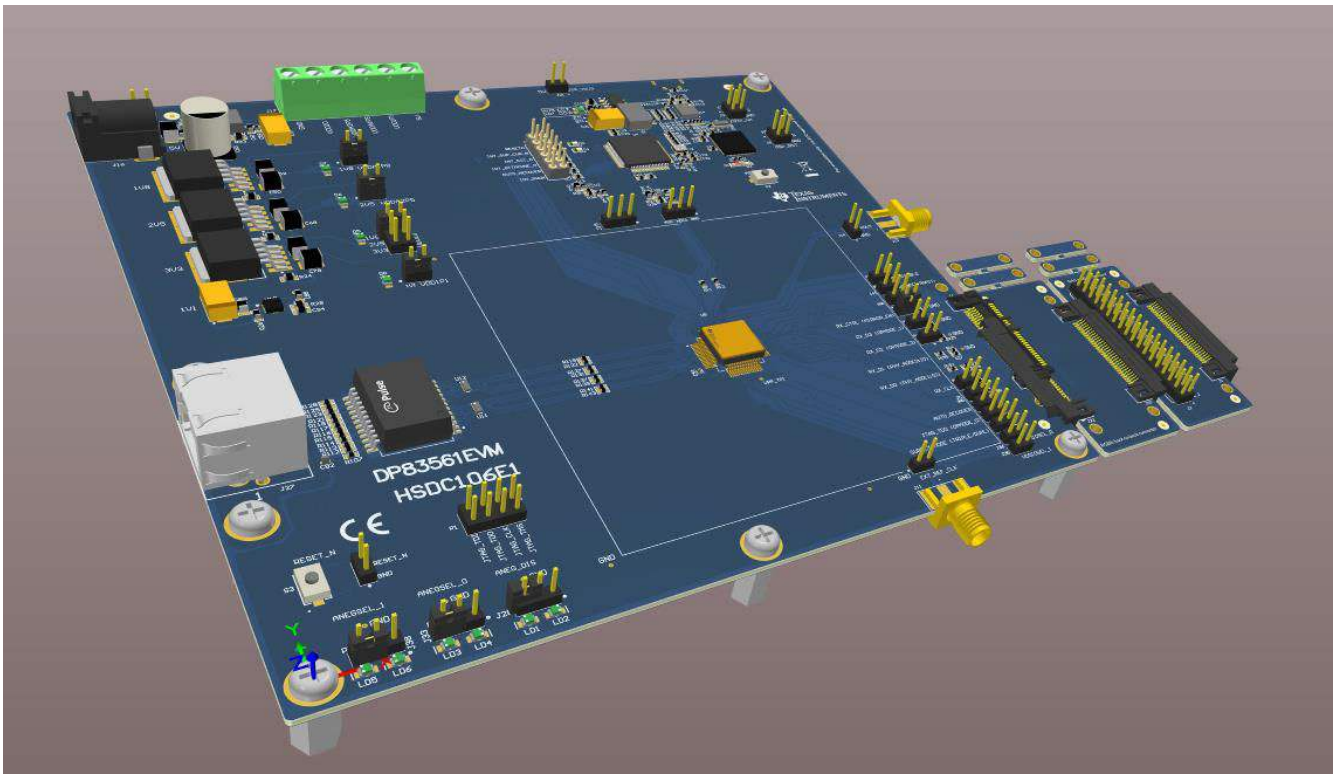

Figure 1-1. DP83561EVM Main PCB and Two Breakout Boards

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1 Definitions

Table 1-1. Terminology

ACRONYM	DEFINITION
PHY	Physical Layer Transceiver
MAC	Media Access Controller
SMI	Serial Management Interface
MDIO	Management Data I/O
MDC	Management Data Clock
RGMII	Reduced Gigabit Media Independent Interface
MII	Media Independent Interface
SFD	Start-of-Frame Detection
VDDA	Analog Core Supply Rail
VDDIO	Digital Supply Rail
PD	Pulldown
PU	Pullup
MC	Microcontroller
AFE	Analog Front End
SEFI	Single Event Functional Interrupt

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2 Introduction

The DP83561-SP is a radiation hardened, high reliability gigabit Ethernet PHY designed for hostile environments like those found in space, avionics, or downhill drilling. The DP83561-SP is a low power, fully featured Physical Layer transceiver with integrated PMD sub-layers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols.

The DP83561EVM is a tool used to highlight the features of the DP83561-SP Ethernet PHY. Breakout connectors are included to allow MAC access and back-to-back configuration support. The EVM also provides on-board tools to configure PHY registers using a USB-MDIO graphical user interface tool. The EVM can be powered by a single Wide-Vin 5V-36V power supply or through a microUSB cable.

Note

The DP83561EVM uses DP83561-SP Engineering Module (EM) parts. EM parts do not ensure radiation performance. They are suitable for prototyping but not suitable for production.

2.1 DP83561EVM Key Features

- Space Grade DP83561-SP is IEEE802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T compliant
- RGMII/MII MAC interfaces
- BER testing via back-to-back configuration or loopback modes
- Compliance testing support
- SEFI monitoring
  - PCS State machine monitor
  - ECC monitor
  - Supply current monitor
  - Temperature monitor
  - Auto-recovery option
- Onboard MSP support to configure PHY over MDIO/MDC
  - USB-2-MDIO support
- Status LEDs
  - Link
  - Power supplies
  - SMI command
- Variable I/O Voltage Range: 1.8-V, 2.5-V, and 3.3-V
- Bootstraps for hardware configuration

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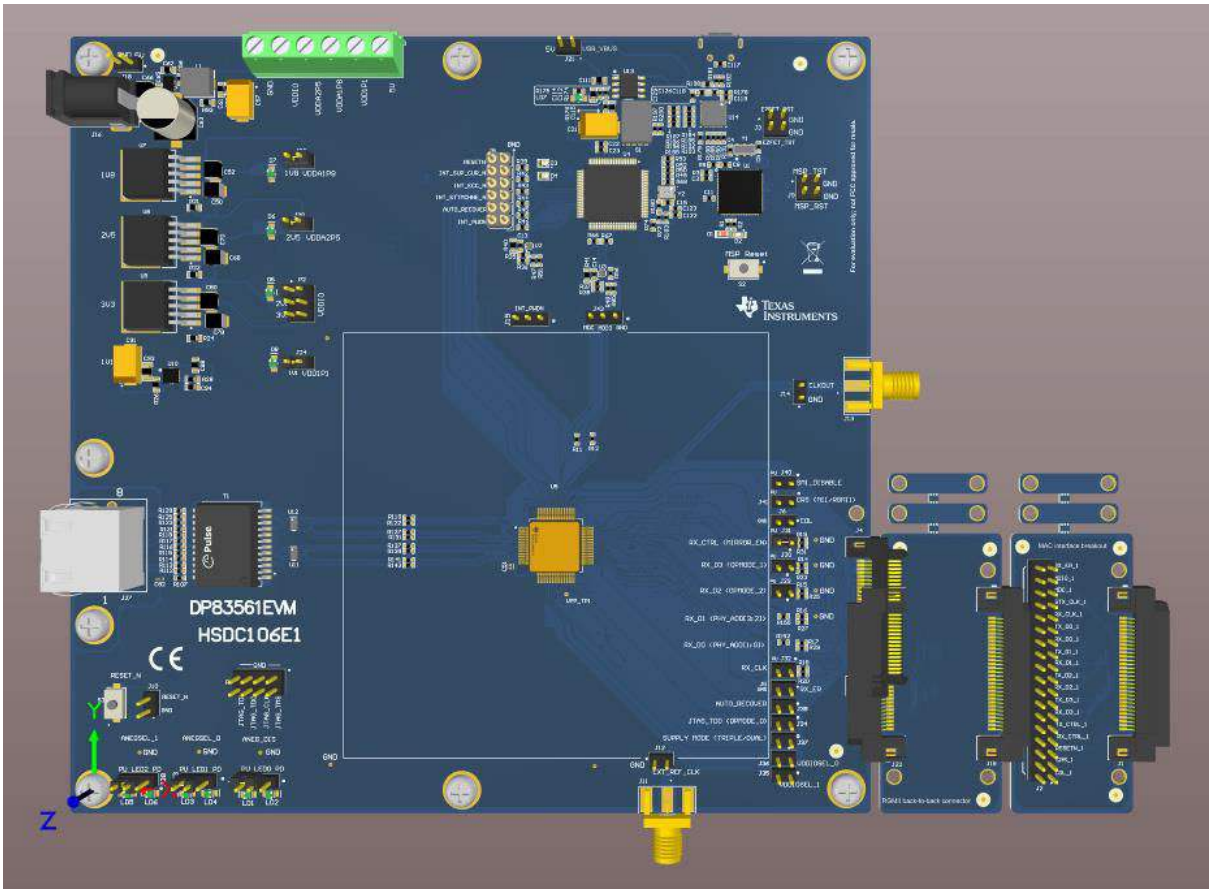

Figure 2-1. DP83561EVM – Top Side

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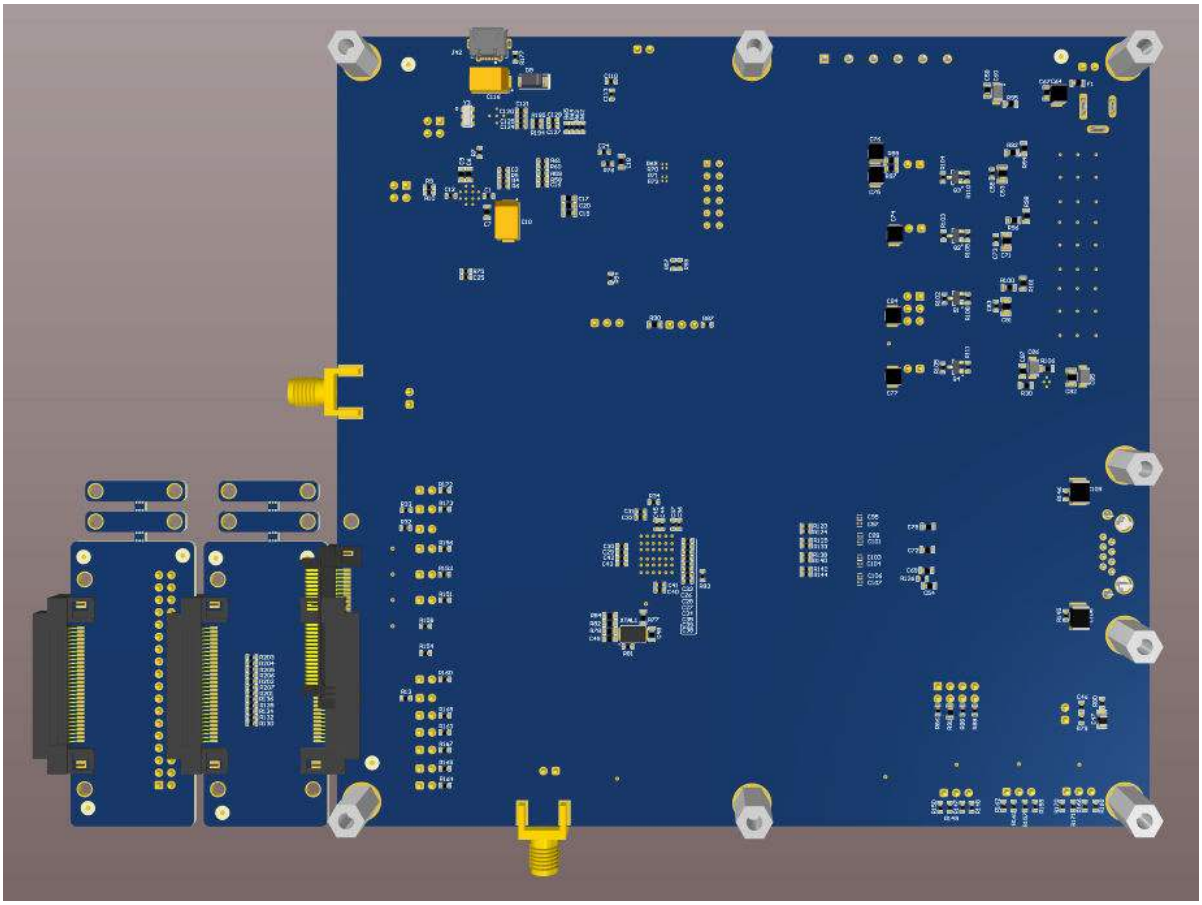

Figure 2-2. DP83561EVM – Bottom Side

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2.2 Block Diagram

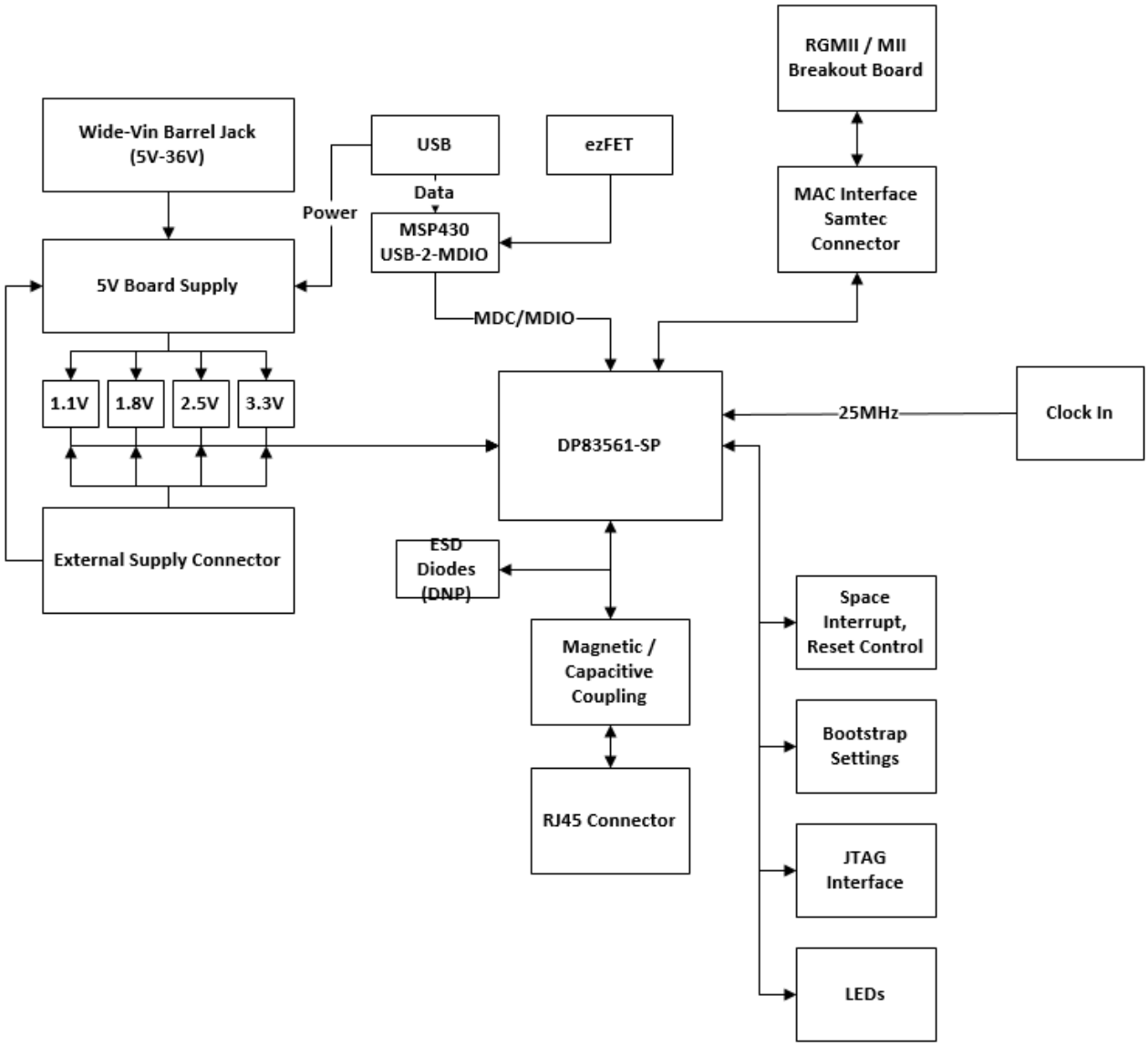

Figure 2-3. DP83561EVM Block Diagram

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2.3 Operation – Quick Setup

The DP83561EVM can operate from a single Wide-Vin 5V-36V DC supply connected to the power jack J16 or the header J18. The DP83561-SP is configured for Dual Supply Mode by default. Due to RJ45 orientation and routing, Mirror Mode is enabled by default. Refer to Section 3.2.2 for additional information on Mirror Mode configuration. The DP83561EVM can be quickly configured as follows:

- Ensure shunt removed at J37 header (set PHY for dual supply mode)
- Place shunt at J15 connecting pins 2 and 3.
- Ensure shunt removed at J23 to disconnect VDDA1P8 LDO (not needed in dual supply mode)
- Place shunt at J20 to connect VDDA2P5 LDO
- Place shunt at P2 in the 3.3 V position to connect VDDIO LDO
- Ensure shunts removed on J35 and J36.
- Place shunt at J24 to connect VDD1P1 LDO
- Ensure shunt removed at J21 header
- Place shunt at J31 to enable Mirror Mode (if necessary, refer to Section 3.2.2).
- **Wide Vin: Connect 5V - 36V to pin 1 of J18 and ground to pin 2 of J18**

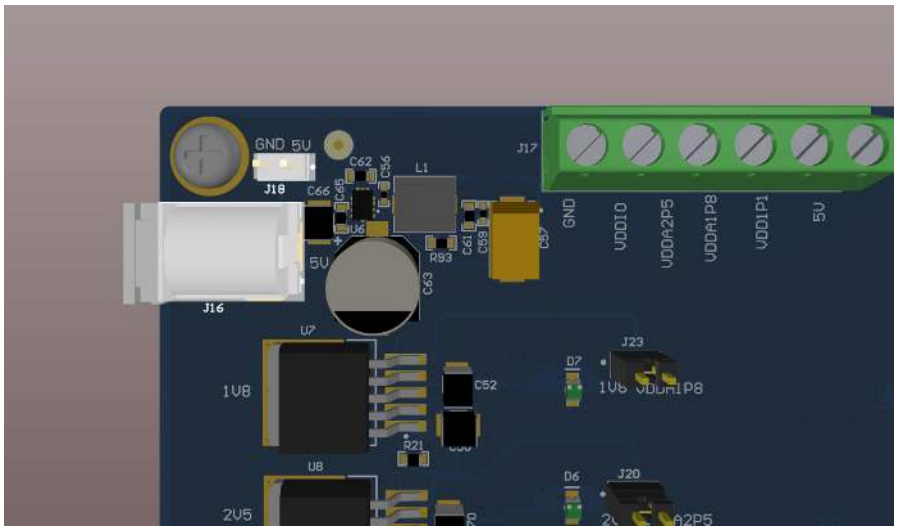

Figure 2-4. Wide-Vin 5V-36V Supply Connection

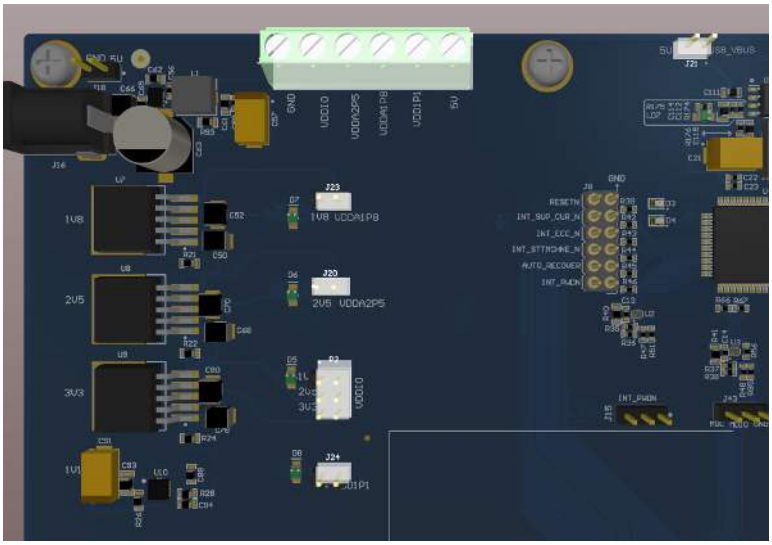

Figure 2-5. DP83561EVM External Supply Connection and Jumpers

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Figure 2-6. DP83561EVM Mirror Mode Strap

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3 Board Setup Details

3.1 Power Supply Selection

Dual Supply Mode vs. Triple Supply Mode

The DP83561-SP can be powered by as few as two supplies in dual supply mode, or three supplies in triple supply mode. In dual supply mode, the VDDA1P8 pin must be left floating. By default the DP83561EVM is configured for dual supply mode. To configure the DP83561-SP in triple supply mode:

- Place shunt on J37 to enable the SUPPLYMODE_SEL strap as described in Section 3.2

The following sections describe powering the DP83561EVM using the on-board LDOs, external supplies, or USB power. Please note that powering the VDDA1P8 pin is only required in triple supply Mode.

3.1.1 VDDIO Selection

In addition to supplying the correct voltage, the DP83561-SP uses straps to select VDDIO levels. If 2.5 V is used as the VDDIO level, the VDDIOSEL_1 strap must be pulled high, which can be done by placing a shunt on J35. If 1.8 V is used asthe VDDIO level, both the VDDIOSEL_1 and VDDIOSEL_0 straps must be pulled high, by placing shunts on J35 and J36. For a VDDIO level of 3.3 V, these pins can be left floating.

Table 3-1. VDDIO Selection Strap Settings

Strap		VDDIO Level
VDDIOSEL_1	VDDIOSEL_0	
0	0	3.3 V
0	1	Reserved
1	0	2.5 V
1	1	1.8 V

Figure 3-1. DP83561EVM VDDIO Selection Straps

3.1.2 On-board Power Supply Operation

- DP83561EVM Onboard Power Using Headers
  - Place shunt at J23 to connect VDDA1P8 LDO (triple supply mode only)
  - Place shunt at J20 to connect VDDA2P5 LDO
  - Place shunt at P2 1.8-V, 2.5-V, or 3.3-V to VDDIO on J17 and place corresponding strap selection shunts
  - Place shunt at J24 to connect VDD1P1 LDO
  - Remove shunt at J21 header
  - **Wide Vin: Connect 5V - 36V to pin 1 of J18 and ground to pin 2 of J18**
- DP83561EVM Onboard Power Using Power Jack

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  - Place shunt at J23 to connect VDDA1P8 LDO (triple supply mode only)
  - Place shunt at J20 to connect VDDA2P5 LDO
  - Place shunt at P2 1.8-V, 2.5-V, or 3.3-V to VDDIO on J17 and place corresponding strap selection shunts
  - Place shunt at J24 to connect VDD1P1 LDO
  - Remove shunt at J21 header
  - **Wide Vin: Connect 5V - 36V to power jack connector J16**

3.1.3 External Power Supply Operation

- DP83561EVM External Power
  - Remove shunt at J23 to disconnect VDDA1P8 LDO
  - Remove shunt at J20 to disconnect VDDA2P5 LDO
  - Remove shunt at P2 to disconnect VDDIO LDO
  - Remove shunt at J24 to disconnect VDD1P1 LDO
  - Remove shunt at J21 header
  - Connect 1.1V to VDD1P1 on J17
  - Connect 1.8V to VDDA1P8 on J15 (triple supply mode only)
  - Connect 2.5V to VDDA2P5 on J17
  - Connect 1.8-V, 2.5-V, or 3.3-V to VDDIO on J17 and place corresponding strap selection shunts
  - Connect ground to GND on J17

3.1.4 USB Power Supply Option

DP838561EVM block powered by USB.

- Place shunt at J23 to connect VDDA1P8 LDO (triple supply mode only)
- Place shunt at J20 to connect VDDA2P5 LDO
- Place shunt at P2 in desired VDDIO level to connect VDDIO LDO and place corresponding strap selection shunts
- Place shunt at J24 to connect VDD1P1 LDO
  - Place shunt at J21 header
- **Connect micro-usb to J42**

Note

Only populate J21 when powering over USB.

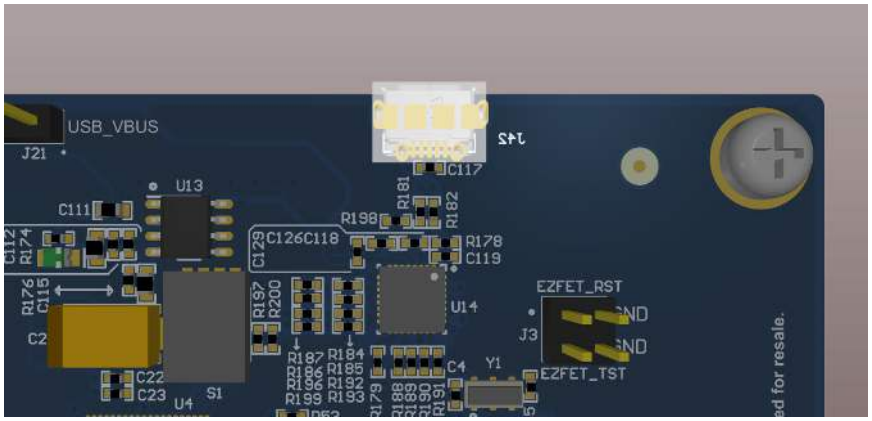

Figure 3-2. DP83561EVM USB Power Supply

3.2 Configuration Options

3.2.1 Bootstrap Options

Some DP83561-SP configurations can be done through bootstrap options. Options can be selected with jumpers or resistor population. Refer to the device data sheet for additional information on bootstrap options. Refer to the schematic and layout sections of this User's Guide for resistor and jumper locations. By default, PHY address must be set to 00 and all straps must be mode 0 except for MIRROR_EN.

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Table 3-2. DP83561-SP 4-Level Bootstrap Resistor Designation and Suggested Bootstrap Resistor Values

PIN NAME	PIN NUMBER	STRAP NAME	STRAP MODE	PU RESISTOR (KΩ)	PU RESISTOR DESIGNATION	PD RESISTOR (KΩ)	PD RESISTOR DESIGNATION
RX_D0	44	PHY_ADD[1:0]	1	OPEN	R152	OPEN	R154
			2	10		2.49	
			3	5.76		2.49	
			4	2.49		OPEN	
RX_D1	45	PHY_ADD[3:2]	1	OPEN	R155	OPEN	R158
			2	10		2.49	
			3	5.76		2.49	
			4	2.49		OPEN	

Table 3-3. DP83561-SP 2-Level Bootstrap Selection and Jumper Designation

PIN NAME	PIN NUMBER	STRAP NAME	STRAP MODE	JUMPER PLACEMENT	JUMPER DESIGNATION
VDDIOSEL_0	22	VDDIOSEL_0	0	OPEN	J36
			1	CLOSED	
VDDIOSEL_1	21	VDDIOSEL_1	0	OPEN	J35
			1	CLOSED	
SUPPLYMODE_SEL	23	SUPPLYMODE_SEL	0	OPEN	J37
			1	CLOSED	
CRS/GPIO_3	33	RGMII/MII_SEL	0	OPEN	J41
			1	CLOSED	
AUTO_RECOVER	34	AUTO_RECOVER	0	OPEN	J39
			1	CLOSED	
RX_CTRL	48	MIRROR_EN	0	OPEN	J31
			1	CLOSED	
SMI_DISABLE	50	SMI_DISABLE	0	OPEN	J40
			1	CLOSED	
POWERGOOD	59	POWERGOOD	0	OPEN	N/A
			1	CLOSED	

Table 3-4. DP83561-SP LED Bootstrap Selection and Jumper Designation

PIN NAME	PIN NUMBER	STRAP NAME	STRAP MODE	JUMPER PLACEMENT	JUMPER DESIGNATION
LED_0	63	ANED_DIS	0	OPEN/PD	J28
			1	PU	
LED_1	62	ANEGSEL_0	0	OPEN/PD	J33
			1	PU	
LED_2	45	ANEGSEL_1	0	OPEN/PD	J38
			1	PU	

3.2.2 Mirror Mode

The DP83561EVM enables Mirror Mode by default. As can be observed in Section 8.4, due to the RJ45 orientation and routing on the board, the differential transmit and receive pairs orientation and polarity have been flipped on J27. Mirror mode must be enabled to correct this change, unless the link partner uses a similar routing and layout strategy, matching the differential pairs correctly.

3.3 Clock Selection

3.3.1 On-Board 25 MHz Crystal

By default, the DP83561 is configured to use the on-board 25 MHz crystal. To verify the on-board 25 MHz crystal is properly connected, confirm the following:

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- Remove R84
- Populate R82, R77

3.3.2 External Clock

To remove the on-board 25 MHz crystal and supply an external 25 MHz clock:

- Remove R82, R77
- Populate R84
- Provide External Clock to SMA at J11

3.4 MAC Interface Breakout Connectors

The DP83561EVM comes with two MAC interface breakout boards, and RGMII back-to-back connector board, and a MAC interface breakout board. When configuring the DP83561-SP for MII mode, the MAC interface breakout board must be used to access the MII pins.

RGMII Back-to-Back Configuration

- Connect J4 of the main DP83561EVM board to J22 of the RGMII back-to-back connector
- Connect J19 of the RGMII back-to-back connector to a second DP83561EVM or other RGMII MAC

Note

RGMII back-to-back connector is reversible, RGMII back-to-back breakout connector can be conneted to a DP83561EVM on either J19 or J22.

Figure 3-3. DP83561EVM RGMII Back-to-Back Connection Diagram

MAC Interface Breakout Board Configuration

The MAC Interface Breakout Board can be used to directly access the MII pins of the DP83561-SP. This board can be used for configurations such as configuring the DP83561EVM for RGMII external loopback tests as described by RGMII BER Testing - External Loopback Configuration, or connecting an MII MAC.

- Connect J4 of the main DP83561EVM board to J1 of the MAC interface breakout board

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- MAC interface pins can be accessed via J2 of the MAC interface breakout board connector.

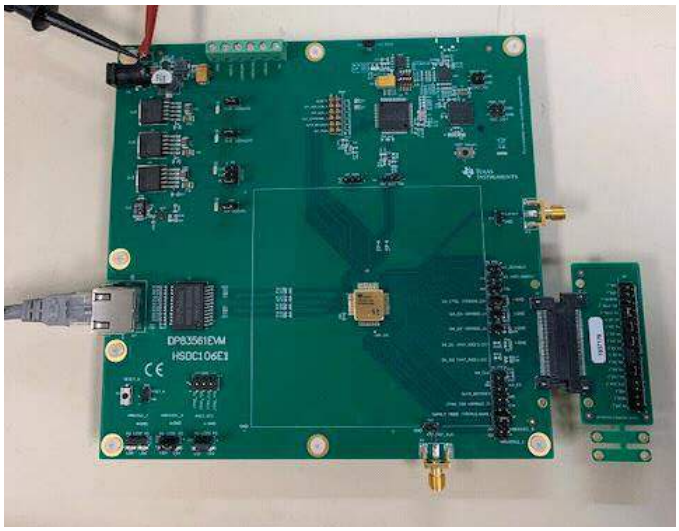

Figure 3-4. MAC Interface Breakout Board Connection

3.5 LED Indication

- Look for D5, D6, D7, and D8 to illuminate when power is successfully supplied to each power rail.
- LED0, LED1, LED2 can be configured through LEDS_CFG1 Register 0x18
  - By default, LED0 indicates valid link established.
  - By default, LED1 indicates 1000Base-T link established
  - By default, LED2 indicates RX/TX activity

3.6 Serial Management Interface

The DP83561EVM supports SMI (MDIO/MDC) through J43 and includes an on-board MSP for USB-2-MDIO control.

Notes:

- DP83561-SP default PHY_ID is 00
- PHY IDs can be changed through bootstrap options found in the datasheet

3.7 Cable Assembly

- Plug a CAT5, CAT5E, or CAT6 cable into the RJ45 connector J16
- In applications where Mirror Mode needs to be enabled, place shunt on J31

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4 BER Testing

The DP83561EVM supports BER testing through RGMII back-to-back configuration and/or internal loopback modes.

RGMII BER Testing - Back-to-Back Configuration

The DP83561EVM supports RGMII BER testing through back-to-back configuration as described by RGMII Back-to-Back Configuration. BER testing can be conducted using two DP83561EVMs and two link partners by checking the packets sent and received by the two link partners.

Referring to Figure 3-3, should a second link partner, Link Partner B, be unavailable, DP83561EVM B can be programmed into Analog Loopback for the BER test. In this case, Link Partner A will send data across the cable to DP83561EVM A, to be sent across the RGMII interface to DP83561EVM B, looped back to DP83561EVM A, and received by Link Partner A. Please note, that in Analog Loopback, the MDI output pairs must have a 100 ohm differential termination. The RGMII Transmit Clock Delay must be set such that the RGMII transmit clock is aligned with respect to transmit data for both boards. This can be done with the following register write:

- Write Register 0x32 = 0xD2

For additional information on configuring loopback modes, please refer to the device data sheet.

RGMII BER Testing - External Loopback Configuration

The DP83561EVM support RGMII BER testing through an external loopback configuration using the MAC Interface Breakout Board. The MAC Interface Breakout Board may be connected to the main DP83561EVM board as described in MAC Interface Breakout Board Configuration. To configure the MAC Interface Breakout Board for external loopback, jumpers must be placed to connect the transmit pins to the corresponding receive pins. Refer to Figure 4-1 for a connection diagram. The RGMII Transmit Clock Delay must be set such that the RGMII transmit clock is aligned with respect to transmit data. This can be done with the following register write:

- Write Register 0x32 = 0xD2

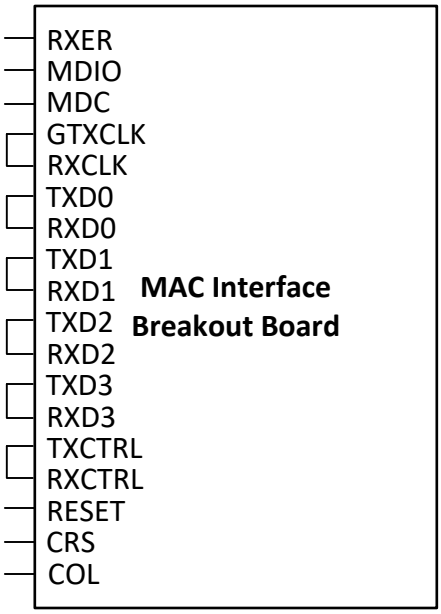

Figure 4-1. MAC Interface Breakout Board External Loopback Connection Diagram

MII BER Testing

In MII mode, the MAC Interface Breakout Board may be used as described in MAC Interface Breakout Board Configuration to support MII BER testing. Referring to Figure 4-2, the link partner, which can be another DP83561EVM, must be configured for Reverse Loopback, and the MII MAC must be configured to generate and

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receive packets, and check for errors. For additional information on configuring loopback modes, please refer to the device data sheet.

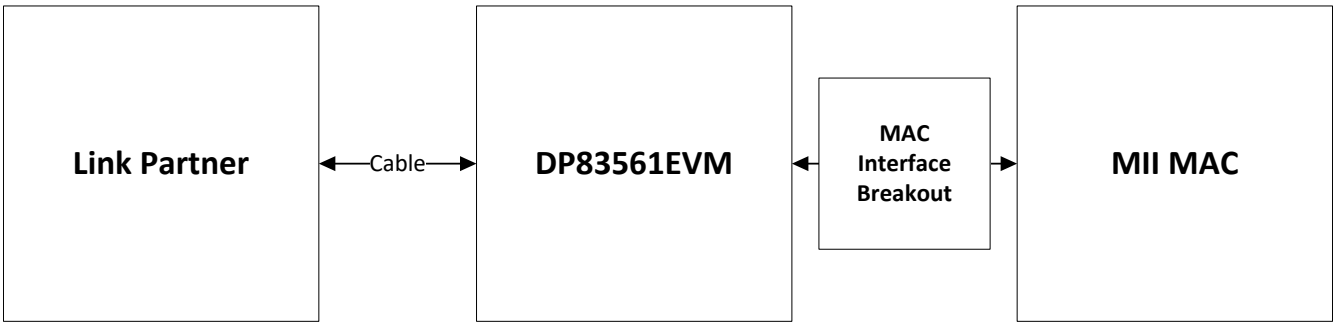

Figure 4-2. DP83561EVM BER Testing MII Connection Diagram

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5 Compliance Testing

The DP83561EVM supports IEEE 802.3 Ethernet Compliance testing, providing an option to connect a test fixture via an RJ45 connector on J16. Please refer to the device datasheet for details on setting the different Ethernet Compliance Test Modes.

Figure 5-1. DP83561EVM Compliance Test Fixture Connection

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6 SEFI Support Monitoring

The DP83561-SP offers a SEFI monitoring suite, monitoring the IEEE PCS state machine, ECC configuration register, supply current, PLL lock, and on-chip temperature. When Auto-Recovery is enabled, the device will automatically reset the PHY when a SEFI is detected. Please refer to the device datasheet for detailed descriptions of each function. This section describes how to observe each interrupt using the DP83561EVM. The DP83561EVM has hooks to observe the following SEFI events:

- IEEE PCS State Machine Monitor
  - If any invalid state changes are made, the DP83561 will indicate a SEFI has occurred and raise the INT_STTMCHNE_N signal.
  - The INT_STTMCHNE_N signal can be observed on the INT_STTMCHNE_N pin of J8.
- ECC Configuration Register Monitor
  - If any change in the configuration registers are detected or corrected by the ECC, an interrupt on the INT_CHECKSUM_N signal will be raised for indication to the higher level system.
  - The INT_CHECKSUM_N signal can be observed on the INT_CHECKSUM_N pin of J8.
- Supply Current Monitor
  - When supply current changes exceed the expected normal operating conditions, the INT_SUP_CUR_N signal will be asserted.
  - The INT_SUP_CUR_N signal can be observed on the INT_SUP_CUR_N pin of J8.
- Temperature Monitor
  - The DP83561-SP has an on chip temperture monitor. The value measured by the sensor can be read using the following steps:
    - Write value 0xCD24 to register 0x01E8
    - Read measured value off of register 0x01EA

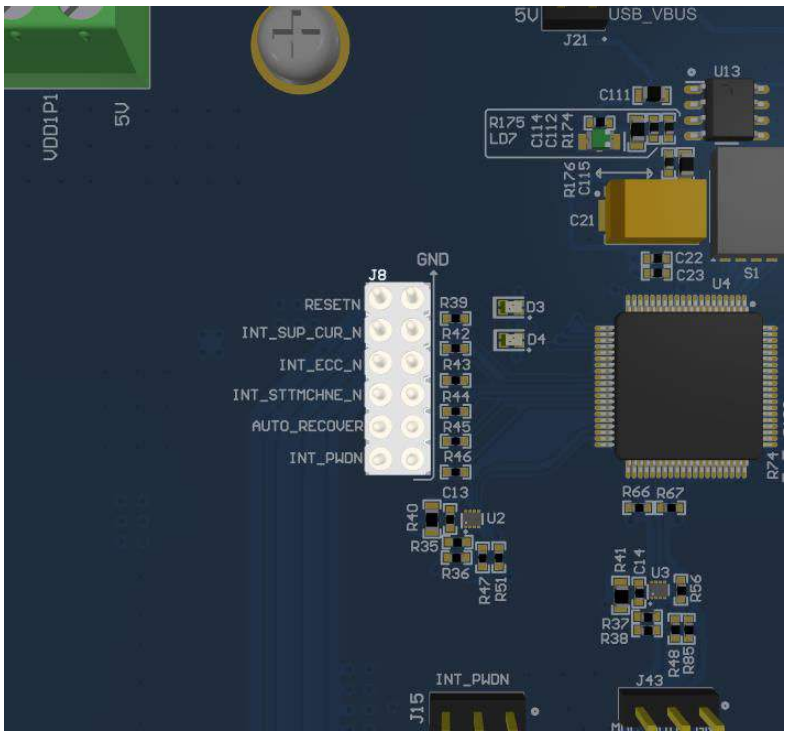

Figure 6-1. DP83561EVM SEFI Interrupt Pins

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Note

To use the pins INT_SUP_CUR_N, INT_ECC_N, and INT_STTMCHNE_N as an interrupt, they must be pulled up to VDDIO through use of an external 2.2k pull-up resistor. The resistors R42, R43, and R44 respectively may be replaced with a 2.2k resistor and connected to VDDIO. VDDIO can be accessed via pins 2, 4, and 6 of header P2.

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7 Software

The on-board MSP430 comes pre-programmed and ready to use. When using this EVM for the first time on a Windows 7 (or above) PC, MSP430 drivers and USB-2-MDIO software utility will have to be installed. USB-2-MDIO software can be used for accessing the PHY's registers. In the case where an external MSP430 or ezFET is needed, the user may simply connect the TST and RST pins of their device to the DP83561EVM.

7.1 MSP430 Driver

Install the latest MSP430 driver from this website: *http://software-dl.ti.com/msp430/msp430_public_sw/mcu/msp430/MSP430_FET_Drivers/latest/index_FDS.html*

http://software-dl.ti.com/msp430/msp430_public_sw/mcu/msp430/MSP430_FET_Drivers/latest/index_FDS.html.

7.2 USB-2-MDIO Software

Download the software from http://www.ti.com/tool/usb-2-mdio*https://www.ti.com/tool/usb-2-mdio* .

The webpage also contains the User's Guide for installing and using the software. Because the MSP430 is on-board the DP83561EVM, it is not necessary to purchase a separate MSP430 Launchpad kit and connect to the PHY using wires. In the case the on-board MSP430 cannot be used for some reason, MDIO and MDC pins are also broken out on J23 and J22 pins, respectively. Users can connect an MSP430 launchpad or their own MDIO-MDC utility on J23 and J22 to access the PHY

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8 Schematics

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8.1 Main Power Schematic

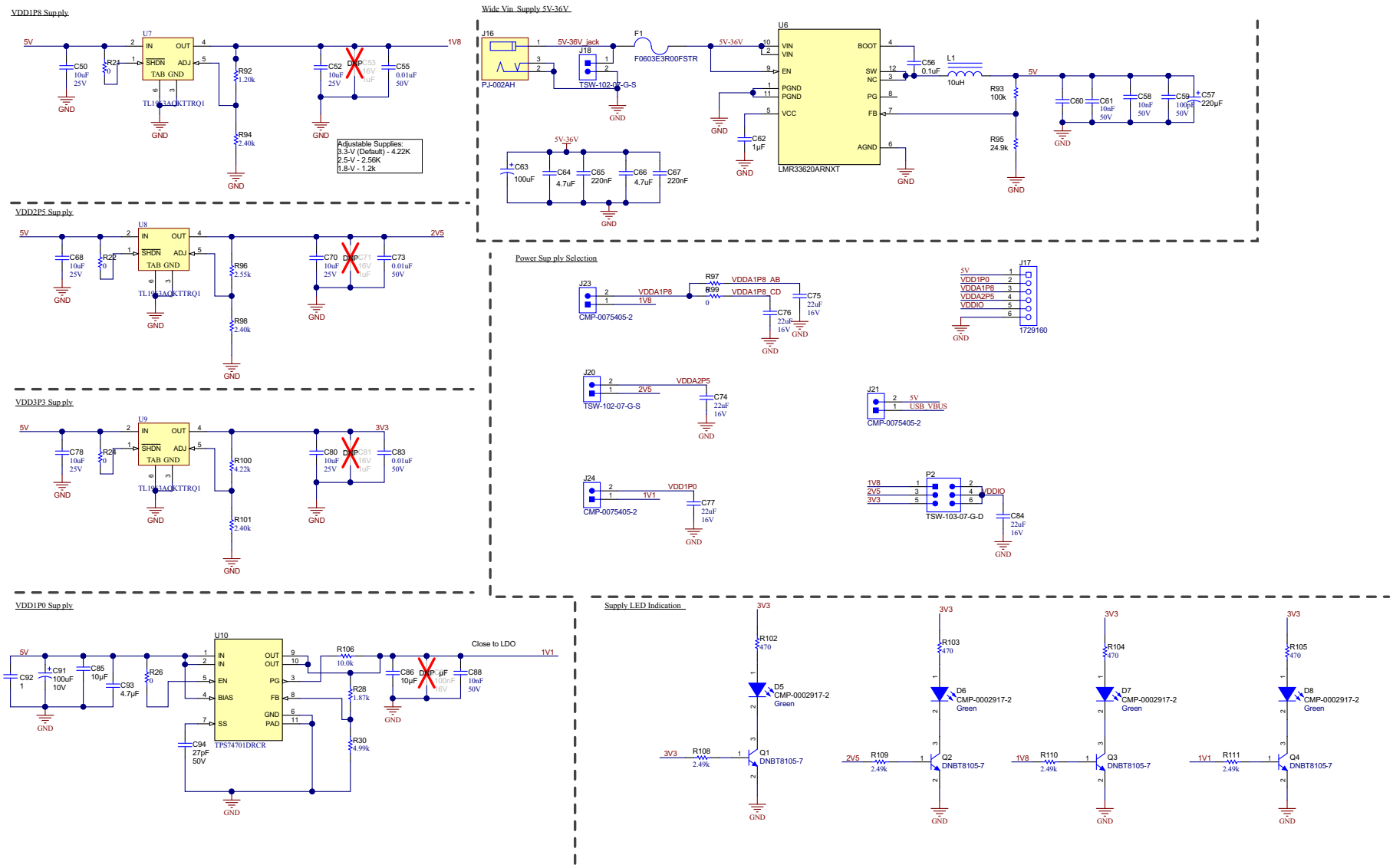

Figure 8-1. DP83561EVM Main Power

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8.2 Main Block Schematic

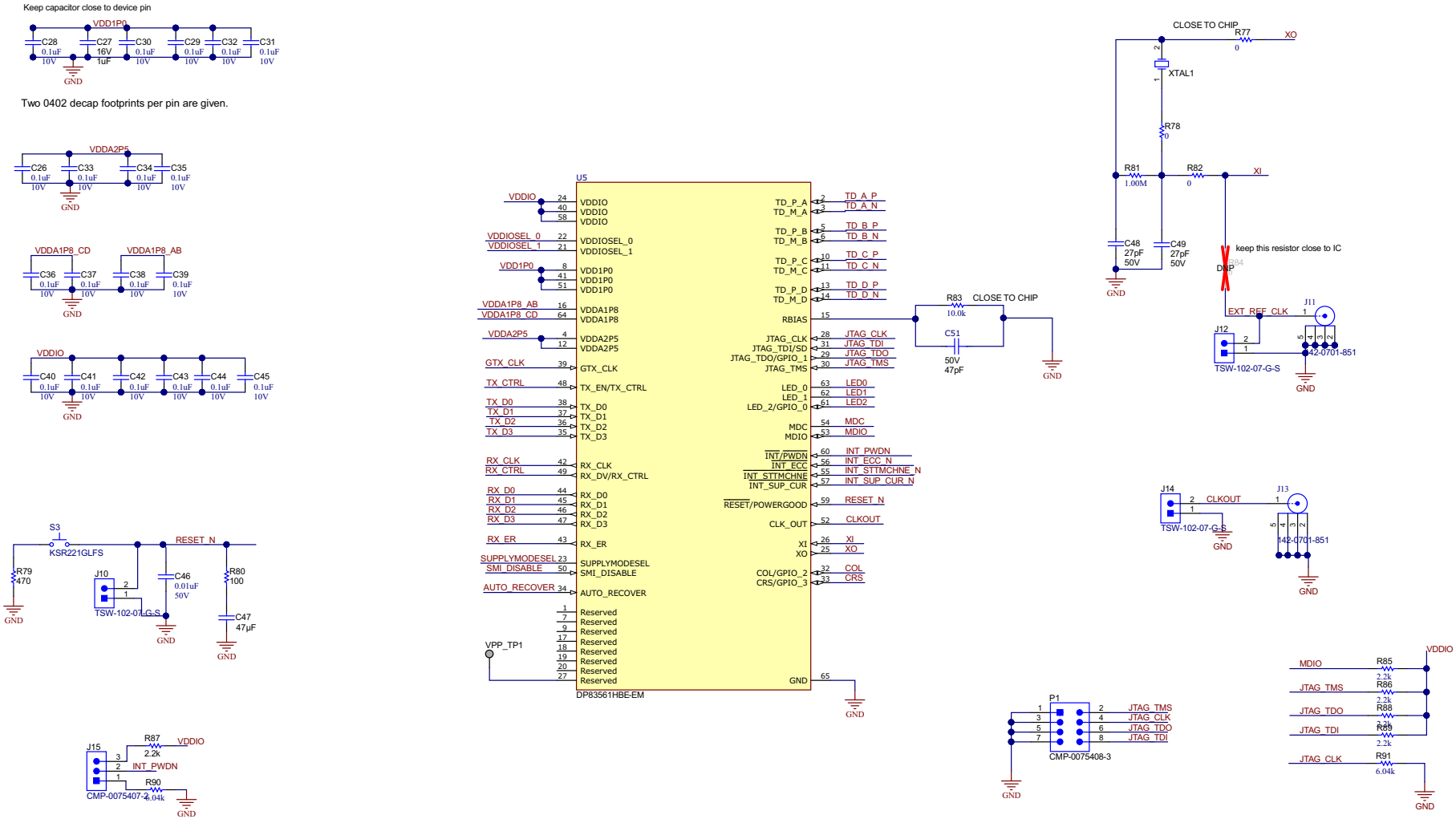

Figure 8-2. DP83561EVM Main Block

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8.3 Bootstrap Settings Schematic

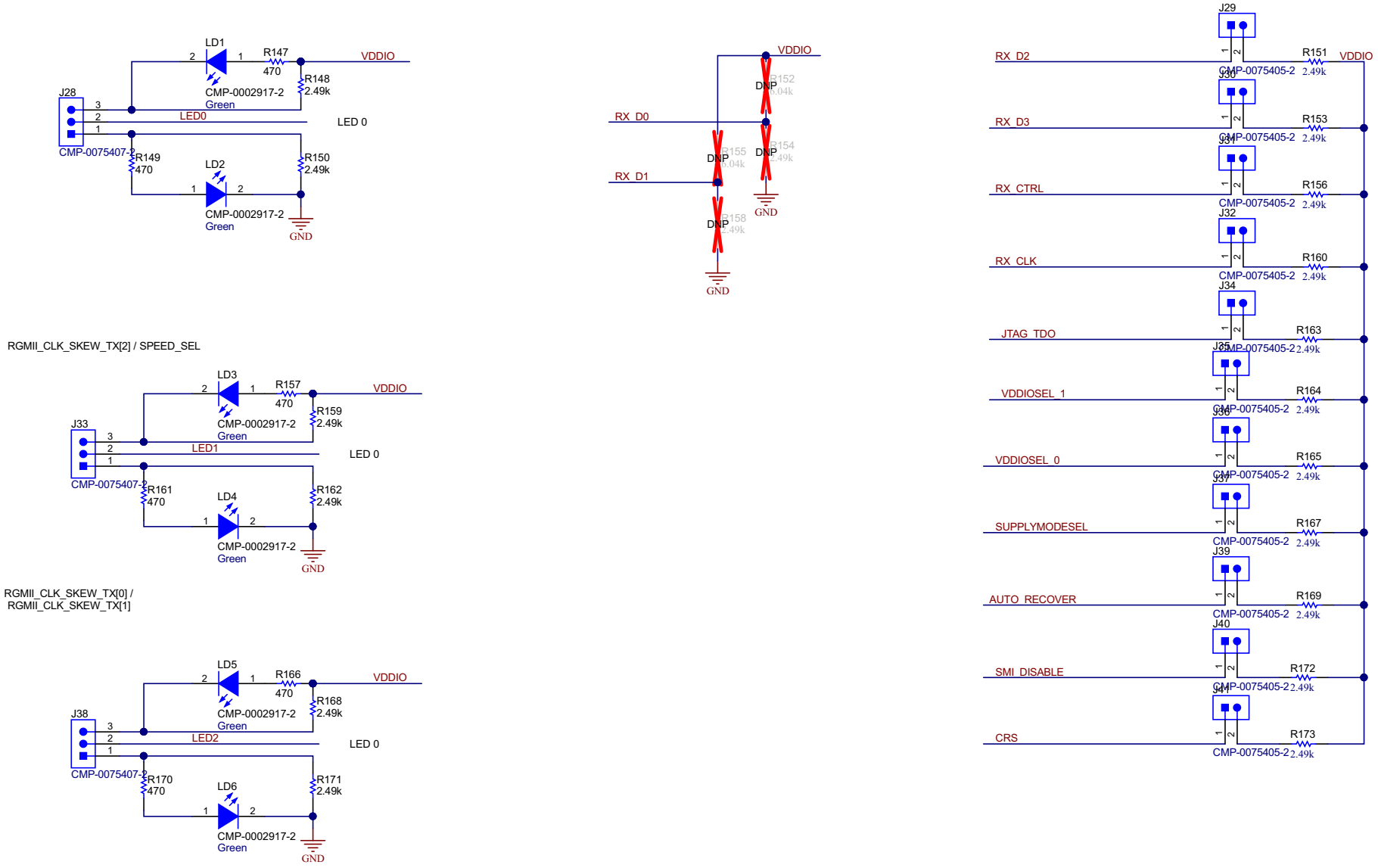

Figure 8-3. DP83561EVM Bootstrap Settings

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8.4 Analog Front End and MAC Interface Schematic

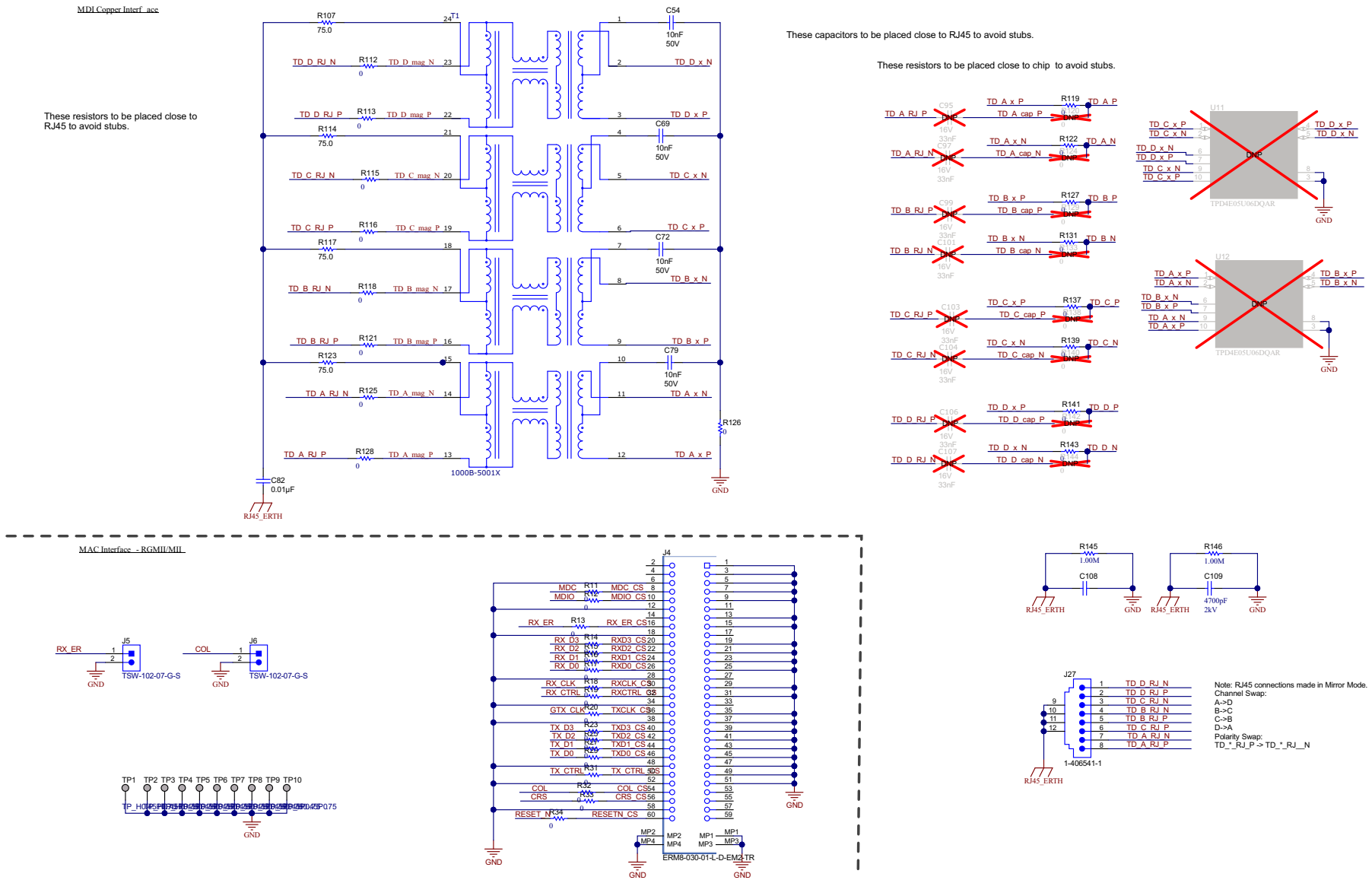

Figure 8-4. DP83561EVM AFE and MAC Interface

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8.5 USB Hub Schematic

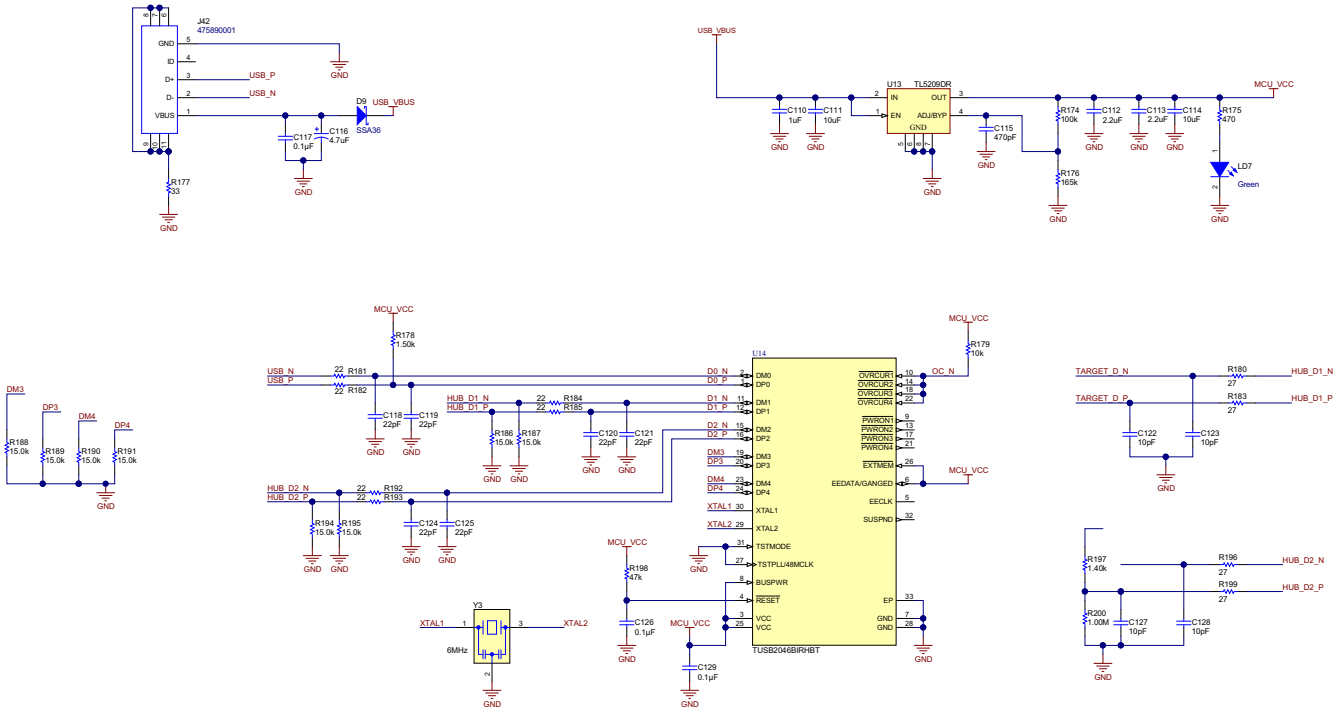

Figure 8-5. DP83561EVM USB Hub

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8.6 COMs 1 Schematic

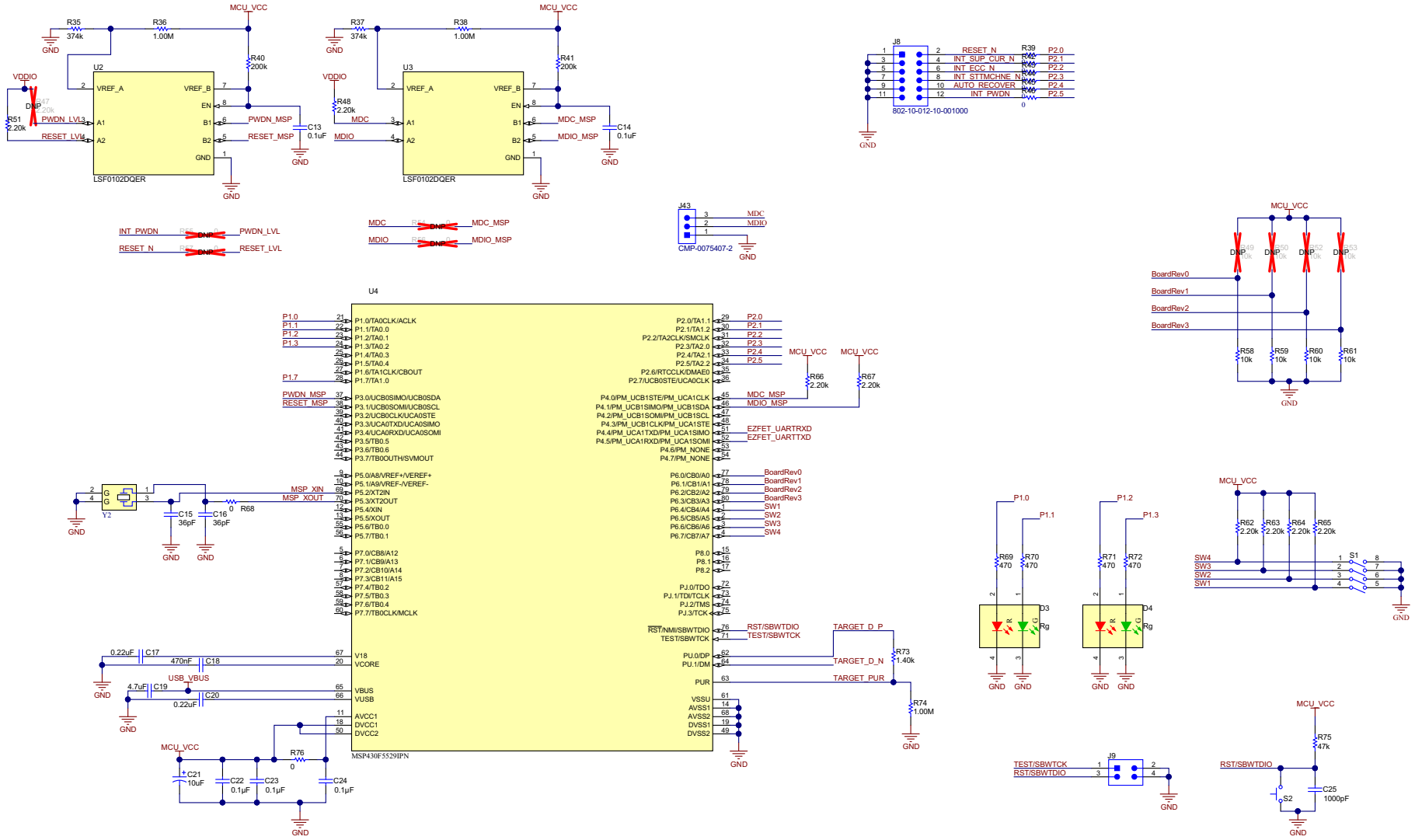

Figure 8-6. DP83561EVM COMs 1

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8.7 COMs 2 Schematic

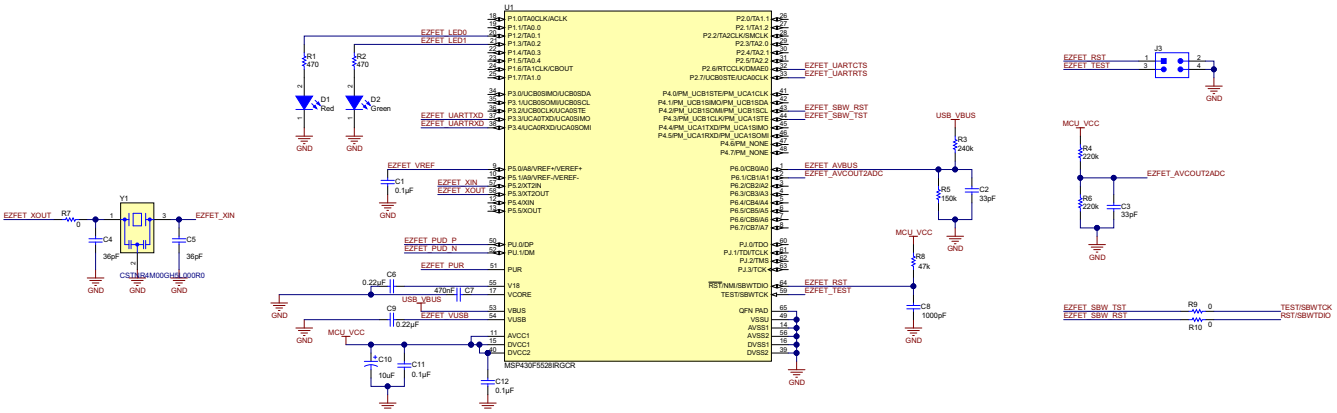

Figure 8-7. DP83561EVM COMs 2

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8.8 Breakout Boards Schematic

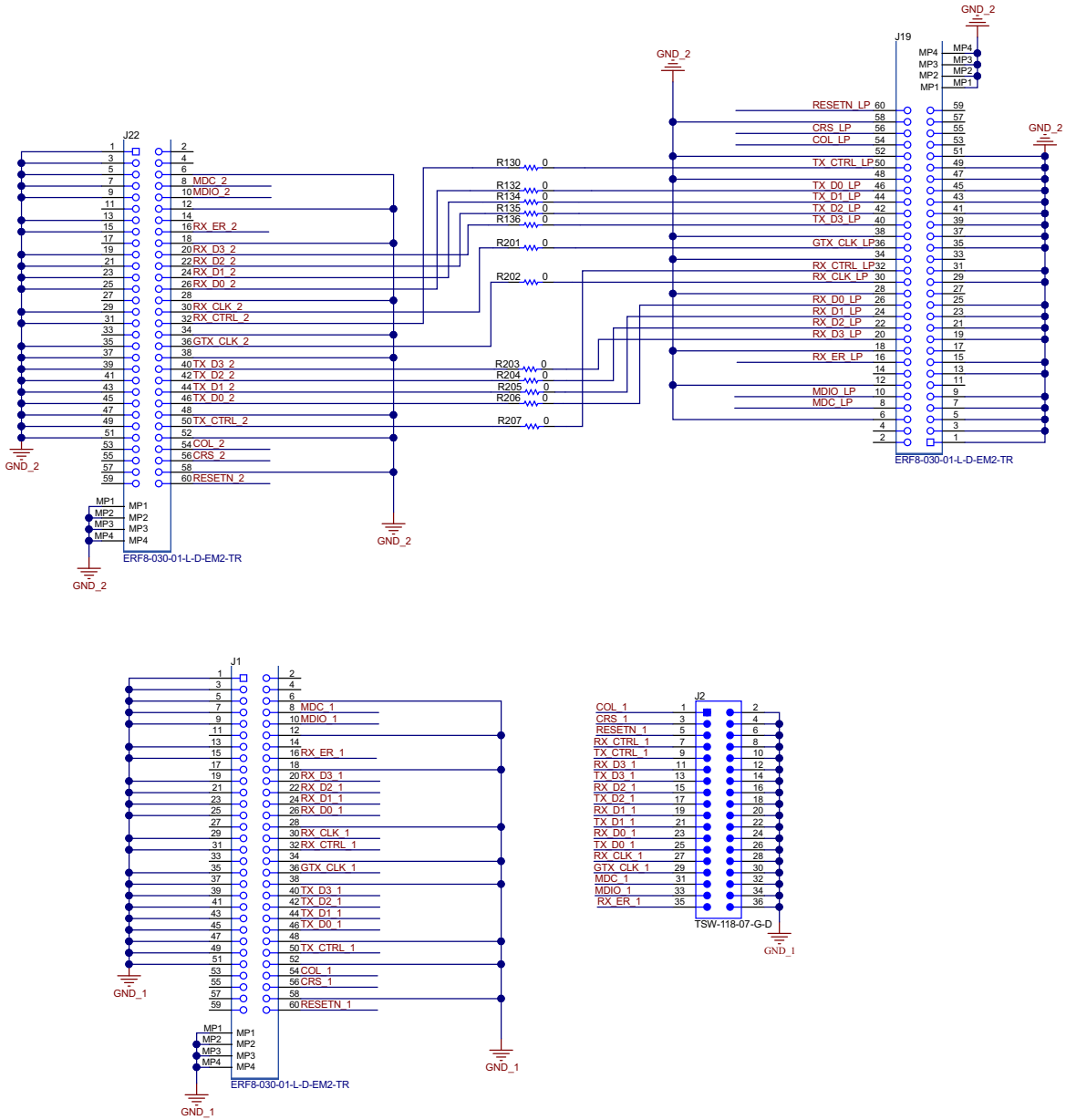

Figure 8-8. DP83561EVM Breakout Connectors

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8.9 Hardware Schematic

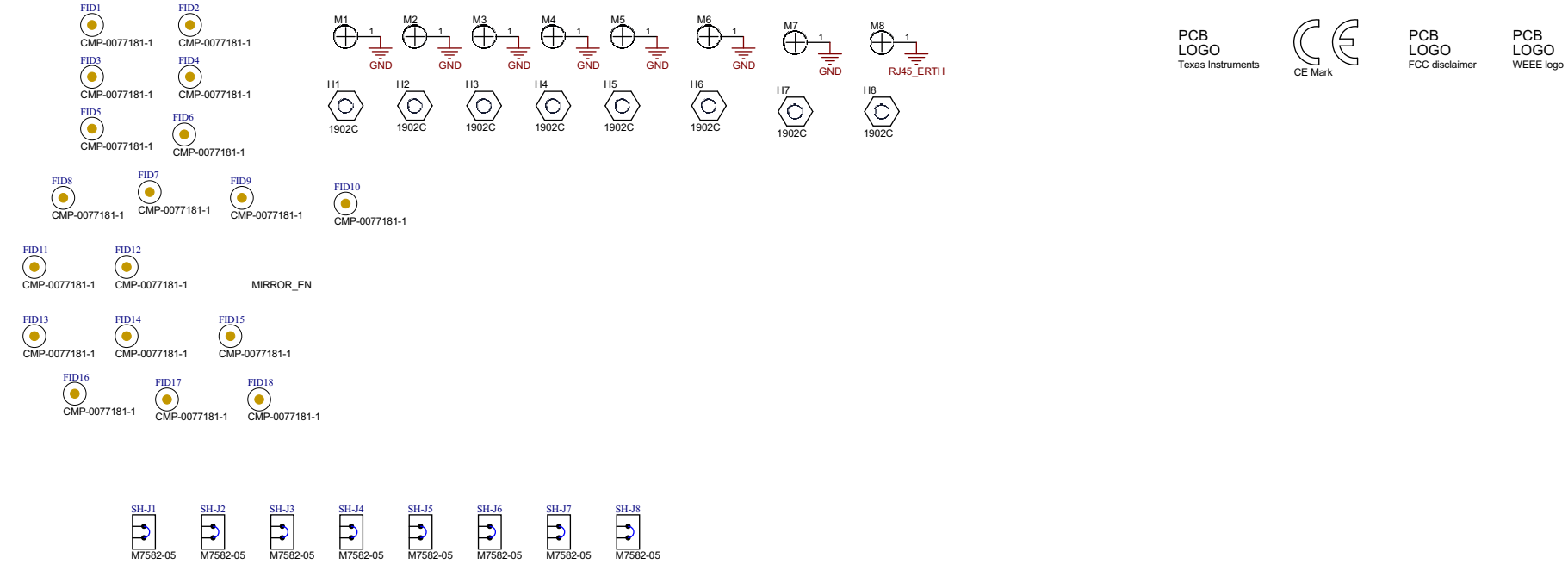

Figure 8-9. DP83561EVM Hardware

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9 Layout

9.1 Top Overlay

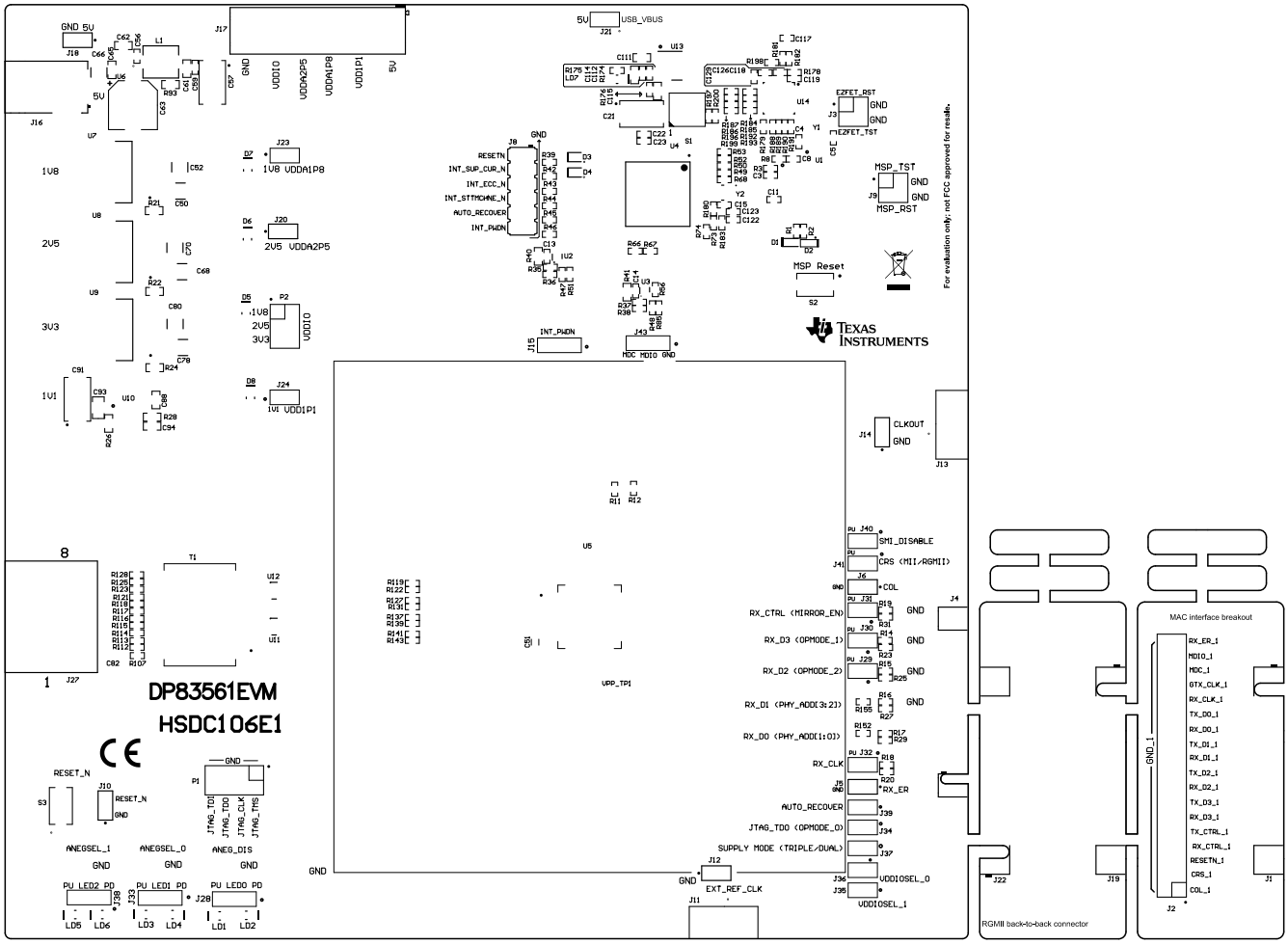

Figure 9-1. Top Overlay

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9.2 Top Layer Mask

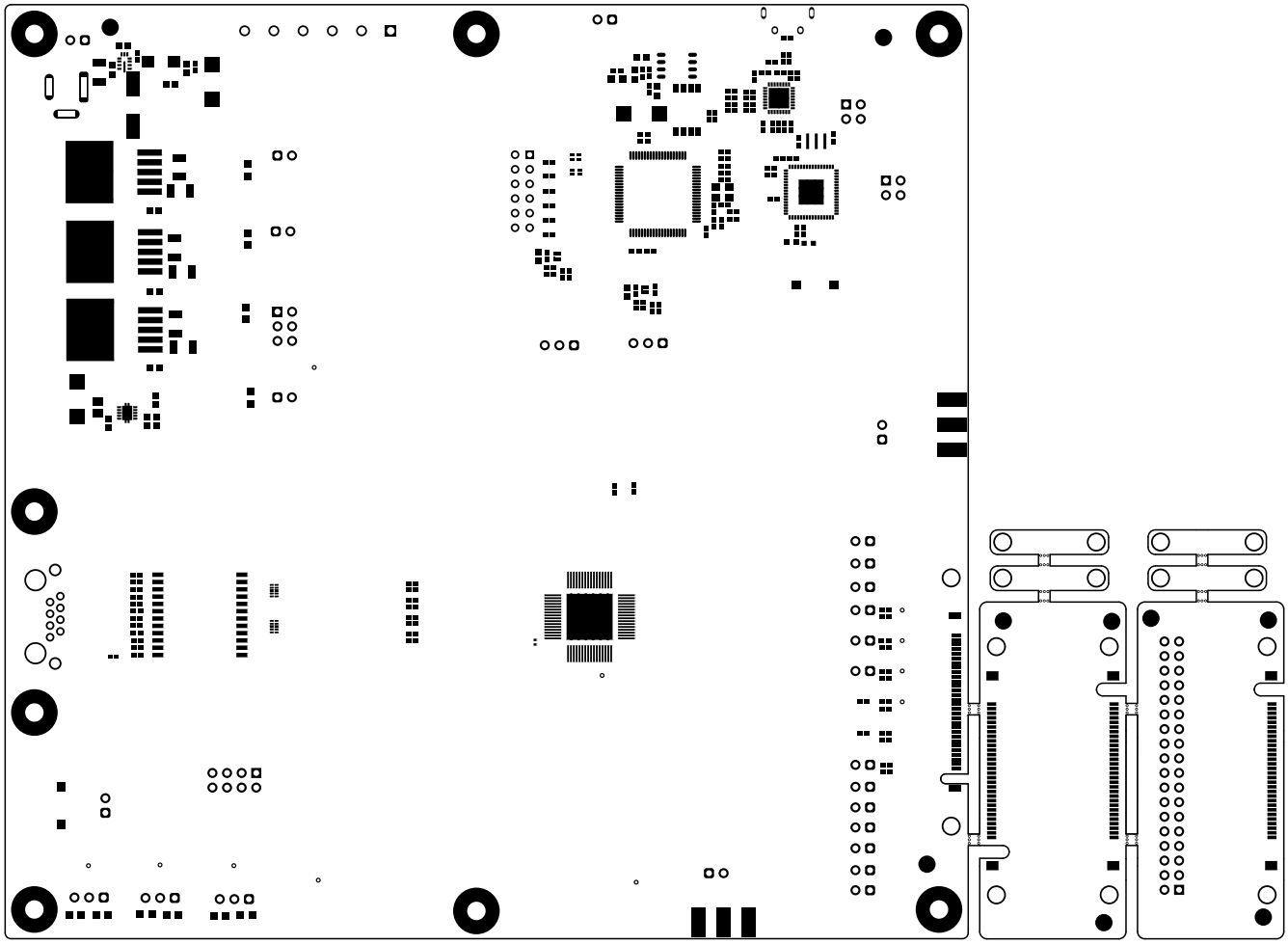

Figure 9-2. Top Layer Mask

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9.3 Top Layer

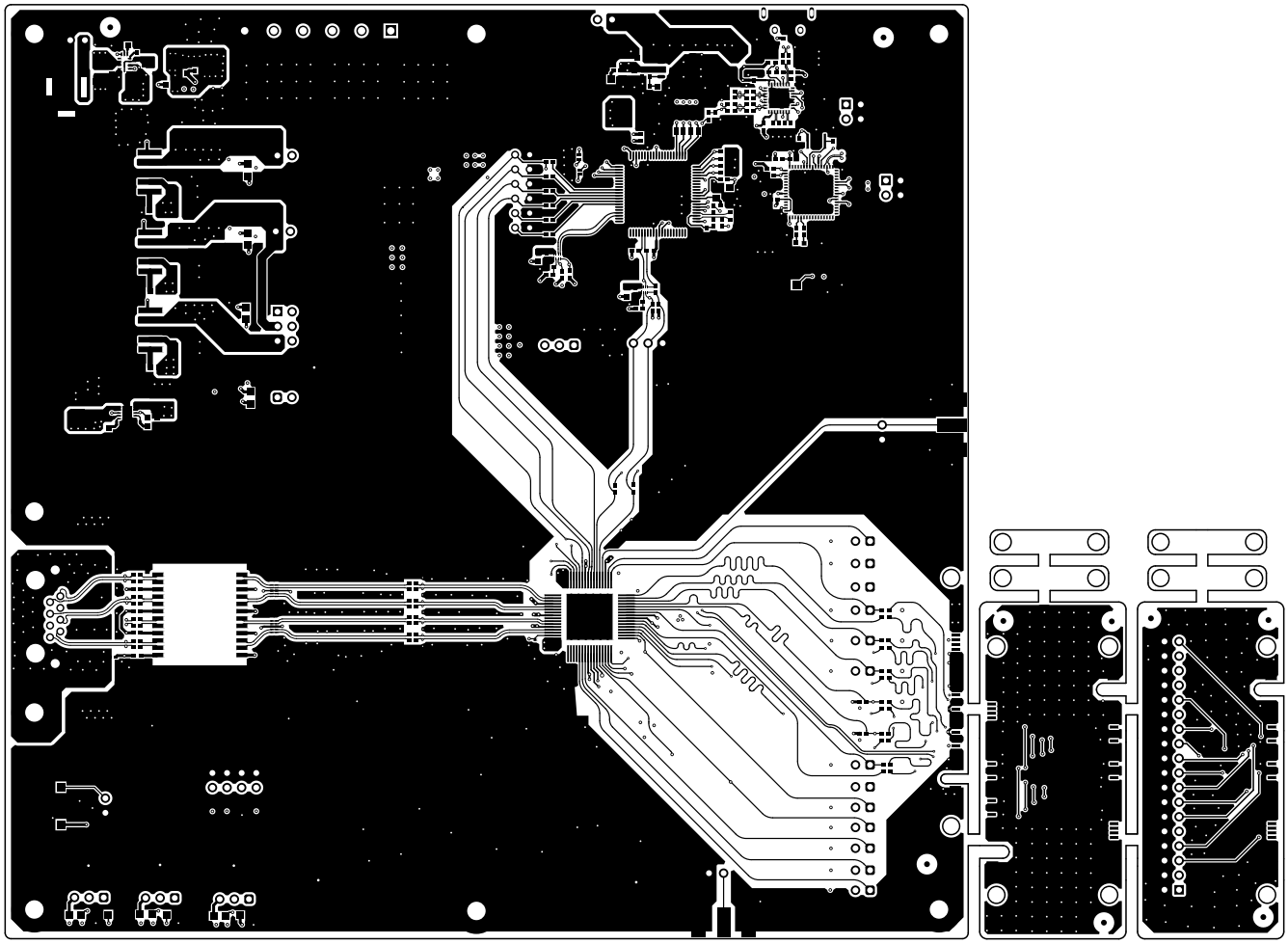

Figure 9-3. Top Layer

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9.4 Ground Layer 1

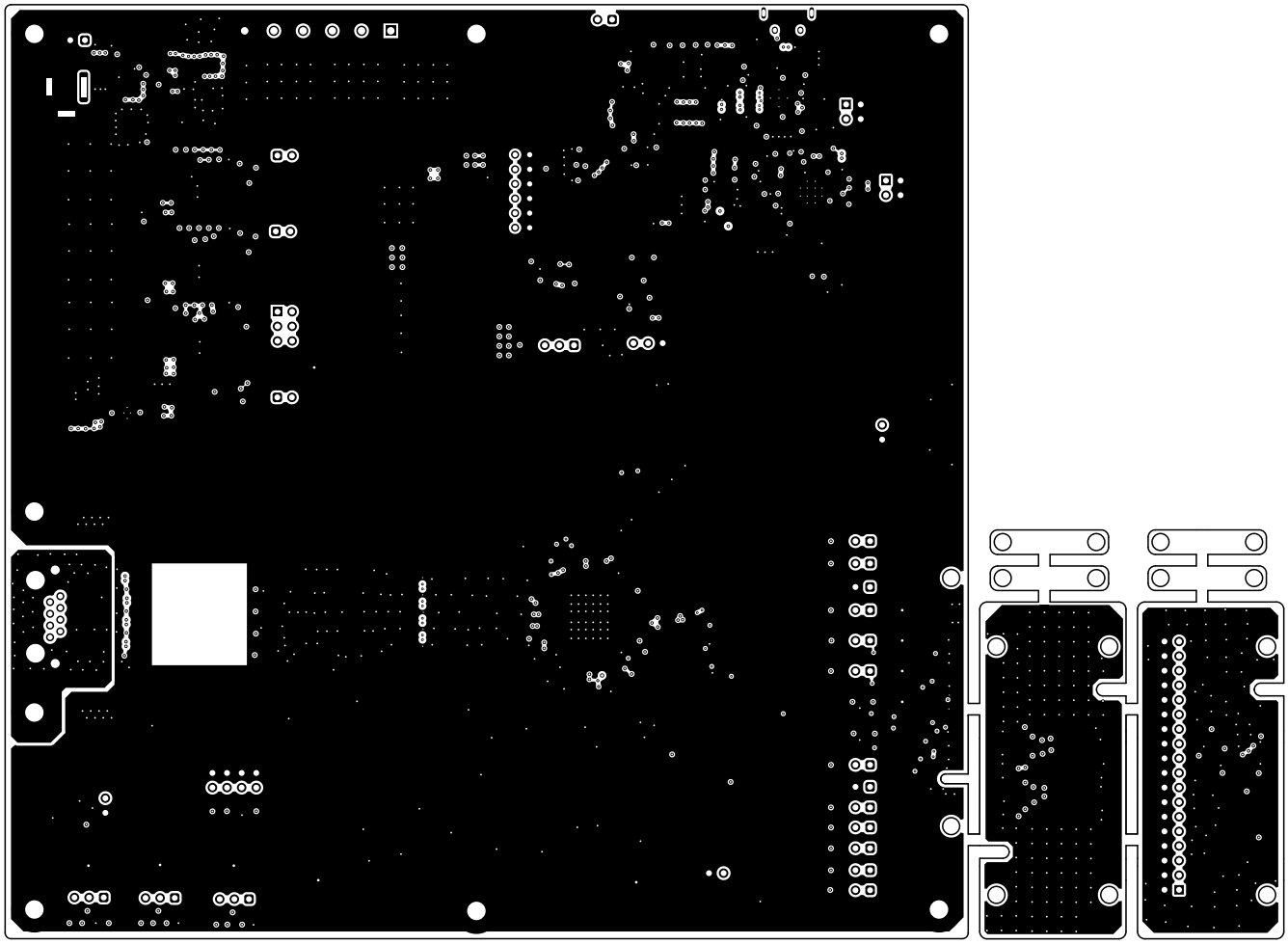

Figure 9-4. Ground Layer 1

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9.5 Signal Layer 1

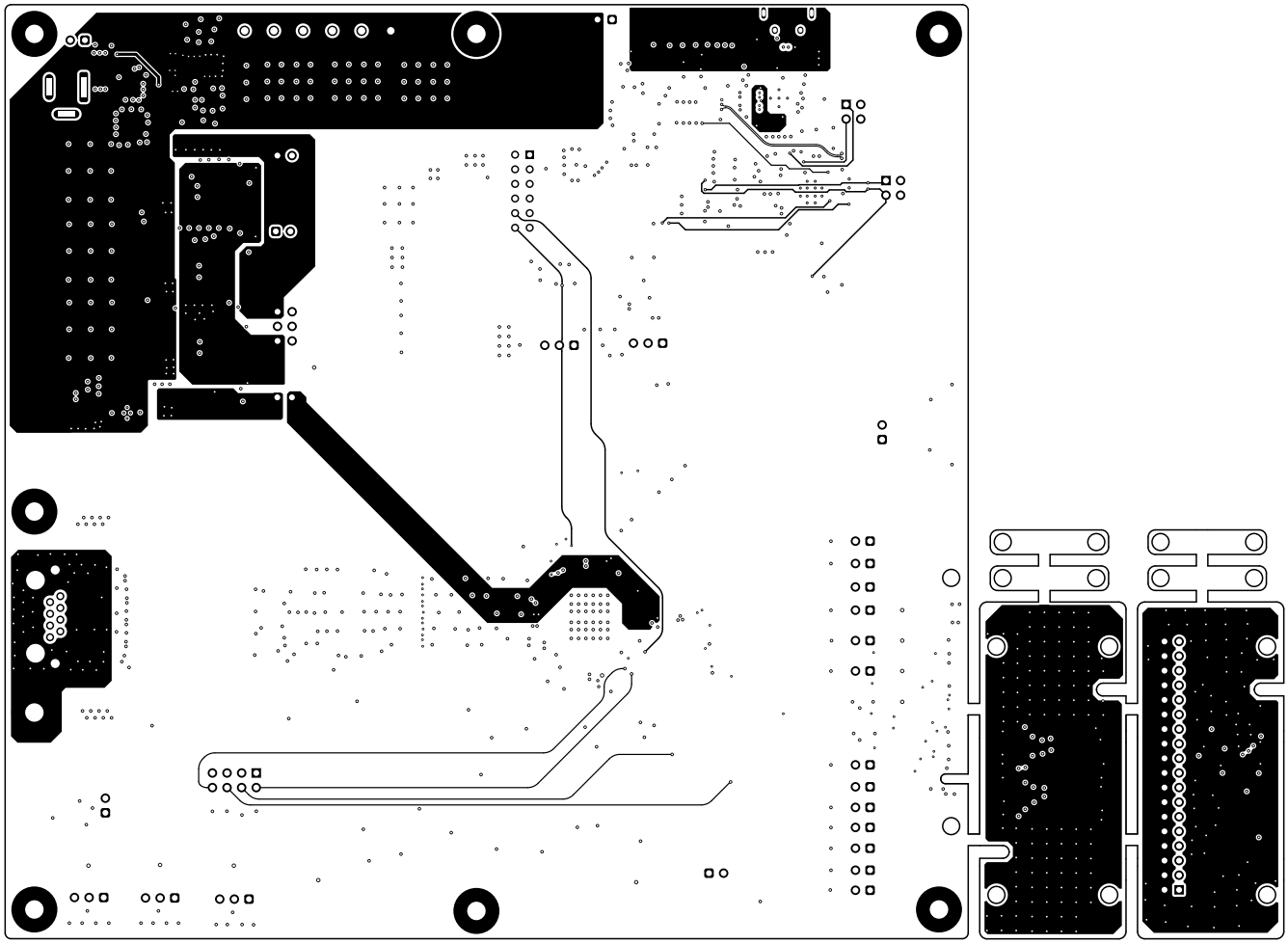

Figure 9-5. Signal Layer 1

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9.6 Signal Layer 2

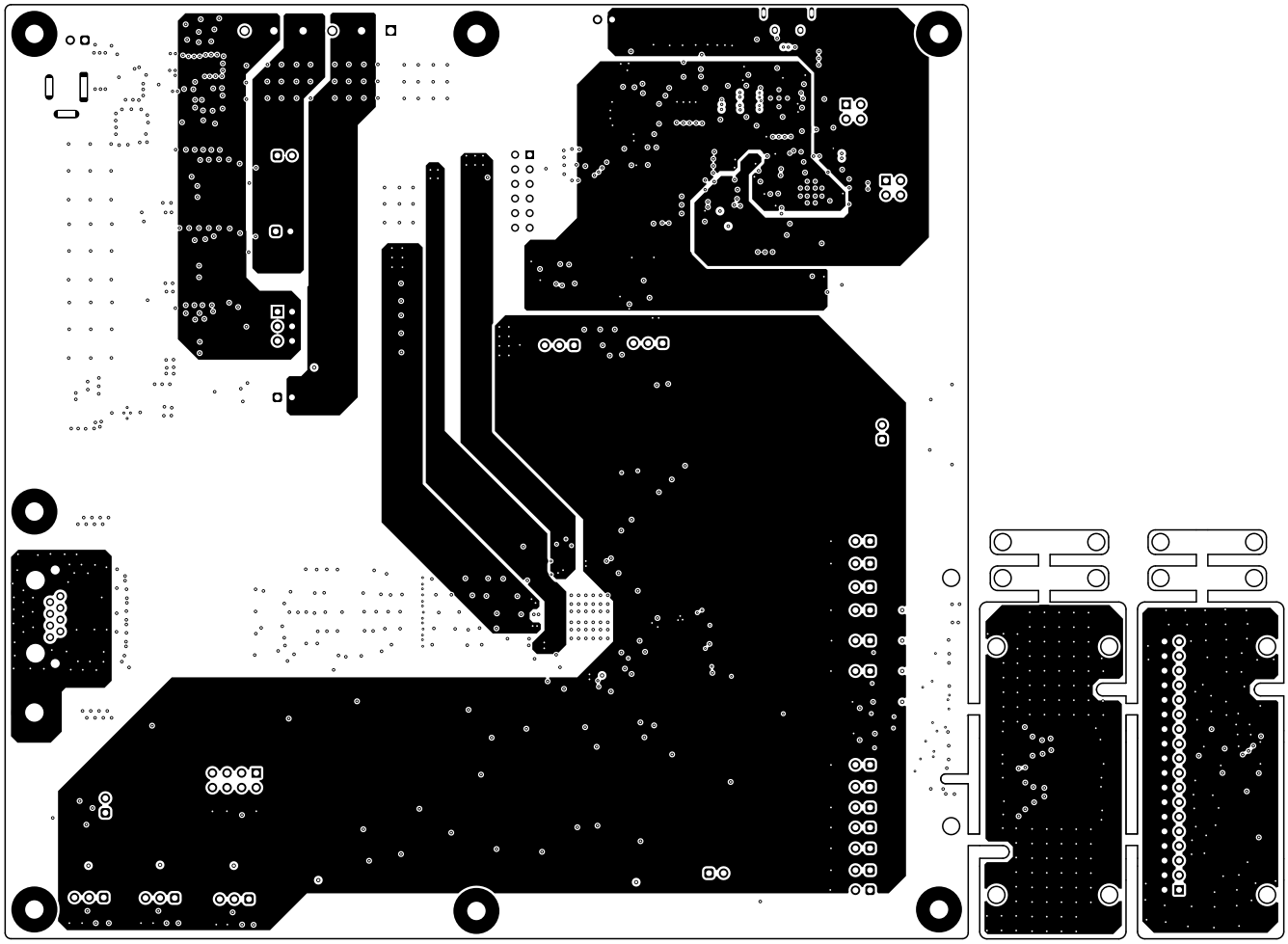

Figure 9-6. Signal Layer 2

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9.7 Ground Layer 2

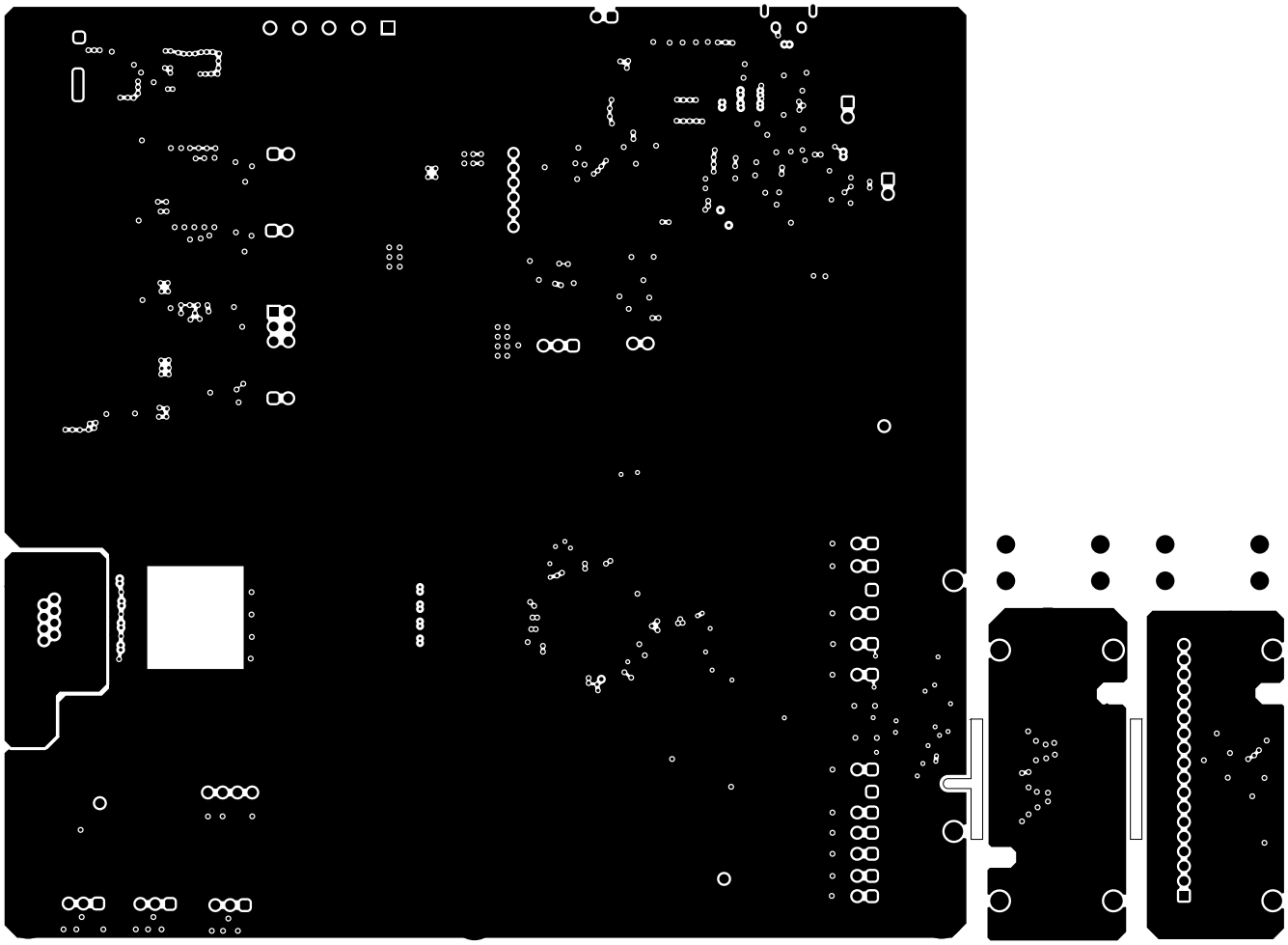

Figure 9-7. Ground Layer 2

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9.8 Bottom Layer

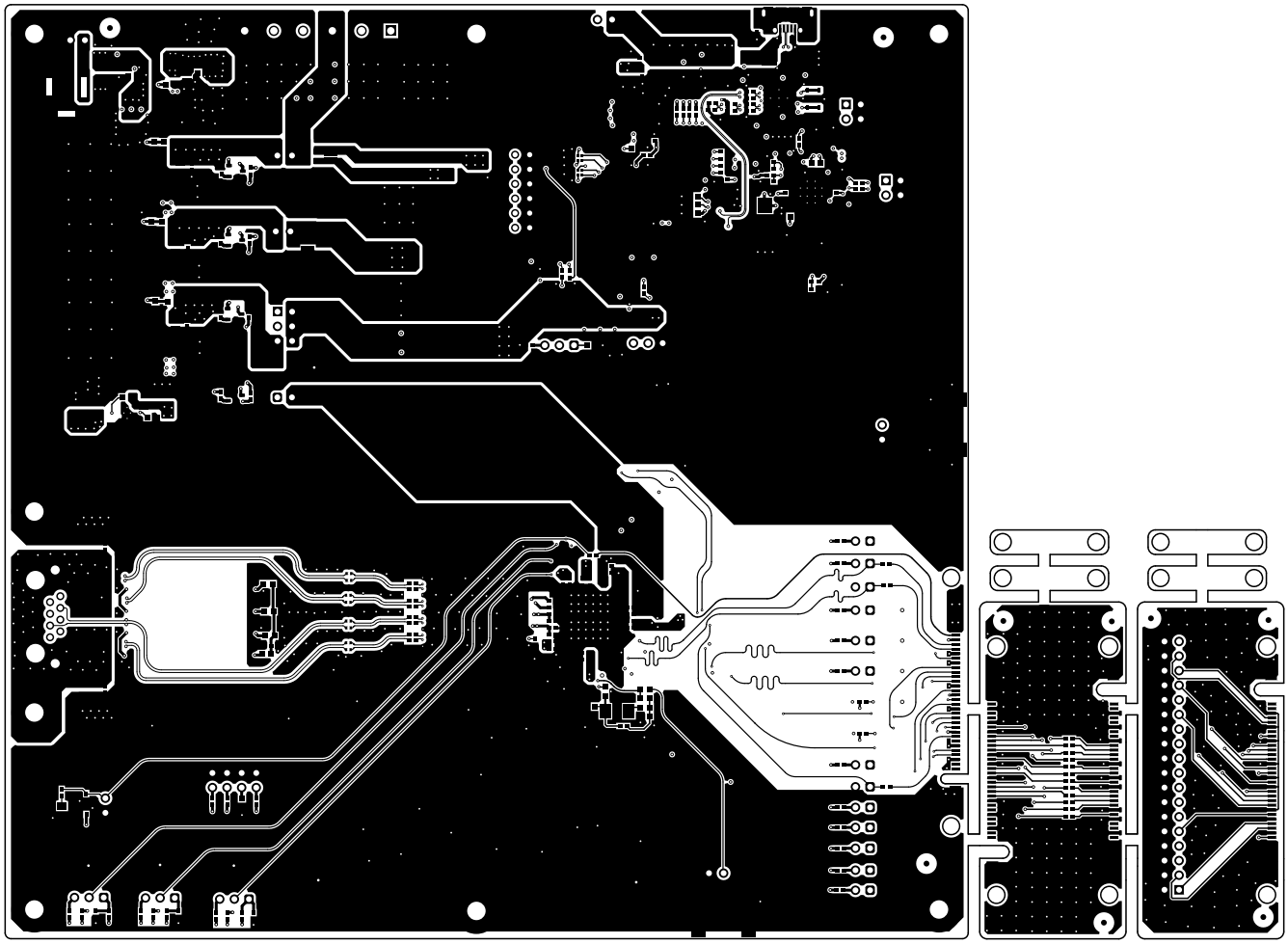

Figure 9-8. Bottom Layer

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9.9 Bottom Layer Mask

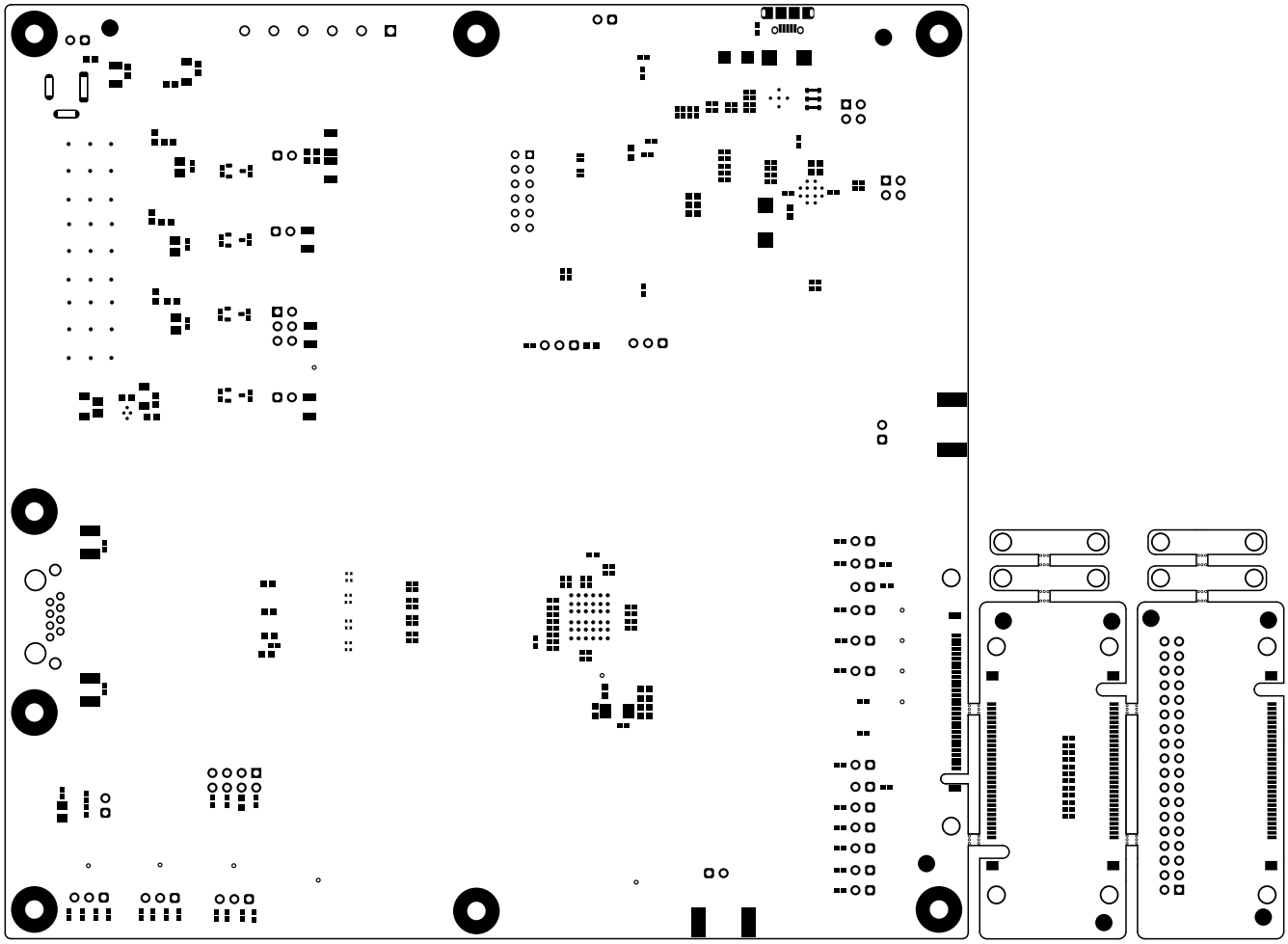

Figure 9-9. Bottom Layer Mask

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9.10 Bottom Overlay

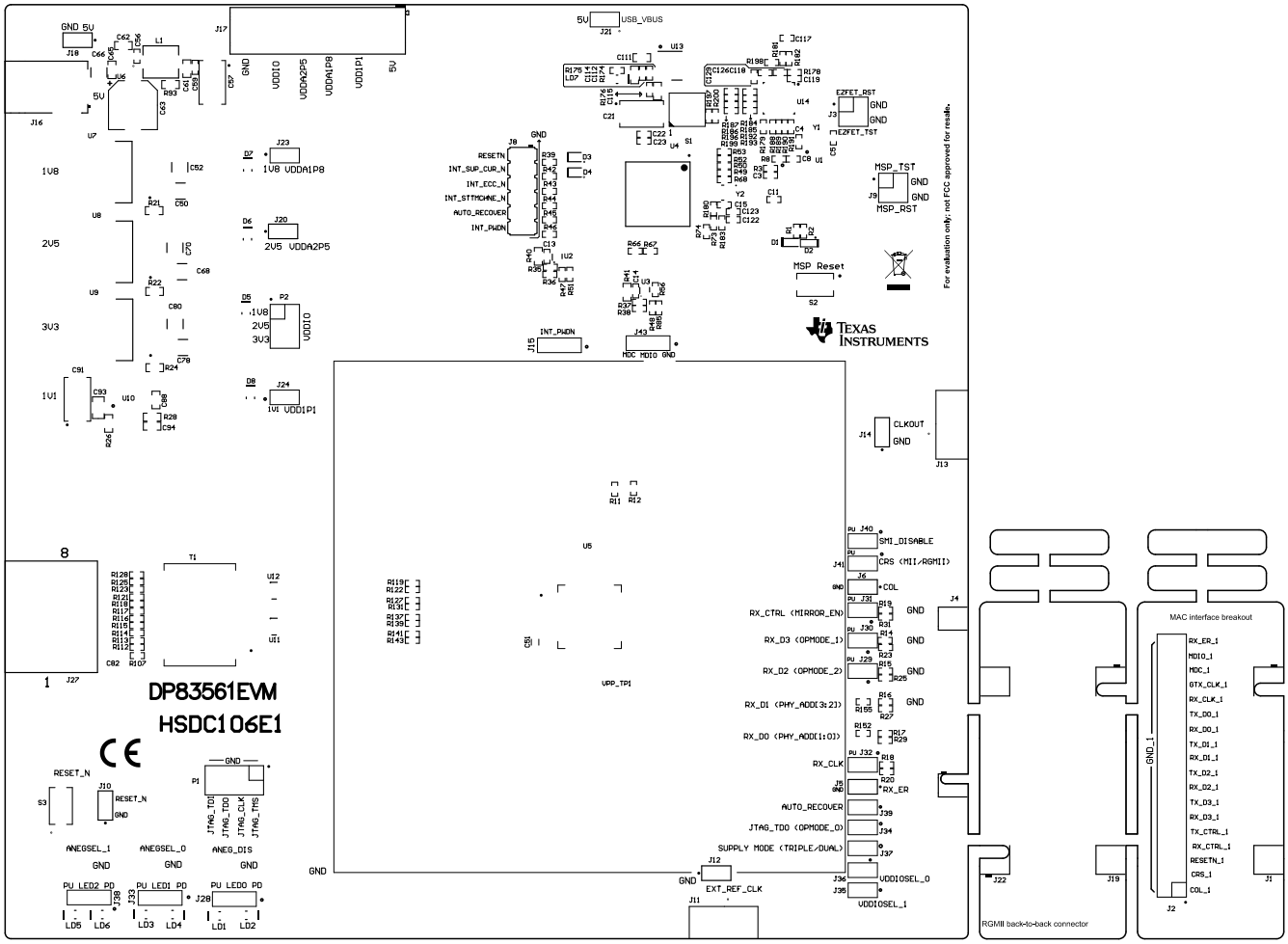

Figure 9-10. Bottom Overlay

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9.11 Board Assembly

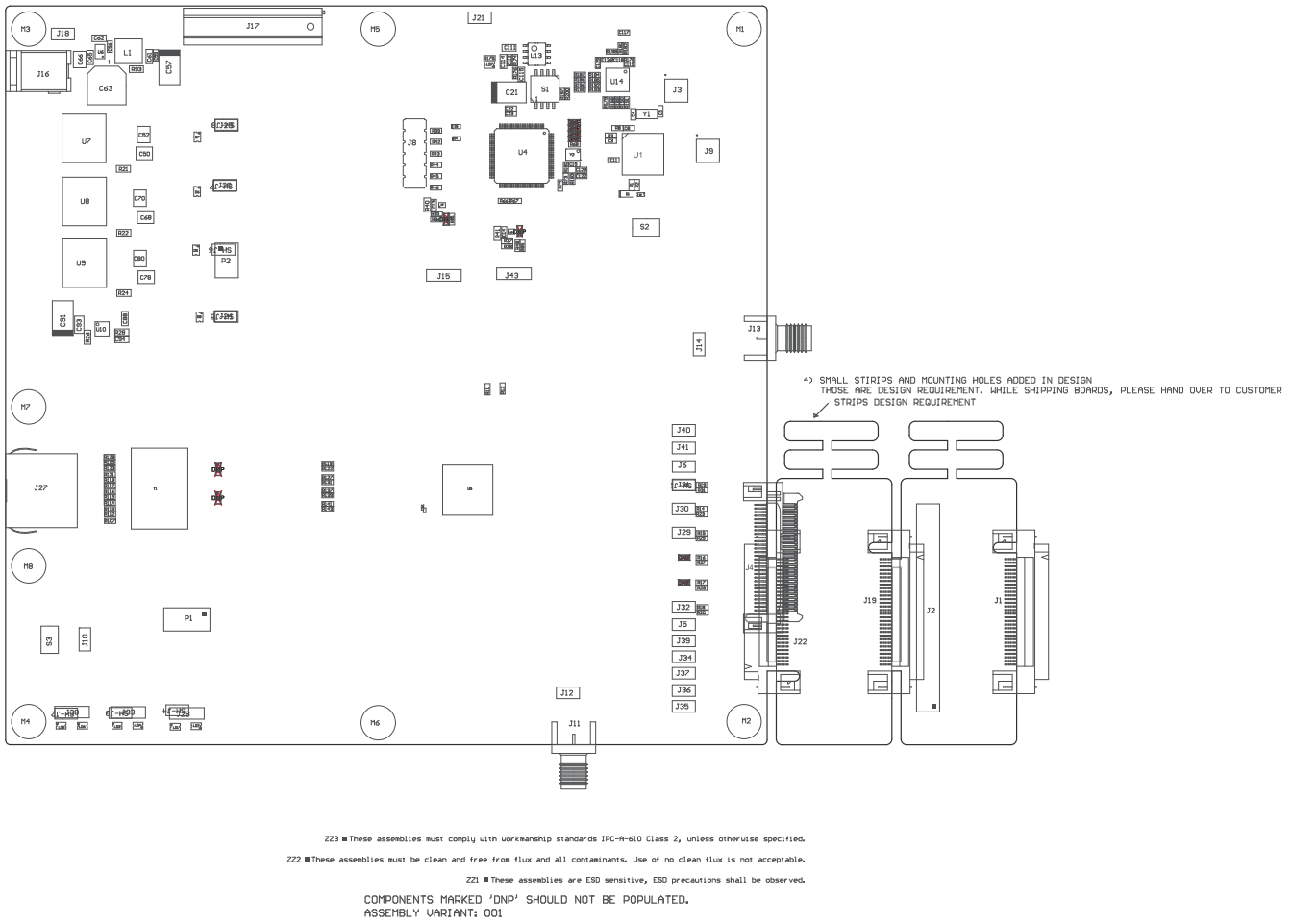

Figure 9-11. Top Assembly

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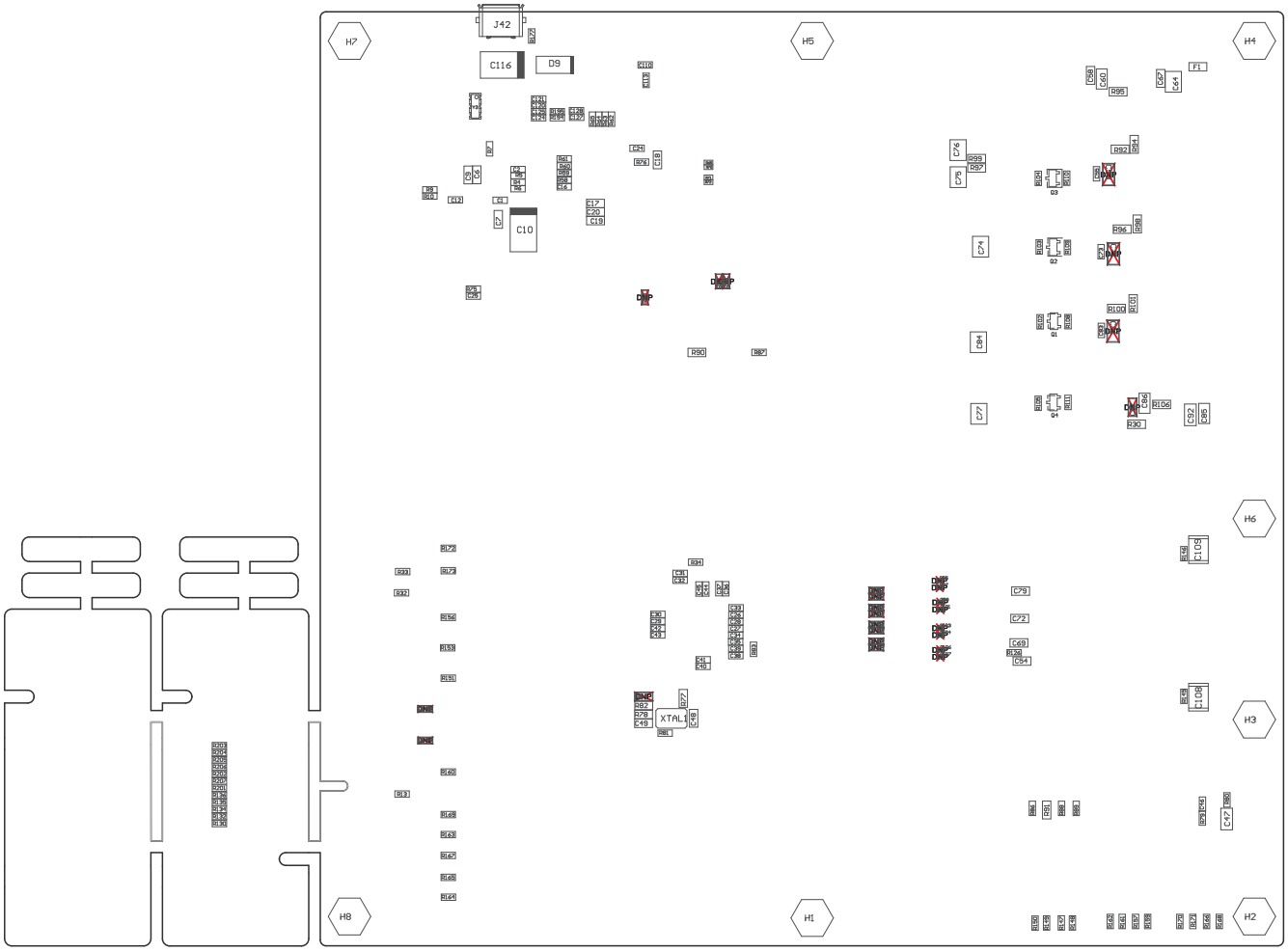

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: 001

Figure 9-12. Bottom Assembly

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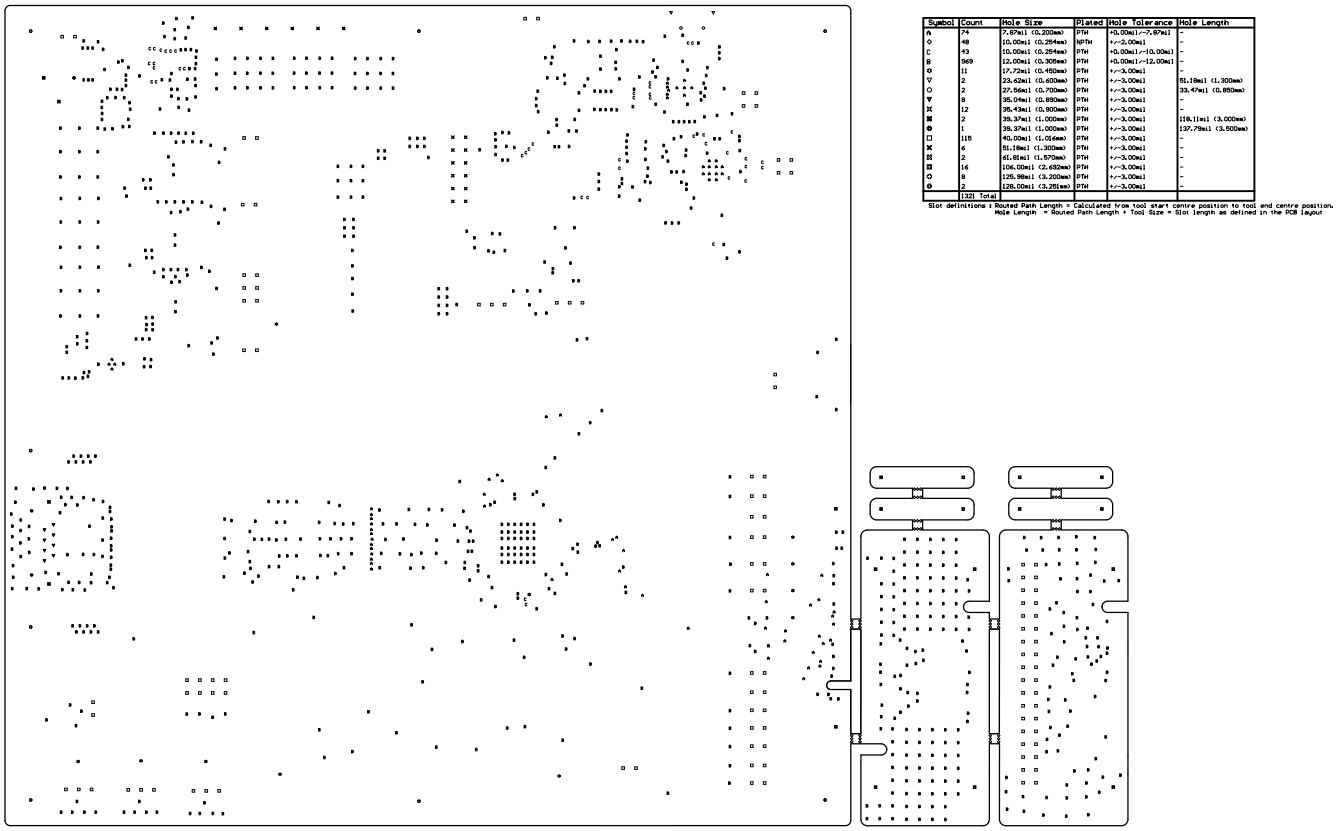

Figure 9-13. Drill Drawing

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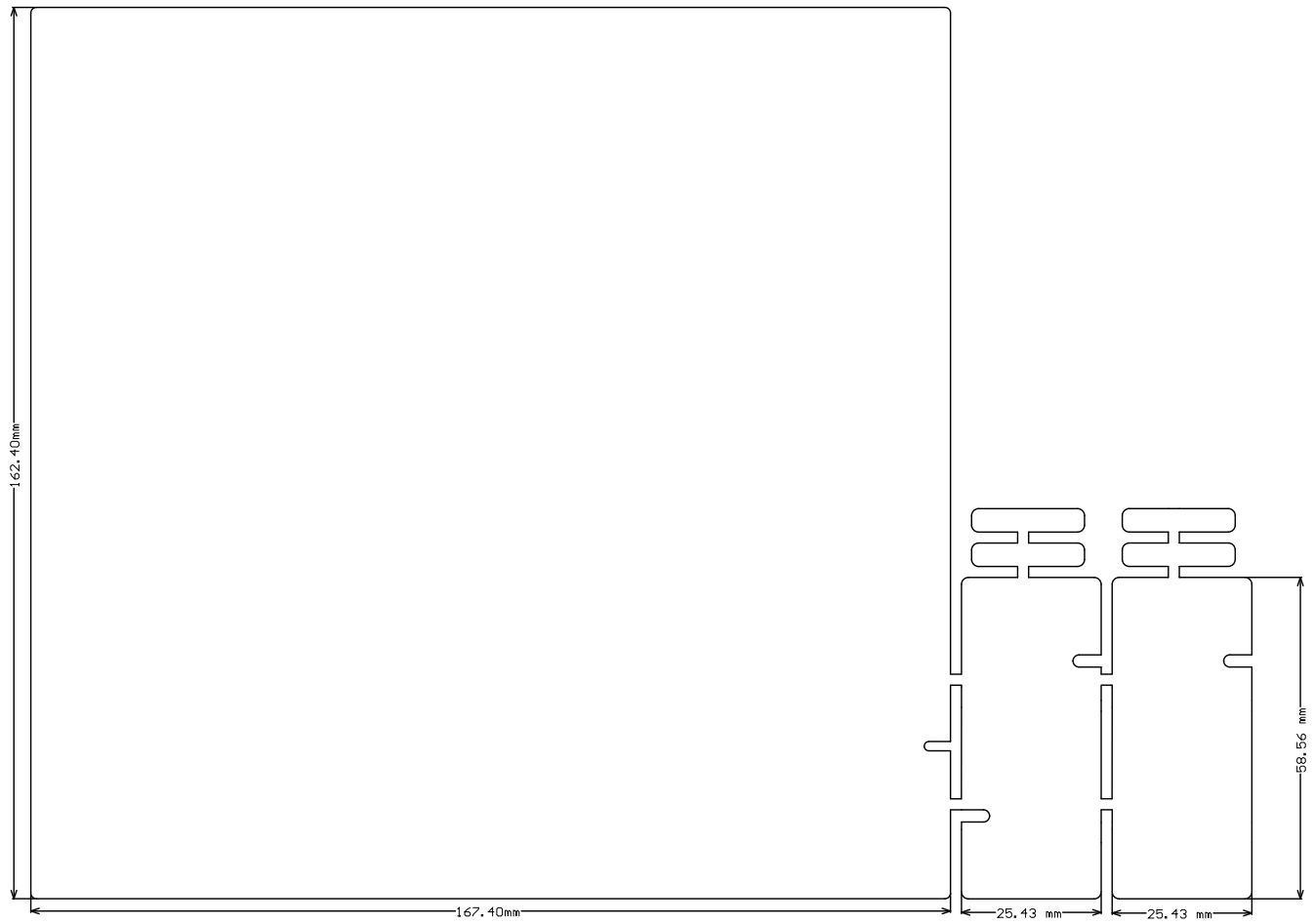

Figure 9-14. Board Dimensions

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10 Bill of Materials

Table 10-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C11, C12, C126, C129	5	0.1uF	CAP, CERM, 0.1 µF, 16 V,+/- 10%, X7R, 0402	0402	CL05B104KO5NNNC	Walsin
C2, C3	2	33pF	CAP, CERM, 33 pF, 25 V, +/- 5%, C0G/NP0, 0402	0402	885012005043	Wurth Elektronik
C4, C5, C15, C16	4	36pF	CAP, CERM, 36 pF, 50 V,+/- 5%, C0G/NP0, 0402	0402	CL05C360JB5NNNC	Samsung Electro-Mechanics
C6, C9	2	0.22uF	CAP, CERM, 0.22 µF, 50 V,+/- 10%, X5R, 0603	0603	CL10A224KB8NNNC	Samsung Electro-Mechanics
C7	1	0.47uF	CAP, CERM, 0.47 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7R1H474K080AB	TDK
C8, C25	2	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H102JA01D	MuRata
C10, C21	2	10uF	CAP, TA, 10 uF, 35 V, +/- 10%, 0.125 ohm, SMD	7343-31	TPSD106K035R0125	AVX
C13, C14, C56	3	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	GCM155R71H104KE02D	MuRata
C17, C20	2	0.22uF	CAP, CERM, 0.22 uF, 16 V, +80/-20%, Y5V, 0603	0603	C0603C224Z4VACTU	Kemet
C18	1	0.47uF	CAP, CERM, 0.47 uF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R71C474KA55D	MuRata
C19	1	4.7uF	CAP, CERM, 4.7 uF, 35 V, +/- 10%, X5R, 0603	0603	C1608X5R1V475K080AC	TDK
C22, C23, C24, C117	4	0.1uF	CAP, CERM, 0.1 µF, 10 V,+/- 10%, X7R, 0402	0402	C0402C104K8RACTU	Kemet
C26, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45	19	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	0402	C1005X5R1A104K050BA	TDK
C27	1	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X5R, 0402	0402	EMK105BJ105KVHF	Taiyo Yuden
C46	1	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H103KA88D	MuRata
C47	1	47uF	CAP, CERM, 47 µF, 4 V,+/- 20%, X6S, 0805	0805	GRM21BC80G476ME15L	MuRata
C48, C49, C94	3	27pF	CAP, CERM, 27 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603	CL10C270FB8NNNC	Samsung Electro-Mechanics
C50, C52, C68, C70, C78, C80	6	10uF	CAP, CERM, 10 uF, 25 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	1210	CGA6P1X7R1E106M250AC	TDK

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Table 10-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C51	1	47pF	Ceramic Capacitor for Automotive 47pF ±1% 50VDC C0G 0402 Paper T/R	0402	GCM1555C1H470FA16D	Murata
C53, C71, C81	3	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X5R, 0805	0805	0805YD105KAT2A	AVX
C54, C58, C61, C69, C72, C79, C88	7	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
C55, C73, C83	3	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H103K050BB	TDK
C57	1	220uF	CAP, TA, 220 µF, 6.3 V, +/- 10%, 0.7 ohm, SMD	7343-31	T491D227K006AT	Kemet
C59	1	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	CC0402JRNPO9BN101	Yageo America
C60, C85, C86	3	10uF	CAP, CERM, 10 µF, 35 V, +/- 20%, X7R, 1206_190	1206_190	C3216X7R1V106M160AC	TDK
C62	1	1uF	CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1V105K080AC	TDK
C63	1	100uF	CAP, AL, 100 uF, 50 V, +/- 20%, SMD	HA0	EMVE500ADA101MHA0G	Chemi-Con
C64, C66	2	4.7uF	CAP, CERM, 4.7 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1210	1210	CGA6P3X7R1H475K250AB	TDK
C65, C67	2	0.22uF	CAP, CERM, 0.22 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7R1H224K080AB	TDK
C74, C75, C76, C77, C84	5	22uF	CAP, CERM, 22 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	1210	CGA6P1X7R1C226M250AC	TDK
C82	1	0.01uF	CAP, CERM, 0.01 µF, 50 V, +/- 5%, X7R, 0402	0402	C0402C103J5RACTU	Kemet
C91	1	100uF	CAP, TA, 100 uF, 10 V, +/- 20%, 0.1 ohm, SMD	7343-31	593D107X0010D2TE3	Vishay-Sprague
C92	1	1uF	CAP, CERM, 1 µF, 16 V, +/- 10%, X5R, 0805	0805	0805YD105KAT2A	AVX
C93	1	4.7uF	CAP, CERM, 4.7 µF, 10 V, +80/-20%, Y5V, 0805	0805	CC0805ZRY5V6BB475	Yageo America
C95, C97, C99, C101, C103, C104, C106, C107	8	33nF	Cap Ceramic 33nF 16V X5R 10% Pad SMD 0402 +85°C Automotive T/R	0402	CGA2B2X5R1C333K050BA	TDK Corporation
C108, C109	2	4700pF	CAP, CERM, 4700 pF, 2000 V, +/- 10%, X7R, 1812	1812	1812GC472KAT1A	AVX
C110	1	1uF	CAP, CERM, 1 uF, 35 V, +/- 20%, X5R, 0402	0402	GRM155R6YA105ME11D	MuRata
C111, C114	2	10uF	CAP, CERM, 10 uF, 35 V, +/- 20%, X5R, 0603	0603	GRM188R6YA106MA73D	Murata
C112, C113	2	2.2uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X6S, 0402	0402	GRM155C81C225KE11D	MuRata
C115	1	470pF	CAP, CERM, 470 pF, 100 V, +/- 5%, X7R, 0603	0603	06031C471JAT2A	AVX
C116	1	4.7uF	CAP, TA, 4.7 uF, 35 V, +/- 10%, 1.3 ohm, SMD	7343-31	293D475X9035D2TE3	Vishay-Sprague

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Table 10-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C118, C119, C120, C121, C124, C125	6	22pF	CAP, CERM, 22 pF, 50 V,+/- 5%, C0G/NP0, 0402	0402	C1005NP01H220J050BA	TDK
C122, C123, C127, C128	4	10pF	CAP, CERM, 10 pF, 16 V,+/- 10%, C0G, 0402	0402	C0402C100K4GACTU	Kemet
D1	1	Red	LED, Red, SMD	LED_0603	150060RS75000	Wurth Elektronik
D2	1	Green	LED, Green, SMD	1.6x0.8mm	150060VS55040	Wurth Elektronik
D3, D4	2	Rg	LED, Rg, SMD	1.6x0.8mm	HSMF-C165	Avago
D5, D6, D7, D8, LD1, LD2, LD3, LD4, LD5, LD6, LD7	11	Green	LED, Green, SMD	2x1.25mm	QTLP630C4TR	Everlight
D9	1	60V	Diode, Schottky, 60 V, 3 A, AEC-Q101, SMA	SMA	SSA36	Fairchild Semiconductor
F1	1		Fuse, 3 A, 32 VDC, SMD	0603	F0603E3R00FSTR	AVX
FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8, FID9, FID10, FID11, FID12, FID13, FID14, FID15, FID16, FID17, FID18	18		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4, H5, H6, H7, H8	8		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J19, J22	3		Receptacle, 0.8mm, 30x2, Gold, Edge Mount	Receptacle, 0.8mm, 30x2, Edge Mount	ERF8-030-01-L-D-EM2-TR	Samtec
J2	1		Header, 100mil, 18x2, Gold, TH	18x2 Header	TSW-118-07-G-D	Samtec
J3, J9	2		Header, 100mil, 2x2, Gold, TH	2x2 Header	TSW-102-07-G-D	Samtec
J4	1		Receptacle, 0.8mm, 30x2, Tin, Edge mount	Receptacle, 0.8mm, 30x2, Edge mount	ERM8-030-01-L-D-EM2-TR	Samtec
J5, J6, J10, J12, J14, J18, J20, J21, J23, J24, J29, J30, J31, J32, J34, J35, J36, J37, J39, J40, J41	21		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J8	1		Header, 2.54 mm, 6x2, Gold, TH	Header, 2.54 mm, 6x2, TH	802-10-012-10-001000	Mill-Max
J11, J13	2		Connector, End launch SMA, 50 ohm, SMT	SMA End Launch	142-0701-851	Cinch Connectivity
J15, J28, J33, J38, J43	5		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J16	1		DC POWER JACK, R/A, TH	DC POWER JACK, R/A, TH	PJ-002AH	CUI Inc.

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Table 10-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
J17	1		Terminal Block, 6x1, 5.08mm, Th	Terminal Block, 6x1, 5.08mm, TH	1729160	Phoenix Contact
J27	1		RJ-45, Right Angle, No LED, tab up	16.26x14.54x15.75	1-406541-1	AMP
J42	1		Connector, Receptacle, Micro-USB Type AB, R/A, Bottom Mount SMT	5.6x2.5x8.2mm	475890001	Molex
L1	1	10uH	Inductor, Shielded, Ferrite, 10 uH, 2.75 A, 0.128 ohm, SMD	Inductor, 5.7x2.8x5.2mm	SRP5030T-100M	Bourns
M1, M2, M3, M4, M5, M6, M7, M8	8		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
P1	1		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec
P2	1		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec
Q1, Q2, Q3, Q4	4	60 V	Transistor, NPN, 60 V, 1 A, AEC-Q101, SOT-23	SOT-23	DNBT8105-7	Diodes Inc.
R1, R2, R79, R102, R103, R104, R105, R147, R149, R157, R161, R166, R170, R175	14	470	RES, 470, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402470RJNED	Vishay-Dale
R3	1	240k	RES, 240 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402240KJNED	Vishay-Dale
R4, R6	2	220k	RES, 220 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402220KJNED	Vishay-Dale
R5	1	150k	RES, 150 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402150KJNED	Vishay-Dale
R7, R9, R10	3	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America
R8, R75, R198	3	47k	RES, 47 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040247K0JNED	Vishay-Dale

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Table 10-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R23, R25, R27, R29, R31, R32, R33, R34, R39, R42, R43, R44, R45, R46, R112, R113, R115, R116, R118, R119, R121, R122, R125, R126, R127, R128, R130, R131, R132, R134, R135, R136, R137, R139, R141, R143, R201, R202, R203, R204, R205, R206, R207	53	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R21, R22, R24, R26, R77, R78, R82, R97, R99	9	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R28	1	1.87k	RES, 1.87 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K87L	Yageo
R30	1	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	0603	CRCW06034K99FKEAC	Vishay-Dale
R35, R37	2	374k	RES, 374 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402374KFKED	Vishay-Dale
R36, R38	2	1.00Meg	RES, 1.00 M, 1%, 0.1 W, 0402	0402	ERJ-2RKF1004X	Panasonic
R40, R41	2	200k	RES, 200 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603200KJNEA	Vishay-Dale
R48, R51, R62, R63, R64, R65, R66, R67	8	2.20k	RES, 2.20 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20FKED	Vishay-Dale
R58, R59, R60, R61, R179	5	10k	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0JNED	Vishay-Dale
R68, R76	2	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R69, R70, R71, R72	4	470	RES, 470, 5%, 0.05 W, 0201	0201	RC0201JR-07470RL	Yageo America
R73, R197	2	1.40k	RES, 1.40 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K40FKED	Vishay-Dale
R74, R200	2	1.00Meg	RES, 1.00 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021M00FKED	Vishay-Dale
R80	1	100	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GEJ101X	Panasonic

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Table 10-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R81, R145, R146	3	1.00Meg	RES, 1.00 M, 1%, 0.063 W, 0402	0402	RC0402FR-071ML	Yageo America
R83	1	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT10K0	Stackpole Electronics Inc
R85, R86, R87, R88, R89	5	2.2k	RES, 2.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20JNED	Vishay-Dale
R90	1	6.04k	RES, 6.04 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K04L	Yageo
R91	1	6.04k	RES, 6.04 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06036K04FKEA	Vishay-Dale
R92	1	1.20k	RES, 1.20 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K2L	Yageo
R93	1	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R94, R98, R101	3	2.40k	RES, 2.40 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA-3AEB242V	Panasonic
R95	1	24.9k	RES, 24.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060324K9FKEA	Vishay-Dale
R96	1	2.55k	RES, 2.55 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K55L	Yageo
R100	1	4.22k	RES, 4.22 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K22FKEA	Vishay-Dale
R106	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R107, R114, R117, R123	4	75.0	RES, 75.0, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040275R0FKED	Vishay-Dale
R108, R109, R110, R111, R148, R150, R151, R153, R156, R159, R160, R162, R163, R164, R165, R167, R168, R169, R171, R172, R173	21	2.49k	RES, 2.49 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K49FKED	Vishay-Dale
R174	1	100k	RES, 100 k, 0.5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100KDHEDP	Vishay-Dale
R176	1	165k	RES, 165 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402165KFKED	Vishay-Dale
R177	1	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040233R0JNED	Vishay-Dale
R178	1	1.50k	RES, 1.50 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K50FKED	Vishay-Dale
R180, R183, R196, R199	4	27	RES, 27, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040227R0JNED	Vishay-Dale
R181, R182, R184, R185, R192, R193	6	22	RES, 22, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040222R0JNED	Vishay-Dale

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Table 10-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R186, R187, R188, R189, R190, R191, R194, R195	8	15.0k	RES, 15.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040215K0FKED	Vishay-Dale
S1	1		Switch, Slide, SPST 4 poles, SMT	SW, SMT Half Pitch 4SPST, 5.8x2.7x6.25 mm	218-4LPST	CTS Electrocomponents
S2, S3	2		Switch, Normally open, 2.3N force, 200k operations, SMD	KSR	KSR221GLFS	C&K Components
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	8		Single Operation 2.54mm Pitch Open Top Jumper Socket	Single Operation 2.54mm Pitch Open Top Jumper Socket	M7582-05	Harwin
U1	1		16-Bit Ultra-Low-Power Microcontroller, 128KB Flash, 8KB RAM, USB, 12Bit ADC, 2 USCIs, 32Bit HW MPY, RGC0064B (VQFN-64)	RGC0064B	MSP430F5528IRGCR	Texas Instruments
U2, U3	2		Dual Bidirectional Multi-Voltage Level Translator, DQE0008A (X2SON-8)	DQE0008A	LSF0102DQER	Texas Instruments
U4	1		25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	PN0080A	MSP430F5529IPN	Texas Instruments
U5	1		Hi-Reliability, High Immunity, Radiation Resistant, Gigabit Ethernet PHY	CFP64	DP83561HBE-EM	Texas Instruments
U6	1		3.8-V to 36-V 2-A Synchronous Step-Down Voltage Regulator, RNX0012B (VQFN-HR-12)	RNX0012B	LMR33620ARNXT	Texas Instruments
U7, U8, U9	3		Single Output Fast Transient Response LDO, 1.5 A, Adjustable 1.21 to 20 V Output, 2.1 to 20 V Input, 5-pin DDPAK (KTT), -40 to 125 degC, Green (RoHS & no Sb/Br)	KTT0005A	TL1963AQKTTRQ1	Texas Instruments
U10	1		Single Output LDO, 500mA, Adj. (0.8 to 3.6V), Programmable Soft-Start, DRC0010J (VSON-10)	DRC0010J	TPS74701DRCR	Texas Instruments
U13	1		Single Output Low Noise LDO, 500 mA, Adjustable 1.3 to 6.5 V Output, 2.5 to 16 V Input, 8-pin SOIC (D), -40 to 125 degC, Green (RoHS & no Sb/Br)	D0008A	TL5209DR	Texas Instruments
U14	1		4-Port Full-Speed USB Hub, 3.3V, -40 to 85 degC, 32-Pin QFN (RHB), Green (RoHS & no Sb/Br)	RHB0032E	TUSB2046BIRHBT	Texas Instruments
XTAL1	1		Crystal, 25 MHz, 18 pF, SMD	ABM3	ABM3-25.000MHZ-D2Y-T	Abracon Corporation
Y1	1		Oscillator, 4 MHz, 700 ppm, 39 pF, SMD	4.5x2mm	CSTNR4M00GH5L000R0	MuRata
Y2	1		Crystal, 24 MHz, 20pF, SMD	3.2x2.5mm	ECS-240-20-33-DU-TR	ECS Inc.

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Table 10-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
Y3	1		Resonator, 6 MHz, 15pF SMD	4.5x1.2x2 mm	CSTCR6M00G53Z-R0	MuRata
C87	0	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	0603	CL10B104KO8NNNC	Samsung Electro-Mechanics
R47	0	2.20k	RES, 2.20 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20FKED	Vishay-Dale
R49, R50, R52, R53	0	10k	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0JNED	Vishay-Dale
R54, R55, R56, R57, R120, R124, R129, R133, R138, R140, R142, R144	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R84	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R152, R155	0	6.04k	RES, 6.04 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04026K04FKED	Vishay-Dale
R154, R158	0	2.49k	RES, 2.49 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K49FKED	Vishay-Dale
T1	0		350µH LAN 10/100/1000 Base-T Pulse Transformer 1:1 Surface Mount	SMD24	1000B-5001X	Pulse Electronics
U11, U12	0		4-Channel Ultra-Low-Capacitance IEC ESD Protection Diode, DQA0010A (USON-10)	DQA0010A	TPD4E05U06DQAR	Texas Instruments

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11 REACH Compliance

In compliance with the Article 33 provision of the EU REACH regulation we are notifying you that this EVM includes component(s) containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are found in Table 11-1:

Table 11-1. REACH Compliance SVHC's

Component Manufacturer	Component Type	Component Part Number	SVHC Substance	SVHC CAS (when available)
Murata	Resonant Ceramic Element	CSTCR6M00G53Z-R0	Lead Titanium Zirconium Oxide	16626-81-2
Murata	Resonant Ceramic Element	CSTNR4M00GH5L000R0	Lead Titanium Zirconium Oxide	12626-81-2

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2021	*	Initial Release

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STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

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