

FEATURES/BENEFITS

- Function compatible to the 74F377, 74FCT377 and 74ABT377
- CMOS power levels: <15mW static
- Undershoot clamp diodes on all inputs
- Fastest CMOS logic family available
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in 40-pin 0.4mm pitch QVSOP (Q2)
- A and C speed grades with 5.2ns t_{PD} for C
- $I_{OL} = 48\text{mA Ind.}$

DESCRIPTION

The QS74FCT2X377 is a high-speed 16-bit CMOS TTL-compatible register. It includes a buffered clock, a buffered output drive, and a synchronous clock enable. Data is stored in the register on the rising edge of the clock if the clock enable input is active. The high-output current I_{OL} and I_{OH} drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

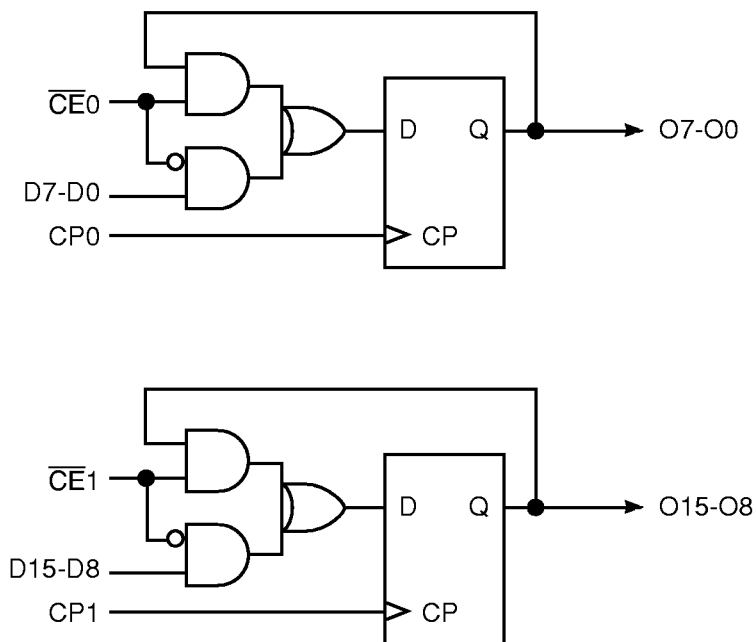


Figure 2. Pin Configuration (All Pins Top View)

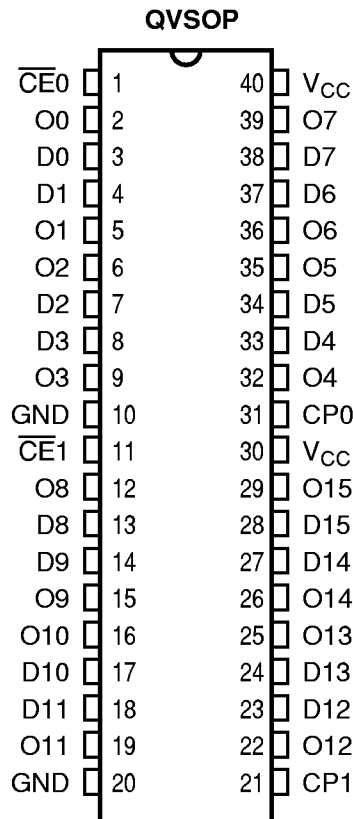


Table 1. Pin Description

Name	I/O	Description
D _i	I	Data Inputs
O _i	O	Data Outputs
CP _i	I	Clock Input
\overline{CE}_i	I	Clock Enable

Table 2. Function Table

\overline{CE}_i	Inputs CP _i	D _i	Internal Q Value	Outputs O _i	Function
H	X	X	NC	NC	Hold Value
L	↑	L	L	L	Load Input Data
L	↑	H	H	H	

Note:

$\overline{CE}0$, CP0 control bits 7-0

$\overline{CE}1$, CP1 control bits 15-8

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_{OUT}	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20mA
DC Output Diode Current with $V_{OUT} < 0$	-50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	1.2 watts
T_{STG} Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Capacitance

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	Typ	Unit
1-9, 11-19, 21, 31	4	pF
22-29, 32-39	6	pF

Note: Capacitance is characterized but not tested.

Table 5. DC Electrical Characteristics Over Operating Range

Industrial: $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs ⁽³⁾	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}$, $0 \leq V_{IN} < V_{CC}$	—	—	5	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$, $0 \leq V_{IN} \leq V_{CC}$	—	—	5	μA
I_{OS}	Short Circuit Current FCT2X374	$V_{CC} = \text{Max.}$, $V_{OUT} = \text{GND}$ ^(2,3)	-60	—	-225	mA
I_{OR}	Current Drive FCT2X2374 (25 Ω)	$V_{CC} = \text{Max.}$, $V_{OUT} = 2.0\text{V}$	50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$ ⁽³⁾	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $I_{OH} = -15\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage FCT2X374	$V_{CC} = \text{Min.}$, $I_{OL} = 64\text{mA}$	—	—	0.55	V
V_{OL}	Output LOW Voltage FCT2X2374 (25 Ω)	$V_{CC} = \text{Min.}$, $I_{OL} = 12\text{mA}$	—	—	0.50	V
R_{OUT}	Output Resistance FCT2X2374 (25 Ω)	$V_{CC} = \text{Min.}$, $I_{OL} = 12\text{mA}$	20	28	40	Ω

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

Table 6. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, \text{Freq} = 0$ $0V \leq V_{IN} \leq 0.2V$ or $V_{CC}-0.2V \leq V_{IN} \leq V_{CC}$	—	3.0	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4V, \text{Freq} = 0^{(2)}$	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}, \text{Outputs Open and Enabled}$ One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/ MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4V$).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 7. Switching Characteristics Over Operating Range

Industrial: $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0V \pm 5\%$
 $C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description	2X374A 2X2374A		2X374C 2X2374C		Unit
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay ⁽¹⁾ CP to Oi	2.0	6.5	2.0	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time ⁽¹⁾ FCT2X374	1.5	6.5	1.5	5.5	ns
t_{PZH} t_{PZL}	Output Enable Time ⁽¹⁾ FCT2X2374	1.5	6.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time ⁽²⁾	1.5	5.5	1.5	5.0	ns
t_S	Data Setup Time	2.0	—	1.5	—	ns
t_H	Data Hold Time	1.5	—	1.0	—	ns
t_W	Clock Pulse Width ⁽²⁾ HIGH or LOW	5.0	—	4.0	—	ns

Notes:

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. This parameter is guaranteed but not tested.