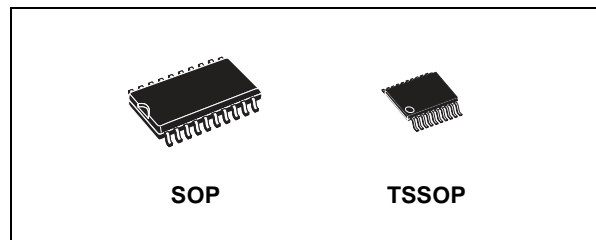




# 74VHC240

## OCTAL BUS BUFFER WITH 3 STATE OUTPUTS (INVERTED)

- HIGH SPEED:  $t_{PD} = 3.6ns$  (TYP.) at  $V_{CC} = 5V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu A$  (MAX.) at  $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8 mA$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}(OPR) = 2V$  to  $5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 240
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE:  $V_{OLP} = 0.9V$  (MAX.)



### ORDER CODES

PACKAGE	TUBE	T & R
SOP	74VHC240M	74VHC240MTR
TSSOP		74VHC240TTR

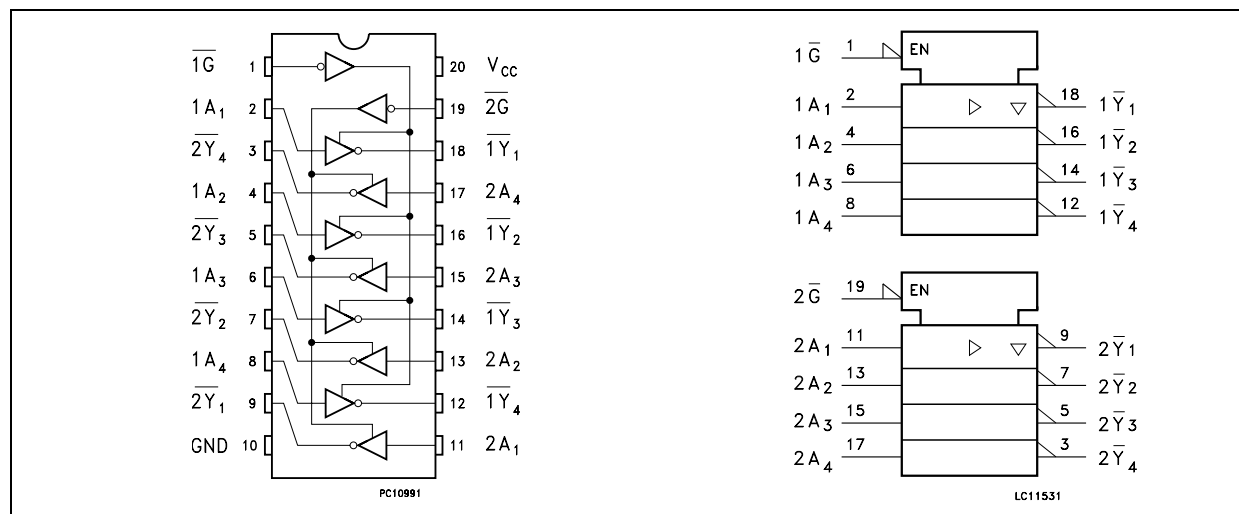
### DESCRIPTION

The 74VHC240 is an advanced high-speed CMOS OCTAL BUS BUFFER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.  $\overline{G}$  output enable governs four BUS BUFFERS. This device is designed to be used with 3 state memory address drivers, etc.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS





## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0 to 5.5		0.7V <sub>CC</sub>			0.7V <sub>CC</sub>		0.7V <sub>CC</sub>		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0 to 5.5				0.3V <sub>CC</sub>		0.3V <sub>CC</sub>		0.3V <sub>CC</sub>	
V <sub>OH</sub>	High Level Output Voltage	2.0	I <sub>O</sub> =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I <sub>O</sub> =-50 μA	2.9	3.0		2.9		2.9		
		4.5	I <sub>O</sub> =-50 μA	4.4	4.5		4.4		4.4		
		3.0	I <sub>O</sub> =-4 mA	2.58			2.48		2.4		
		4.5	I <sub>O</sub> =-8 mA	3.94			3.8		3.7		
V <sub>OL</sub>	Low Level Output Voltage	2.0	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	
		3.0	I <sub>O</sub> =4 mA			0.36		0.44		0.55	
		4.5	I <sub>O</sub> =8 mA			0.36		0.44		0.55	
I <sub>OZ</sub>	High Impedance Output Leakage Current	5.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND			±0.25		± 2.5		± 2.5	μA
I <sub>I</sub>	Input Leakage Current	0 to 5.5	V <sub>I</sub> = 5.5V or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		40	μA

AC ELECTRICAL CHARACTERISTICS (Input  $t_r = t_f = 3\text{ns}$ )

Symbol	Parameter	Test Condition			Value						Unit	
		$V_{CC}$ (V)	$C_L$ (pF)		$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time	3.3(*)	15			5.3	7.5	1.0	9.0	1.0	9.0	ns
		3.3(*)	50			7.8	11.0	1.0	12.5	1.0	12.5	
		5.0(**)	15			3.6	5.5	1.0	6.5	1.0	6.5	
		5.0(**)	50			5.1	7.5	1.0	8.5	1.0	8.5	
$t_{PZL}$ $t_{PZH}$	Output Enable Time	3.3(*)	15	$R_L = 1\text{K}\Omega$		6.6	10.6	1.0	12.5	1.0	12.5	ns
		3.3(*)	50	$R_L = 1\text{K}\Omega$		9.1	14.1	1.0	16.0	1.0	16.0	
		5.0(**)	15	$R_L = 1\text{K}\Omega$		4.7	7.3	1.0	8.5	1.0	8.5	
		5.0(**)	50	$R_L = 1\text{K}\Omega$		6.2	9.3	1.0	10.5	1.0	10.5	
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time	3.3(*)	50	$R_L = 1\text{K}\Omega$		10.3	14.0	1.0	16.0	1.0	16.0	ns
		5.0(**)	50	$R_L = 1\text{K}\Omega$		6.7	9.2	1.0	10.5	1.0	10.5	
$t_{OSLH}$ $t_{OSHL}$	Output to Output Skew time (note 1)	3.3(*)	50					1.5			1.5	ns
		5.0(**)	50					1.0			1.0	

(\*) Voltage range is  $3.3\text{V} \pm 0.3\text{V}$ (\*\*) Voltage range is  $5.0\text{V} \pm 0.5\text{V}$ Note 1 : Parameter guaranteed by design.  $t_{soLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{soHL} = |t_{pHLm} - t_{pHLn}|$ 

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition			Value						Unit	
					$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance					6	10		10		10	pF
$C_{OUT}$	Output Capacitance					8						pF
$C_{PD}$	Power Dissipation Capacitance (note 1)					17						pF

1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$  (per circuit)

## DYNAMIC SWITCHING CHARACTERISTICS

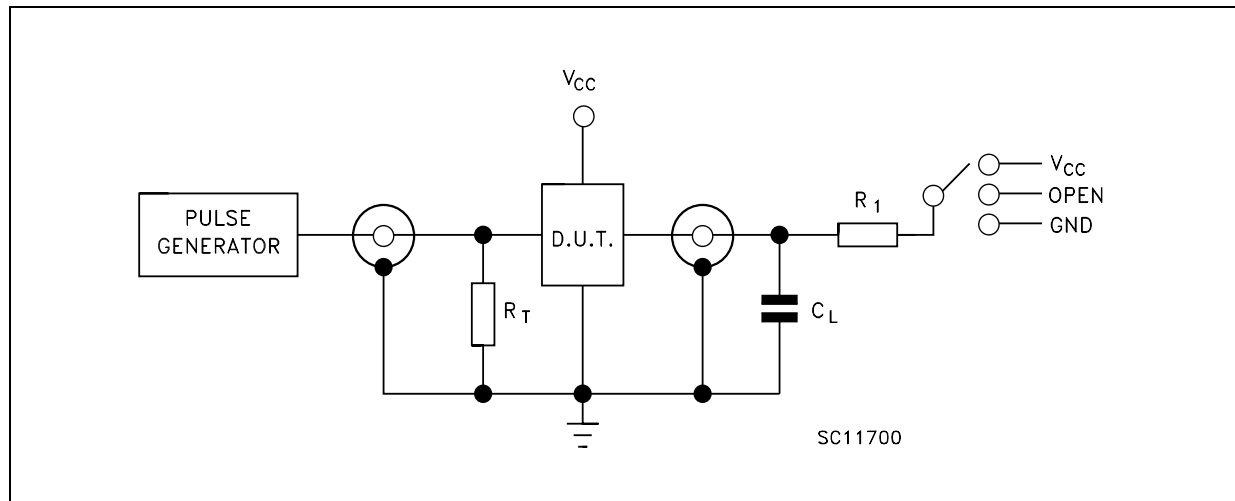
Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> = 50 pF	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C <sub>L</sub> = 50 pF		0.6	0.9					V
V <sub>OLV</sub>				-0.9	-0.6						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	5.0		3.5							V
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	5.0				1.5					V

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

## TEST CIRCUIT



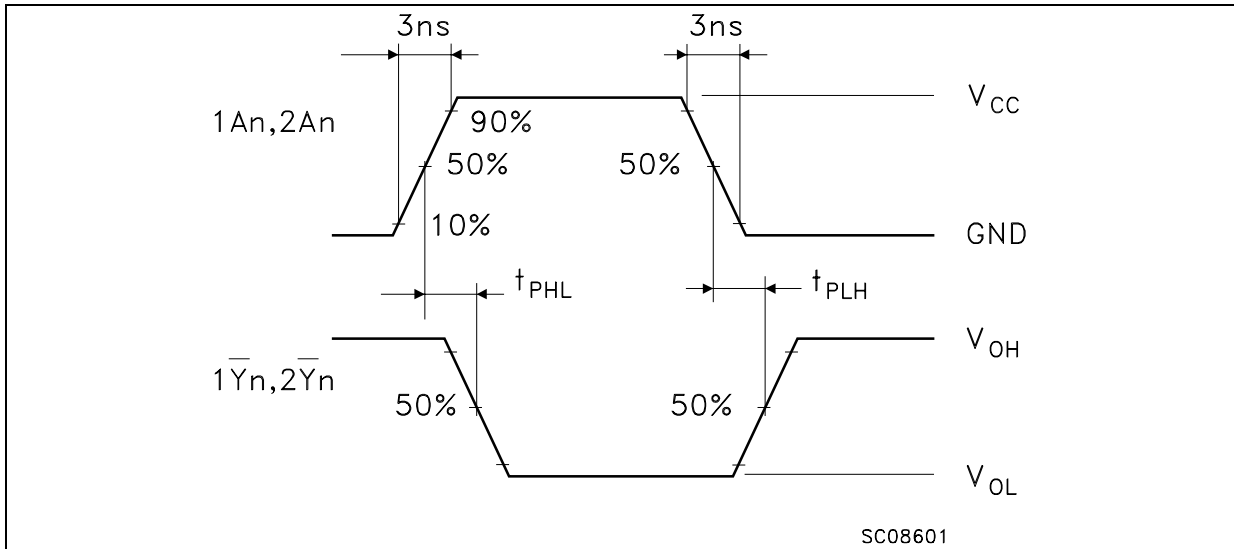
TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	V <sub>CC</sub>
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND

C<sub>L</sub> = 15/ 50pF or equivalent (includes jig and probe capacitance)

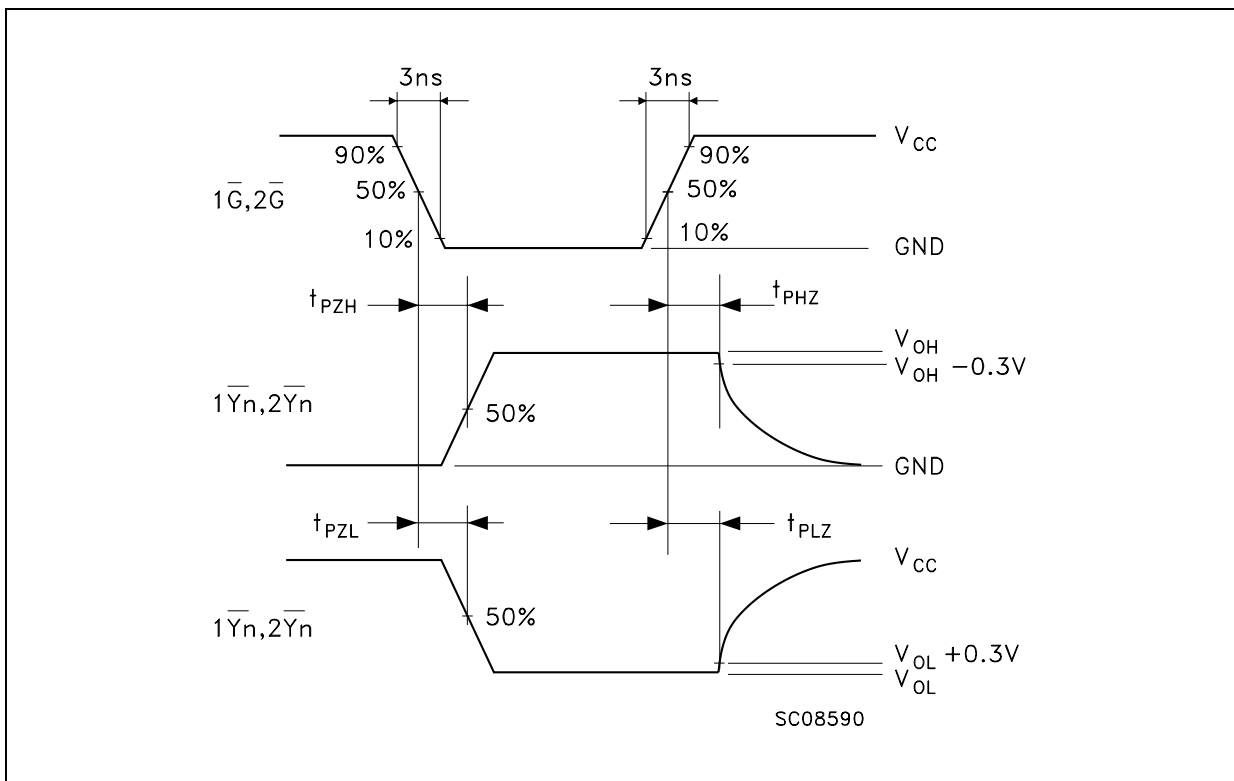
R<sub>L</sub> = R<sub>1</sub> = 1KΩ or equivalent

R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

WAVEFORM 1 : PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

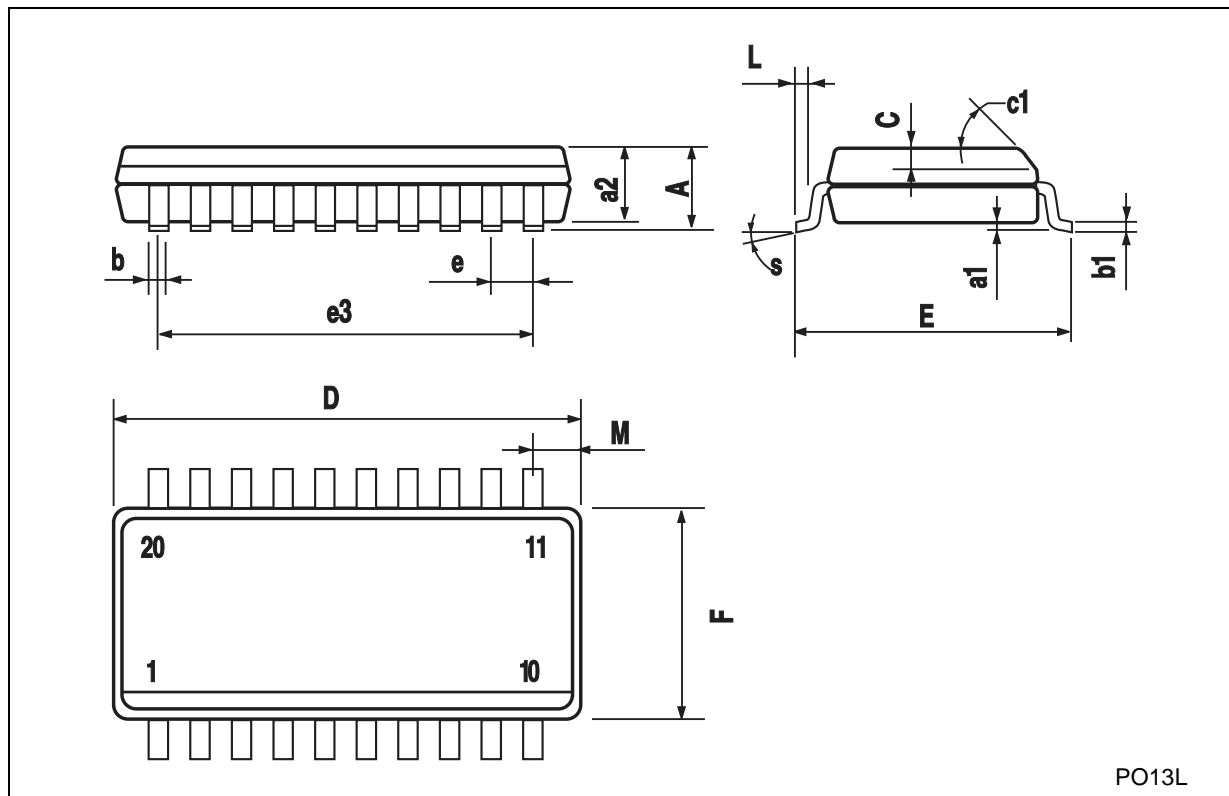


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



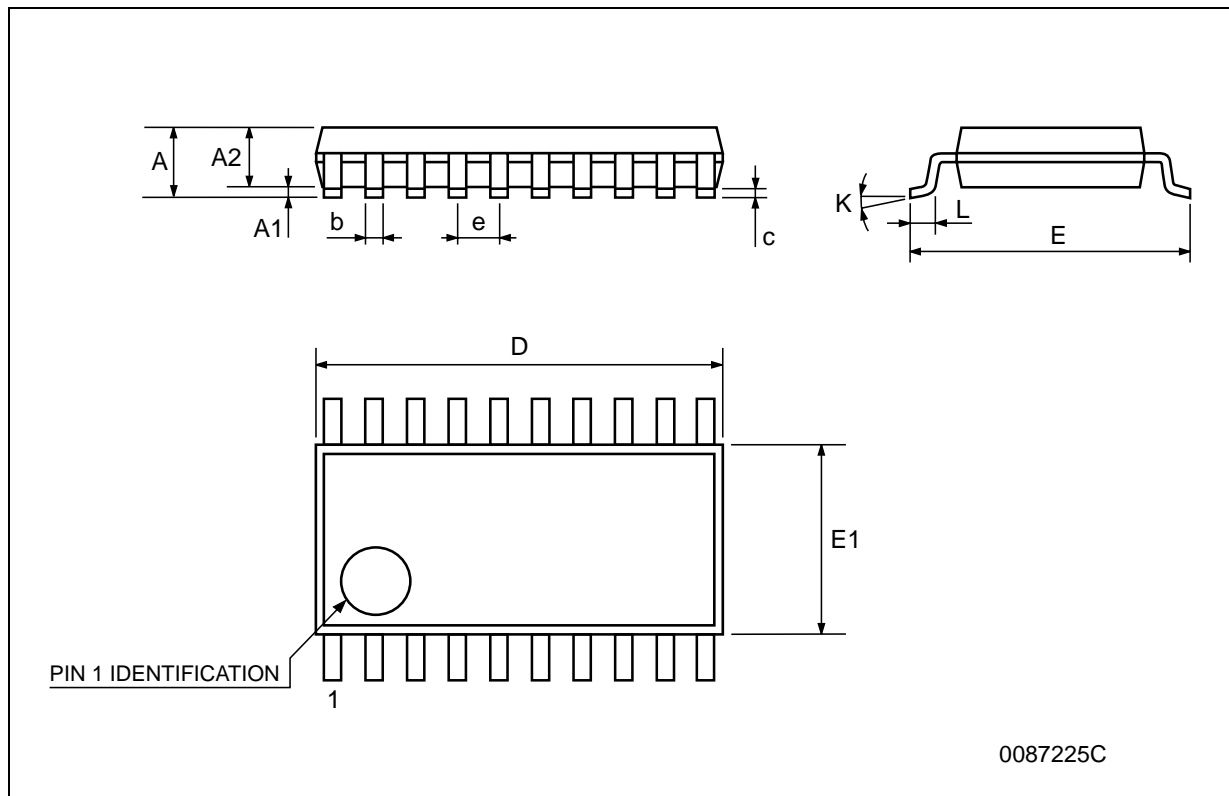
## SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



## TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030





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