AK4637

24bit Mono CODEC with MIC/SPK-AMP

1. General Description

The AK4637 is a low power 24-bit Mono CODEC with a microphone and speaker amplifiers.

The AK4637 supports sampling frequency from 8kHz to 48kHz. It is suitable for a wide range of application from speech signal processing for narrowband, wideband and super wideband to sound signal processing for audio band.

The input circuits include a microphone amplifier and a high performance digital ALC (automatic level control) circuit. In addition, the output circuits include a speaker amplifier with 1W output power. It is suitable for various products as well as portable applications with recording/playback function.

The AK4637 are available in a small 20-pin QFN (3mm x 3mm, 0.4mm pitch: AK4637EN) package saving mounting area on the board.

Application:

- **IP Camera**
- **Digital Camera**
- **MFP(Multi Function Printer)**

2. Features

1. **Recording Functions**
   - **Analog Input**
     1 Monaural Single-ended input or Differential input
   - **Microphone Amplifier: +30dB ~ 0dB, 3dB Step**
   - **Microphone Power Supply: 2.0V or 2.4V, Noise Level= –108dBV**
   - **Digital ALC (Automatic Level Control)**
     - Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute
   - **ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)**
     S/(N+D): 84dB, DR, S/N: 95dB (MIC-Amp=0dB)
   - **Wind Noise Reduction Filter**
   - **5-Band Notch Filter: Include Dynamic Gain Control**
   - **Digital Microphone Interface**
2. **Playback Functions**
   - **Digital ALC (Automatic Level Control)**
     - Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute
   - **Sidetone Mixer & Volume Control (0dB ~ –18dB, 6dB Step)**
   - **Digital Volume Control**
     - +12dB ~ –89.5dB, 0.5dB Step & Mute
   - **Mono Speaker Amplifier (with Line Output Switch)**
     - Speaker Amplifier Porformance: S/(N+D): 75dB@250mW, S/N: 97 dB
     - BTL Output
     - Output Power: 400mW@8Ω (AVDD=3.3V), 1W@8Ω (AVDD=5V)
   - **Analog Mixing: BEEP Input**
3. **Power Management**

4. Master Clock:
   (1) PLL Mode
   Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin), 16fs, 32fs, 64fs (BICK pin)
   (2) External Clock Mode
   Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)
5. Sampling Frequencies
   - PLL Master Mode:
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - PLL Slave Mode (BICK pin): 8kHz ~ 48kHz
   - EXT Master/Slave Mode:
     8kHz ~ 48kHz (256fs, 384fs, 512fs), 8kHz ~ 24kHz (1024fs)
6. Master/Slave Mode
7. Audio Interface Format: MSB First, 2's complement
   - ADC: DSP Mode, 16/24bit MSB justified, 16/24bit I^2S
   - DAC: DSP Mode, 16/24bit MSB justified, 16bit LSB justified, 16/24bit I^2S
8. μP I/F: I^2C Bus (Ver 1.0, 400kHz Fast-Mode)
9. Operating Temperature: Ta = –40 ~ 85°C
10. Power Supply
    - Analog Power Supply (AVDD): 2.8 ~ 5.5V
    - Digital Power Supply (DVDD): 1.6 ~ 1.98V
    - Digital I/O Power Supply (TVDD): 1.6 or (DVDD – 0.2) ~ 3.6V
11. Package:
    - 20-pin QFN (3 x 3 mm, 0.4mm pitch)

3. Table of Contents

4. Block Diagram

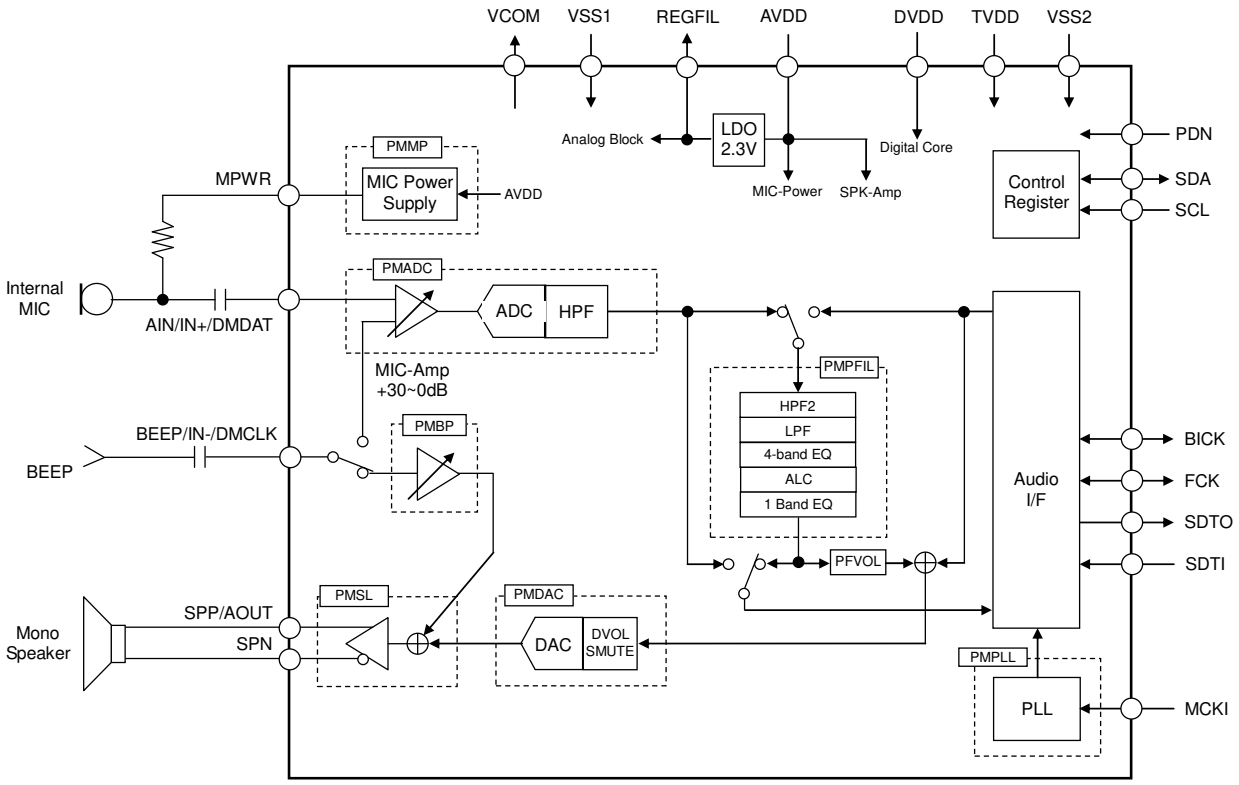


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Layout

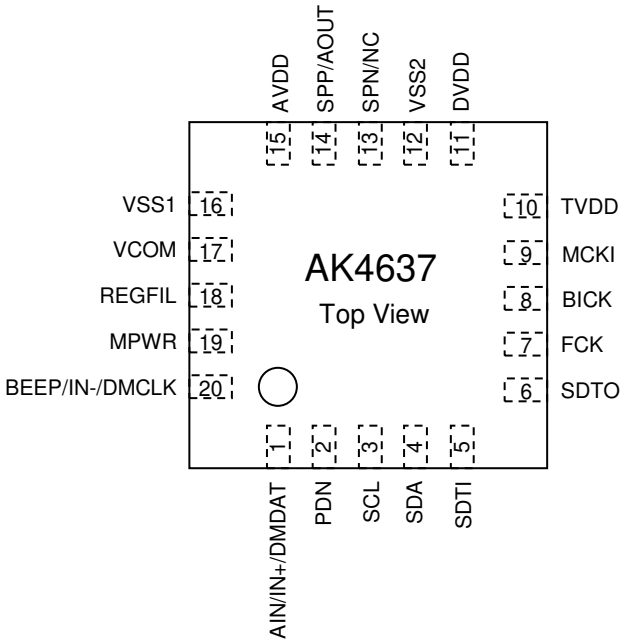


Figure 2. Pin Layout

■ Comparison Table of the AK4951EN

1. Function

Function	AK4951EN	AK4637EN
Stereo/Mono	Stereo	Mono
AVDD	2.8V ~ 3.5V	2.8V ~ 5.5V
SVDD	1.8V ~ 5.5V	-
DVDD	1.6V ~ 1.98V	←
TVDD	1.6V or (DVDD-0.2)V ~ 3.5V	1.6V or (DVDD-0.2)V ~ 3.6V
Differential Input	No	Yes
MIC Sensitivity Correction	Yes	No
Automatic Wind Noise Reduction	Yes	No
Stereo Separation Emphasis Circuit	Yes	No
Headphone Amplifier	Yes	No
Audio I/F Format	DSP Mode is Not Available	DSP Mode is Available
Package	32-pin QFN (4 x 4mm, 0.4mm pitch)	20-pin QFN (3 x 3mm, 0.4mm pitch)

2. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	LOSEL	PMDAC	~~PMADR~~	PMADC
01H	Power Management 2	~~PMOSC~~	0	~~PMHPR~~	~~PMHPL~~	M/S	PMPLL	PMSL	~~LOSEL~~
02H	Signal Select 1	SLPSN	MGAIN3	DACS	~~MPSEL~~	PMMP	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SPKG1	SPKG0	0	MICL	~~INL1~~	~~INL0~~	~~INR1~~	MDIF
04H	Signal Select 3	LVCM1	LVCM0	DACL	0	~~PTS1~~	~~PTS0~~	~~MONO1~~	~~MONO0~~
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	~~BCKO~~	CKOFF	BCKO1	BCKO0
07H	Mode Control 3	TSDSEL	THDET	SMUTE	~~DVOLC~~	MSBS	BCKP	DIF1	DIF0
08H	Digital MIC	~~READ~~	0	~~PMDMR~~	PMDM	DCLKE	0	DCLKP	DMIC
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0FH	BEEP Control	~~HPZ~~	BPVCM	BEEPS	~~BEEPH~~	BPLVL3	BPLVL2	BPLVL1	BPLVL0
10H	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
11H	EQ Common Gain Select	0	0	0	EQC5	EQC4	EQC3	EQC2	0
12H	EQ2 Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
13H	EQ3 Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
14H	EQ4 Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
15H	EQ5 Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0
16H	Digital Filter Select 1	0	0	0	0	0	HPFC1	HPFC0	HPFAD
17H	Digital Filter Select 2	~~GN1~~	~~GN0~~	~~EQ0~~	~~FIL3~~	0	0	LPF	HPF
18H	Digital Filter Mode	0	0	PFVOL1	PFVOL0	PFDAC1	PFDAC0	ADCPF	PFSDO
19H	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1AH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1BH	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1CH	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
1DH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
1EH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
1FH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
20H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
21H	Digital Filter Select 3	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
22H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
23H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
24H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
25H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
26H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
27H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
28H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
29H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
2AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
2BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
2CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
2DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
2EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
2FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
30H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
31H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
32H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
33H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
34H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
35H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
36H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
37H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
38H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
39H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
3AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
3BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
3CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
3DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
3EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
3FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

These bits are added to the AK4637.
These bits are removed from the AK4637.
These bits are changed from the AK4637.

■ PIN/FUNCTION

No.	Pin Name	I/O	Function
1	AIN	I	Analog Input Pin (MDIF bit = "0": Single-ended Input, DMIC bit = "0": default)
	IN+	I	Positive Analog Input Pin (MDIF bit = "1": Full-differential Input, DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
2	PDN	I	Reset & Power-down Pin "L": Reset & Power-down, "H": Normal Operation
3	SCL	I	Control Data Clock Pin
4	SDA	I/O	Control Data Input/Output Pin
5	SDTI	I	Audio Serial Data Input Pin
6	SDTO	O	Audio Serial Data Output Pin
7	FCK	I/O	Frame Clock Pin
8	BICK	I/O	Audio Serial Data Clock Pin
9	MCKI	I	External Master Clock Input Pin
10	TVDD	-	Digital I/O Power Supply Pin, 1.6 or (DVDD-0.2) ~ 3.6V
11	DVDD	-	Digital Power Supply Pin, 1.6 ~ 1.98V
12	VSS2	-	Ground 2 Pin
13	SPN	O	Speaker-Amp Negative Output Pin (LOSEL bit = "0": default)
	NC	O	No Connect Pin (LOSEL bit = "1") This pin should be open.
14	SPP	O	Speaker-Amp Positive Output Pin (LOSEL bit = "0": default)
	AOUT	O	Line Output Pin (LOSEL bit = "1")
15	AVDD	-	Analog Power Supply Pin, 2.8 ~ 5.5V
16	VSS1	-	Ground 1 Pin
17	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2μF±10% or 4.7μF±10% capacitor in series.
18	REGFIL	O	LDO Voltage Output pin for Analog Block (typ 2.3V) This pin must be connected to VSS1 with 2.2μF±10% capacitor in series.
19	MPWR	O	MIC Power Supply Pin
20	BEEP	I	Beep Signal Input Pin (MDIF bit="0": Single-ended Input, DMIC bit="0": default)
	IN-	I	Negative Analog Input Pin (MDIF bit = "1": Full-differential Input, DMIC bit="0")
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")

Note 1. All input pins except analog input pins (AIN/IN+, IN-/BEEP) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	AIN/IN+/DMDAT, BEEP/IN-/DMCLK, MPWR, SPN, SPP/AOUT	Open
Digital	MCKI, SDTI	Connect to VSS2
	SDTO	Open

6. Absolute Maximum Ratings

(VSS1=VSS2=0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	−0.3	6.0	V
	Digital	DVDD	−0.3	2.5	V
	Digital I/O	TVDD	−0.3	6.0	V
	Speaker-Amp	SVDD	−0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	−0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	−0.3	TVDD+0.3	V
Operating Temperature (powered applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C
Maximum Power Dissipation (Note 5)		Pd	-	800	mW

Note 2. All voltages are with respect to ground.
VSS1 and VSS2 must be connected to the same analog ground plane.

Note 3. AIN/IN+ and BEEP/IN- pins

Note 4. PDN, SCL, SDA, SDTI, FCK, BICK and MCKI pins
Pull-up resistors at the SDA and SCL pins must be connected to a voltage in the range from TVDD or more to 6V or less.

Note 5. This power is the AK4637 internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θja (Junction to Ambient) is 50°C/W at JESD51-9 (2p2s) for the AK4637. When Pd = 800mW and the θja is 50°C/W for the AK4637, the junction temperature does not exceed 125°C. In this case, the AK4637 will not be damaged by its internal power dissipation. Therefore, the AK4637 should be used in the condition of θja ≤ 50°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1=VSS2=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 6)	Analog	AVDD	2.8	3.3	3.5	V
	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 7)	TVDD	1.6 or (DVDD-0.2)	1.8	3.5	V

Note 2. All voltages are with respect to ground.

Note 6. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be “L” upon power up, and should be changed to “H” after all power supplies are supplied to avoid an internal circuit error.

Note 7. The minimum value is higher voltage between DVDD-0.2 and 1.6V.

*** When TVDD is powered ON and the PDN pin is “L”, AVDD and DVDD can be powered ON/OFF. The PDN pin must be set to “H” after all power supplies are ON, when the AK4637EN is powered-up from power-down state.**

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

(Ta=25°C; AVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=0V; fs=48kHz, BICK=64fs; Signal Frequency =1kHz; 24bit Data; Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
MIC Amplifier: AIN pin; MDIF bit = "0" (Single-ended input)						
Input Resistance (Note 8)			20	30	40	kΩ
Gain	Gain Setting		0	-	+30	dB
	Step Width		-	3	-	dB
MIC Power Supply: MPWR pin						
Output Voltage	MICL bit = "0"		2.2	2.4	2.6	V
	MICL bit = "1"		1.8	2.0	2.2	
Output Noise Level (A-weighted)			-	-108	-	dBV
Load Resistance			2.0	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (f = 1kHz) (Note 9)			-	100	-	dB
ADC Analog Input Characteristics: AIN pins → ADC (Programmable Filter = OFF) → SDTO						
Resolution			-	-	24	Bits
Input Voltage (Note 10)		(Note 11)	-	0.261	-	Vpp
		(Note 12)	1.86	2.07	2.28	Vpp
S/(N+D) (-1dBFS)		(Note 11)	73	83	-	dBFS
		(Note 12)	-	84	-	dBFS
D-Range (–60dBFS, A-weighted)		(Note 11)	78	88	-	dB
		(Note 12)	-	95	-	dB
S/N (A-weighted)		(Note 11)	78	88	-	dB
		(Note 12)	-	95	-	dB
PSRR (f = 1kHz) (Note 9)			-	90	-	dB

Note 8. Full Differential Input: IN+=20kΩ(typ), IN-=57kΩ(typ)@MGAIN3-0 bits = "0000" (0dB),
IN+=16kΩ(typ), IN-=244kΩ(typ)@MGAIN3-0 bits = "0110" (+18dB)

Note 9. PSRR applied to AVDD with 500mVpp sine wave.

Note 10. Single-ended Input: Vin = 0.9 x 2.3Vpp (typ) @MGAIN3-0 bits = "0000" (0dB)
Full Differential Input: Vin = (IN+) – (IN–) = 0.9 x 2.3Vpp (typ)
IN+ = 0.45 x 2.3Vpp (typ), IN– = 0.45 x 2.3Vpp (typ)

Note 11. MGAIN3-0 bits = "0110" (+18dB)
Full Differential Input: S/(N+D) = 81dB、DR = S/N = 86dB

Note 12. MGAIN3-0 bits = "0000" (0dB)
Full Differential Input: S/(N+D) = 83dB、DR = S/N = 93dB

Parameter			Min.	Typ.	Max.	Unit
DAC Characteristics:						
Resolution			-	-	24	Bit
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
SPKG1-0 bits = "11", –0.5dBFS (Po=1000mW) (AVDD=5V)			-	2.83	-	Vrms
S/(N+D)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	80	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			40	75	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
SPKG1-0 bits = "11", –0.5dBFS (Po=1000mW) (AVDD=5V)			-	20	-	dB
S/N (A-weighted)	SPKG1-0 bits = "01"		80	97	-	dB
Output Offset Voltage	SPKG1-0 bits = "01"		-30	0	+30	mV
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	100	pF
PSRR (f = 1kHz) (Note 13)			-	60	-	dB
Line Output Characteristics: DAC → AOUT pin, ALC=OFF, IVOL=DVOL= 0dB, R_L=10kΩ, LVCM1-0 bits = "01"						
Output Voltage	(0dBFS)	LVCM0 bit = "0" AVDD=2.8V	-	2.26	-	Vpp
		LVCM0 bit = "1"	-	1.0	-	Vrms
	(-3dBFS)	LVCM0 bit = "0" AVDD=2.8V	1.44	1.6	1.76	Vpp
		LVCM0 bit = "1"	1.82	2.0	2.22	Vpp
S/(N+D)	(0dBFS)	LVCM0 bit = "0" AVDD=2.8V	-	80	-	dB
		LVCM0 bit = "1"	-	40	-	dB
	(-3dBFS)		75	85	-	dB
S/N (A-weighted)			82	94	-	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF
Mono Input: BEEP pin (PMBP bit ="1", BPVCM bit = "0", BPLVL3-0 bits = "0000")						
Input Resistance			46	66	86	kΩ
Maximum Input Voltage (Note 14)			-	-	1.54	Vpp
Gain						
BEEP pin → SPP/SPN pins (Note 15)		SPKG1-0 bits = "00"	+4.4	+6.4	+8.4	dB
		SPKG1-0 bits = "01"	-	+8.4	-	dB
		SPKG1-0 bits = "10"	-	+11.1	-	dB
		SPKG1-0 bits = "11"	-	+14.9	-	dB
BEEP pin → AOUT pin		LVCM1-0 bits = "00"	-1	0	+1	dB
		LVCM1-0 bits = "01"	-	+2	-	dB
		LVCM1-0 bits = "10"	-	+2	-	dB
		LVCM1-0 bits = "11"	-	+4	-	dB

Note 13. PSRR applied to AVDD with 500mVpp sine wave.

Note 14. The maximum value is the smaller one of AVDD Vpp or 3.3Vpp when BPVCM bit = "1". However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (Set by BPLVL3-0 bits)

Note 15. This gain is an ideal gain when no load resistance.

Parameter	Min.	Typ.	Max.	Unit
Power Supplies:				
Power Up (PDN pin = "H", All Circuit Power Up)				
AVDD+DVDD+TVDD (Note 16)	-	6.6	10.2	mA
AVDD+DVDD+TVDD (Note 17)	-	5.6	-	mA
Power Down (PDN pin = "L")				
AVDD+DVDD+TVDD (Note 18)	-	0	10	μA

Note 16. When PLL Master Mode (MCKI=12MHz), PMADC=PMDAC=PMPFIL=PMSL=PMVCM=PMPLL =PMBP=PMMP=M/S=SLPSN bits = "1" and LOSEL bit = "0". In this case, the MPWR pin outputs 0mA. AVDD= 4.9mA (typ), DVDD= 1.5mA (typ), TVDD= 0.2mA (typ).

Note 17. When EXT Slave Mode (PMPLL=M/S bits ="0"), PMADC =PMDAC=PMSL=PMVCM=PMBP =PMMP=SLPSN bits = "1" and PMPFIL = LOSEL bits = "0". In this case, the MPWR pin outputs 0mA. AVDD= 4.6mA (typ), DVDD= 1.0mA (typ), TVDD= 0.02mA (typ).

Note 18. All digital input pins are fixed to TVDD or VSS2.

■ Power Consumption on Each Operation Mode

Conditions: Ta=25°C; AVDD= 3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=0V; fs=48kHz,
Programmable Filter=OFF, External Slave Mode, BICK=64fs; AIN input = No signal;
SDTI input = No data; Speaker output = No load.

Mode	Power Management Bit						AVDD [mA]	DVDD [mA]	TVDD [mA]	Total Power [mW]
	PMVCM	PMADC	PMDAC	LOSEL	PMSL	PMPFIL				
All Power-down	0	0	0	0	0	0	0	0	0	0
AIN → ADC	1	1	0	0	0	0	1.6	0.65	0.02	6.5
DAC → SPK	1	0	1	0	1	0	3.2	0.55	0.02	11.6
DAC → Line out	1	0	1	1	1	0	1.6	0.55	0.02	6.3
AIN → ADC & DAC → SPK	1	1	1	0	1	0	4.1	1.0	0.02	15.4
AIN → ADC & DAC → Line out	1	1	1	1	1	0	2.5	1.0	0.02	10.1

Table 1. Power Consumption on Each Operation Mode (typ)

■ Filter Characteristics

(Ta=25°C; fs=48kHz; AVDD=2.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 19)	±0.16dB	PB	0	-	18.8	kHz
	−0.66dB		-	21.1	-	kHz
	−1.1dB		-	21.7	-	kHz
	−6.9dB		-	24.1	-	kHz
Stopband (Note 19)		SB	28.4	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 20)		GD	-	17	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	−3.0dB	FR	-	3.7	-	Hz
(Note 19)	−0.5dB		-	10.9	-	Hz
	−0.1dB		-	23.9	-	Hz
DAC Digital Filter (LPF):						
Passband	−0.006dB ~ +0.076dB	PB	0	-	21.9	kHz
(Note 19)	−6.0dB		-	24	-	kHz
Stopband (Note 19)		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.006	-	+0.076	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 20)		GD	-	27	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 19. The passband and stopband frequencies scale with fs (sampling frequency).

Note 20. A calculating delay time which is induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. For the signal through the programmable filters (1st order HPF + 1st order LPF + 4-band Equalizer + ALC + 1-band Equalizer), the group delay is increased by 4/fs from the value above in both recording and playback modes if there is no phase change by the IIR filter.

■ DC Characteristics

(Ta=25°C; fs=48kHz; AVDD=2.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface & Serial µP Interface (SDA, CSL, PDN, SDTI, BICK, FCK, MCKI pins Input)					
High-Level Input Voltage (TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
(TVDD < 2.2V)		80%TVDD	-	-	V
Low-Level Input Voltage (TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
(TVDD < 2.2V)		-	-	20%TVDD	V
Input Leakage Current	Iin1	-	-	±10	µA
Audio Interface & Serial µP Interface (SDA, BICK, FCK, SDTO pins Output)					
High-Level Output Voltage (Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin: Iout = 80µA)	VOL1	-	-	0.2	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout = 3mA)	VOL2	-	-	0.4	V
(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Digital MIC Interface (DMDAT pin Input; DMIC bit = "1", AVDD=2.8~3.6V)					
High-Level Input Voltage	VIH2	65%AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35%AVDD	V
Input Leakage Current	Iin2	-	-	±10	µA
Digital MIC Interface (DMCLK pin Output; DMIC bit = "1" , AVDD=2.8~3.6V)					
High-Level Output Voltage (Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80µA)	VOL3	-	-	0.4	V

■ Switching Characteristics

(Ta=25°C; fs=48kHz; C_L=20pF; AVDD=2.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	PLL3-0 bits = “0100”	fCLK	-	11.2896	-	MHz
	PLL3-0 bits = “0101”	fCLK	-	12.288	-	MHz
	PLL3-0 bits = “0110”	fCLK	-	12	-	MHz
	PLL3-0 bits = “0111”	fCLK	-	24	-	MHz
	PLL3-0 bits = “1100”	fCLK	-	13.5	-	MHz
	PLL3-0 bits = “1101”	fCLK	-	27	-	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
FCK Output Timing						
Frequency		fs	-	Table 8	-	Hz
DSP Mode: Pulse Width High		tFCKH	-	1/fBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO1-0 bit = “00”	fBCK	-	16fs	-	Hz
	BCKO1-0 bit = “01”	fBCK	-	32fs	-	Hz
	BCKO1-0 bit = “10”	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = BICK pin)						
FCK Input Timing						
Frequency	PLL3-0 bits = “0001”	fs	-	fBCK/16	-	Hz
	PLL3-0 bits = “0010”	fs	-	fBCK/32	-	Hz
	PLL3-0 bits = “0011”	fs	-	fBCK/64	-	Hz
DSP Mode: Pulse Width High		tFCKH	1/fBCK−60	-	1/fs−1/fBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Frequency	PLL3-0 bits = “0001”	fBCK	0.128	-	0.768	MHz
	PLL3-0 bits = “0010”	fBCK	0.256	-	1.536	MHz
	PLL3-0 bits = “0011”	fBCK	0.512	-	3.072	MHz
Pulse Width Low		tBCKL	0.4/fBCK	-	-	s
Pulse Width High		tBCKH	0.4/fBCK	-	-	s

Parameter		Symbol	Min.	Typ.	Max.	Unit
External Slave Mode						
MCKI Input Timing						
Frequency	CM1-0 bits = "00"	fCLK	-	256fs	-	Hz
	CM1-0 bits = "01"	fCLK	-	384fs	-	Hz
	CM1-0 bits = "10"	fCLK		512fs		Hz
	CM1-0 bits = "11"	fCLK	-	1024fs	-	Hz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
FCK Input Timing						
Frequency	CM1-0 bits = "00"	fs	8	-	48	kHz
	CM1-0 bits = "01"	fs	8	-	48	kHz
	CM1-0 bits = "10"	fs	8	-	48	kHz
	CM1-0 bits = "11"	fs	8	-	24	kHz
DSP Mode: Pulse Width High		tFCKH	1/fBCK−60	-	1/fs−1/fBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Frequency		fBCK	16fs	-	64fs	Hz
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	2.048	-	12.288	MHz
	384fs	fCLK	3.072	-	18.432	MHz
	512fs	fCLK	4.096	-	24.576	MHz
	1024fs	fCLK	8.192	-	24.576	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
FCK Output Timing						
Frequency	CM1-0 bits = "00"	fs	-	fCLK/256	-	Hz
	CM1-0 bits = "01"	fs	-	fCLK/384	-	Hz
	CM1-0 bits = "10"	fs	-	fCLK/512	-	Hz
	CM1-0 bits = "11"	fs	-	fCLK/1024	-	Hz
DSP Mode: Pulse Width High		tFCKH	-	1/fBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO1-0 bit = "00"	fBCK	-	16fs	-	Hz
	BCKO1-0 bit = "01"	fBCK	-	32fs	-	Hz
	BCKO1-0 bit = "10"	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (DSP Mode)					
Master Mode					
FCK "↑" to BICK "↑" (Note 21)	tDBF	0.5x1/fBCK−40	0.5x1/fBCK	0.5x1/fBCK+40	ns
FCK "↑" to BICK "↓" (Note 22)	tDBF	0.5x1/fBCK−40	0.5x1/fBCK	0.5x1/fBCK+40	ns
BICK "↑" to SDTO (BCKP bit ="0")	tBSD	−70	-	70	ns
BICK "↓" to SDTO (BCKP bit ="1")	tBSD	−70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
FCK "↑" to BICK "↑" (Note 21)	tFCKB	0.4x1/fBCK	-	-	ns
FCK "↑" to BICK "↓" (Note 22)	tFCKB	0.4x1/fBCK	-	-	ns
BICK "↑" to FCK "↑" (Note 21)	tBFCK	0.4x1/fBCK	-	-	ns
BICK "↓" to FCK "↑" (Note 22)	tBFCK	0.4x1/fBCK	-	-	ns
BICK "↑" to SDTO (BCKP bit ="0")	tBSD	-	-	80	ns
BICK "↓" to SDTO (BCKP bit ="1")	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Audio Interface Timing (Right/Left justified &I²S)					
Master Mode					
BICK "↓" to FCK Edge (Note 23)	tBFCK	−40	-	40	ns
FCK Edge to SDTO (MSB) (Except I²S mode)	tFCKD	−70	-	70	ns
BICK "↓" to SDTO	tBSD	−70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
FCK Edge to BICK "↑" (Note 23)	tFCKB	50	-	-	ns
BICK "↑" to FCK Edge (Note 23)	tBFCK	50	-	-	ns
FCK Edge to SDTO (MSB) (Except I²S mode)	tFCKD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Digital Audio Interface Timing; C_L=100pF					
DMCLK Output Timing					
Period	tSCK	-	1/(64fs)	-	s
Rising Time	tSRise	-	-	10	ns
Falling Time	tSFall	-	-	10	ns
Duty Cycle	dSCK	40	50	60	%
Audio Interface Timing					
DMDAT Setup Time	tDSDS	50	-	-	ns
DMDAT Hold Time	tDSDH	0	-	-	ns

Note 21. MSBS, BCKP bits = "00" or "11".
Note 22. MSBS, BCKP bits = "01" or "10".
Note 23. BICK rising edge must not occur at the same time as FCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus) (Note 24)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 25)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 26)	tAPD	200	-	-	ns
PDN Reject Pulse Width (Note 26)	tRPD	-	-	50	ns
PMADC "↑" to SDTO valid (Note 27)					
ADRST1-0 bits ="00"	tPDV	-	1059	-	1/fs
ADRST1-0 bits ="01"	tPDV	-	267	-	1/fs
ADRST1-0 bits ="10"	tPDV	-	531	-	1/fs
ADRST1-0 bits ="11"	tPDV	-	135	-	1/fs
VCOM Voltage					
Rising Time (Note 28)	tRVCM	-	0.6	2.0	ms

Note 24. I^2C Bus is a trademark of NXP B.V.

Note 25. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

Note 26. The AK4637 can be reset by the PDN pin = "L". The PDN pin must be held "L" for more than 200ns for a certain reset. The AK4637 is not reset by the "L" pulse less than 50ns.

Note 27. This is the count of FCK "↑" from the PMADC bit = "1".

Note 28. All analog blocks including PLL block are powered up after the VCOM voltage (VCOM pin) rises up. An external capacitor of the VCOM pin is 2.2μF (AVDD ≤ 3.6V) or 4.7μF (AVDD > 3.6V) and the REGFIL pin is 2.2μF. The capacitance variation should be ±10%.

■ Timing Diagram

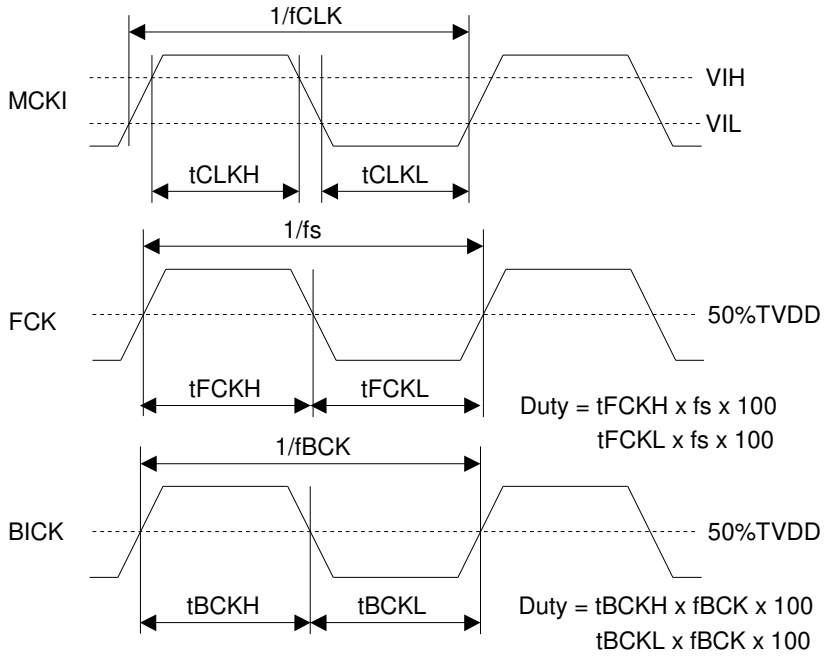


Figure 3. Clock Timing (PLL/EXT Master mode)

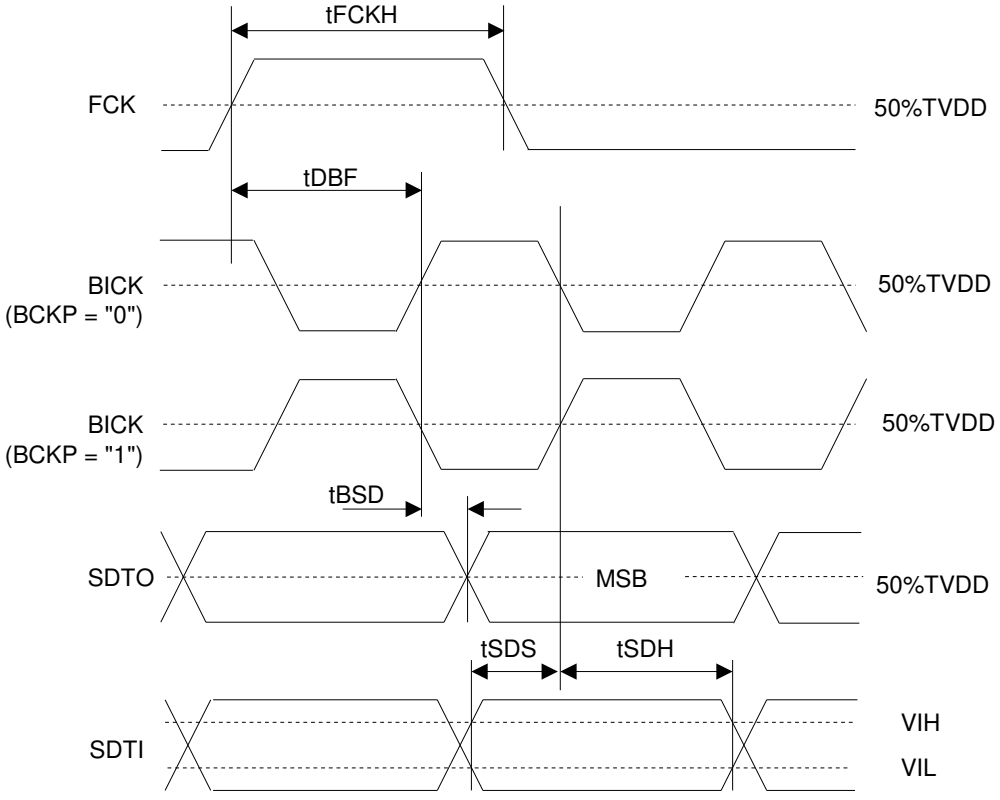


Figure 4. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS bit= “0”)

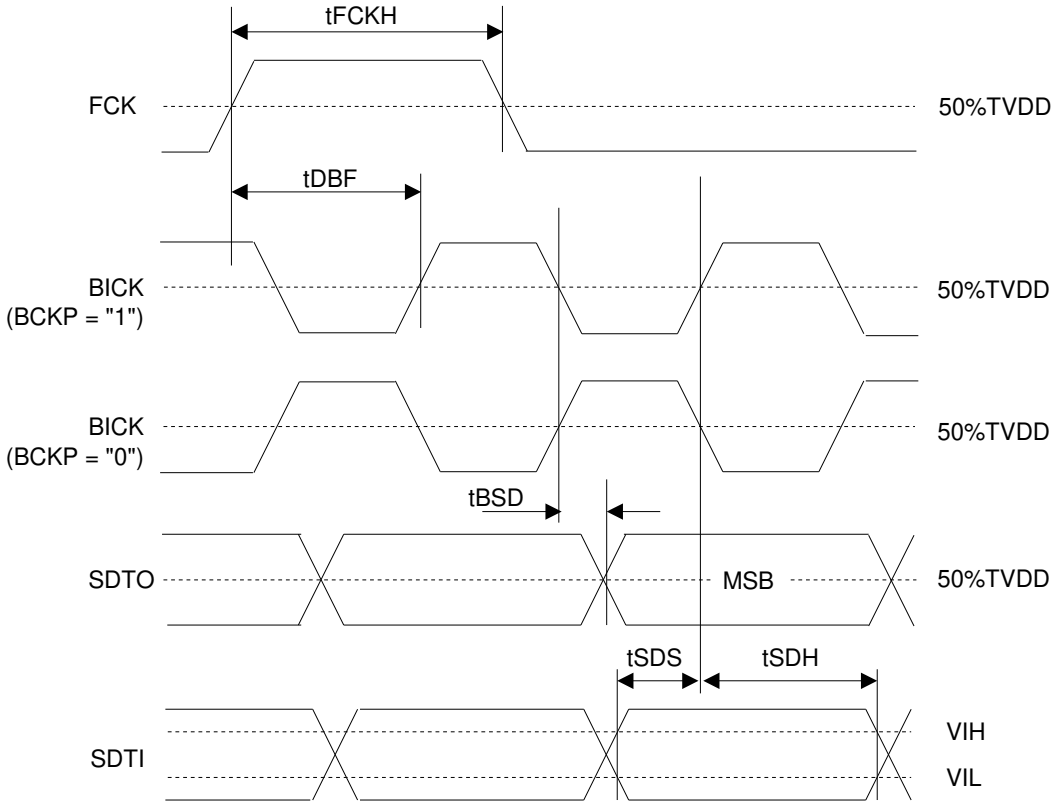


Figure 5. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS bit= “1”)

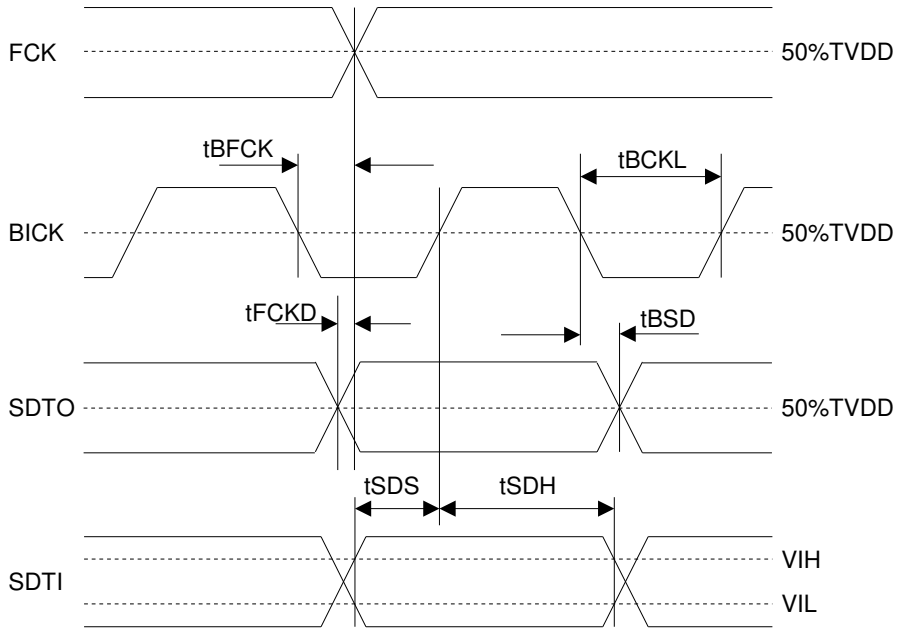


Figure 6. Audio Interface Timing (PLL/EXT Master mode; Except DSP mode)

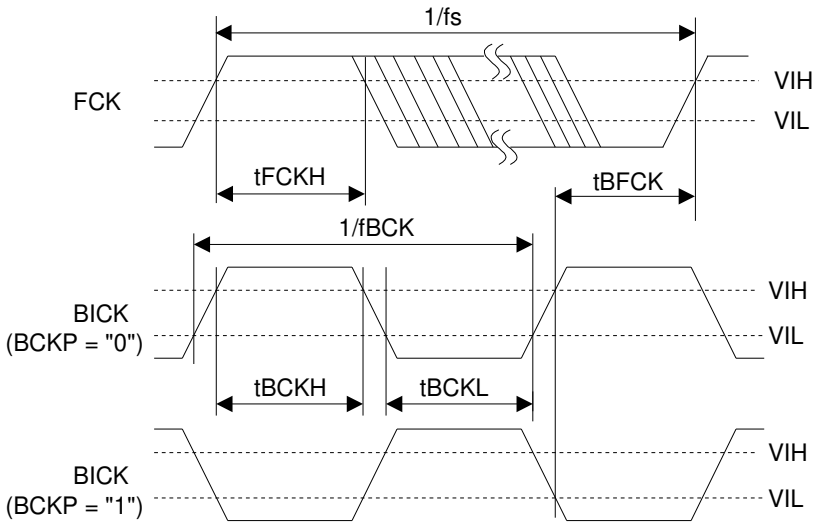


Figure 7. Clock Timing (PLL/EXT Slave mode; DSP mode, MSBS bit= “0”)

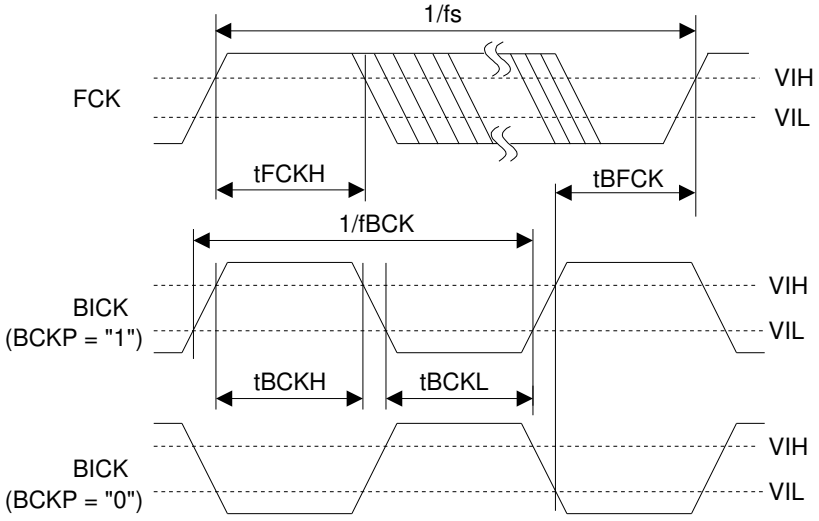


Figure 8. Clock Timing (PLL/EXT Slave mode; DSP mode, MSBS bit= “1”)

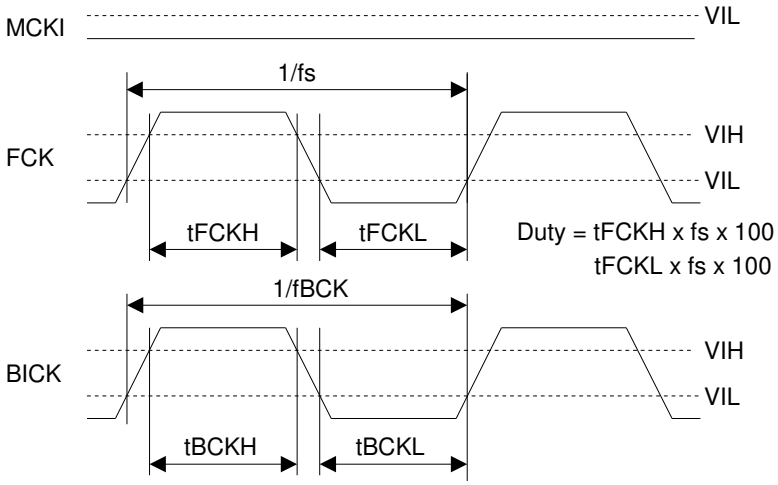


Figure 9. Clock Timing (PLL Slave mode; Except DSP mode)

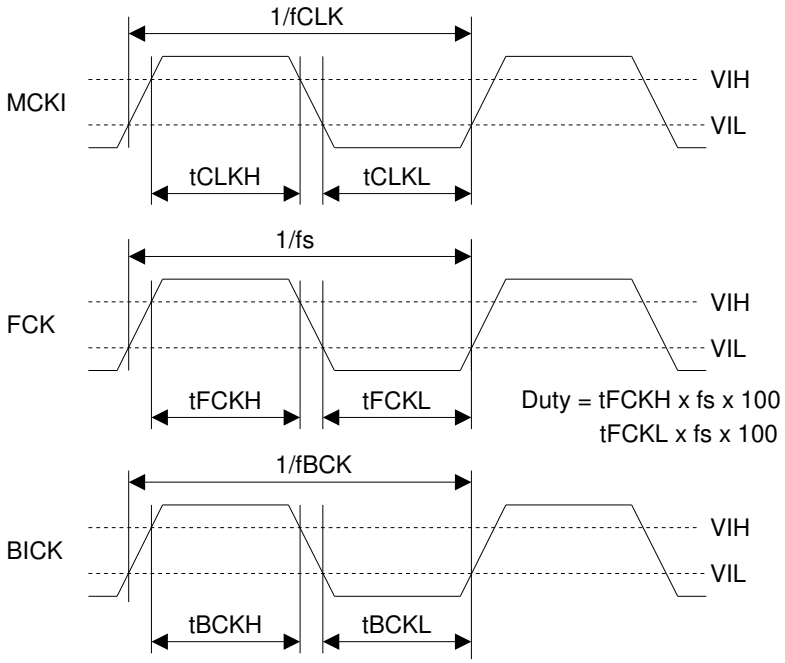


Figure 10. Clock Timing (EXT Slave mode)

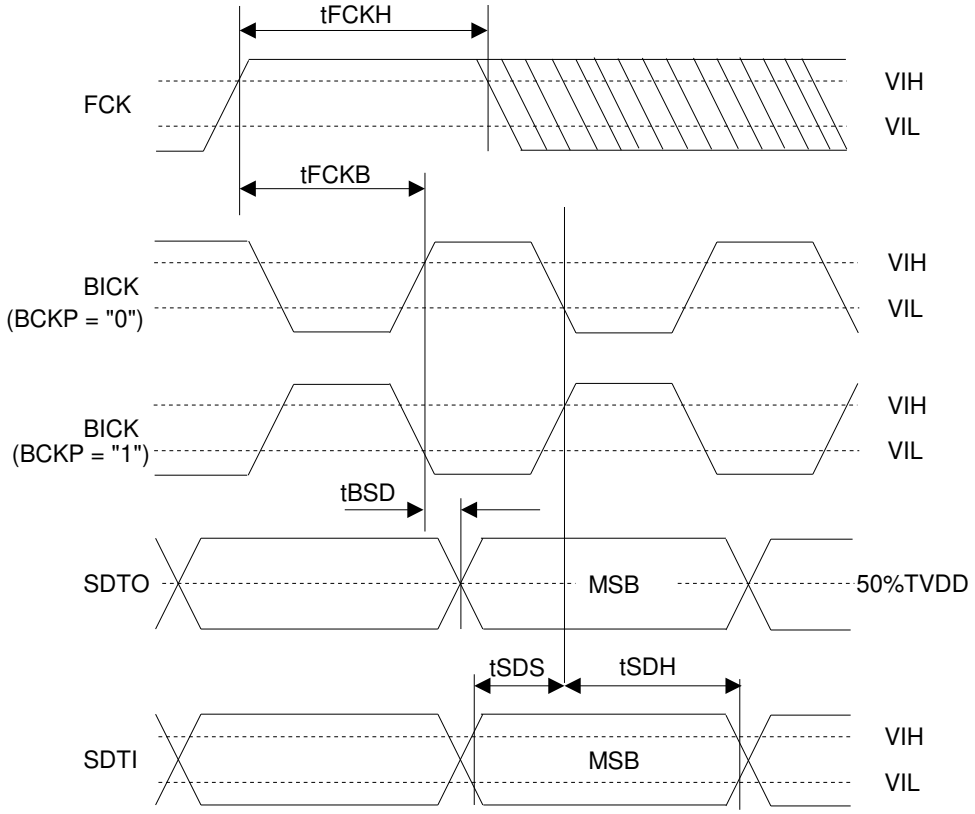


Figure 11. Audio Interface Timing (PLL/EXT Slave mode, DSP mode; MSBS bit= “0”)

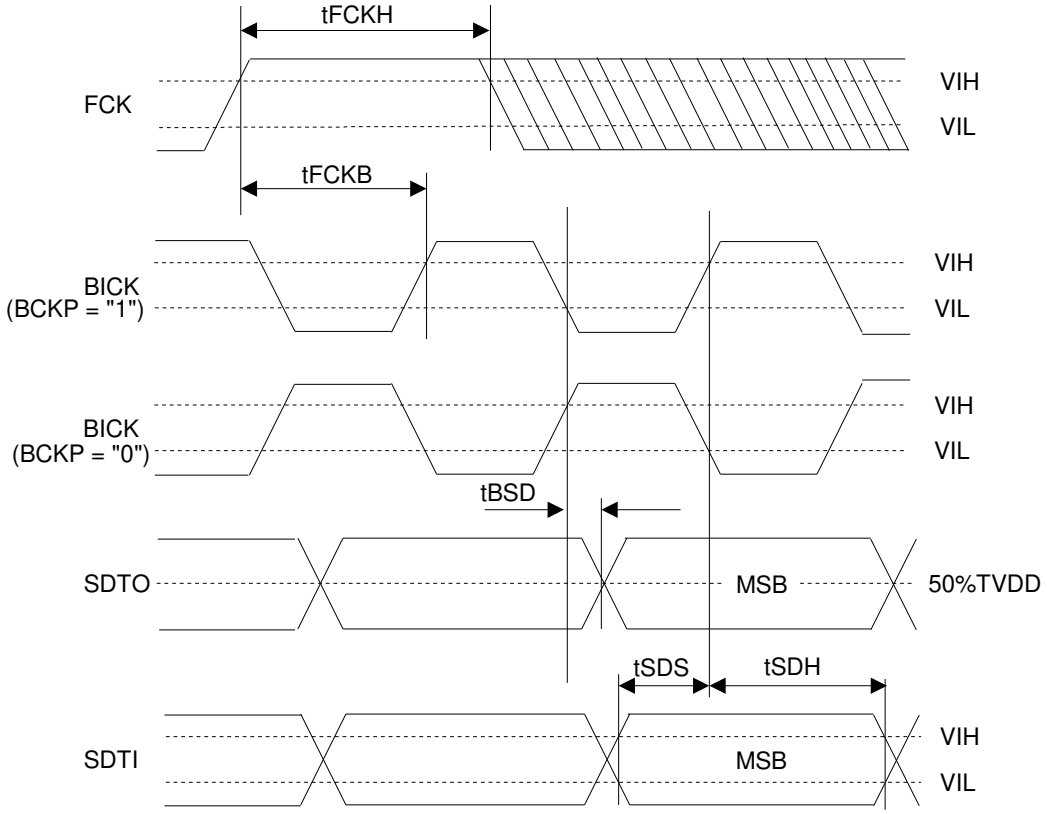


Figure 12. Audio Interface Timing (PLL/EXT Slave mode, DSP mode, MSBS bit= “1”)

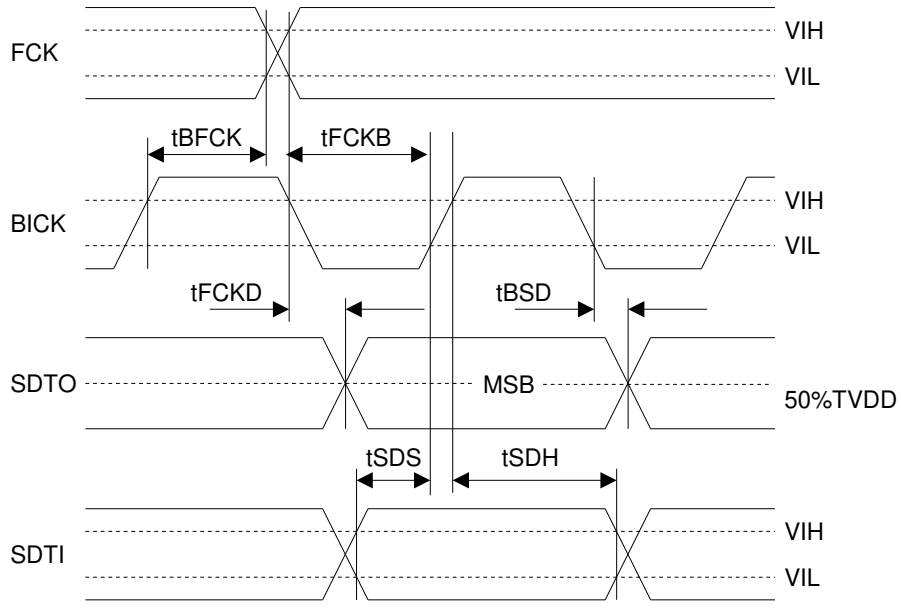
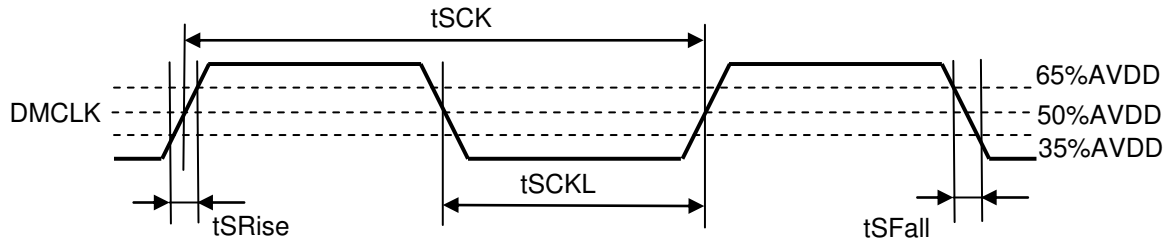


Figure 13. Audio Interface Timing (PLL/EXT Slave mode; Except DSP mode)



dSCK = 100 x tSCKL / tSCK

Figure 14. DMCLK Clock Timing

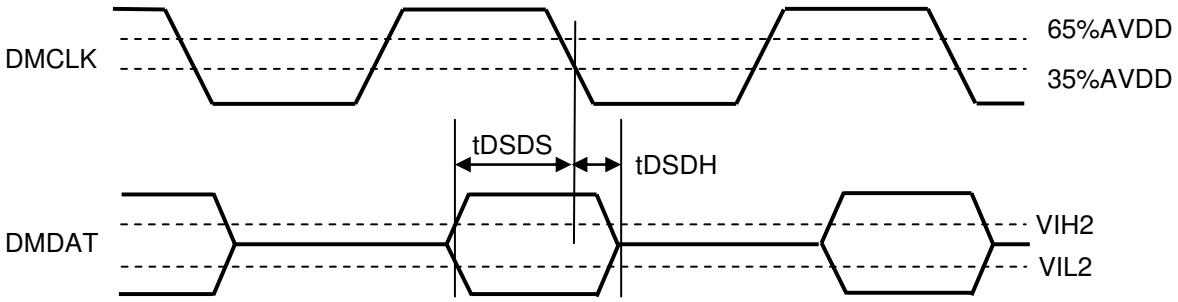


Figure 15. Audio Interface Timing (DCLKP bit = "1")

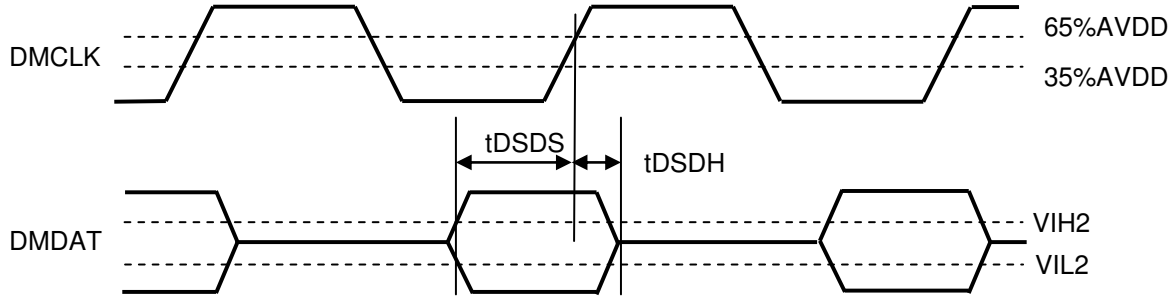


Figure 16. Audio Interface Timing (DCLKP bit = "0")

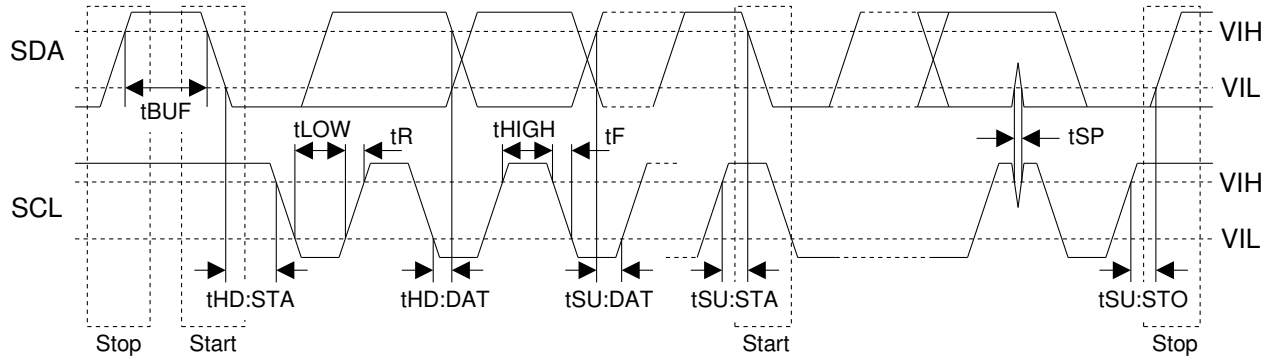


Figure 17. I^2C Bus Mode Timing

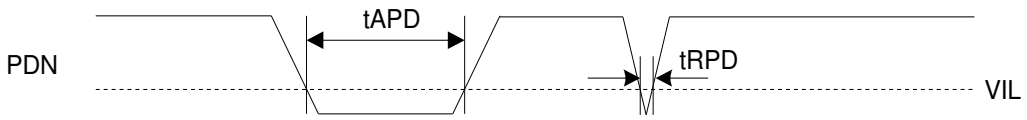


Figure 18. Power Down & Reset Timing 1

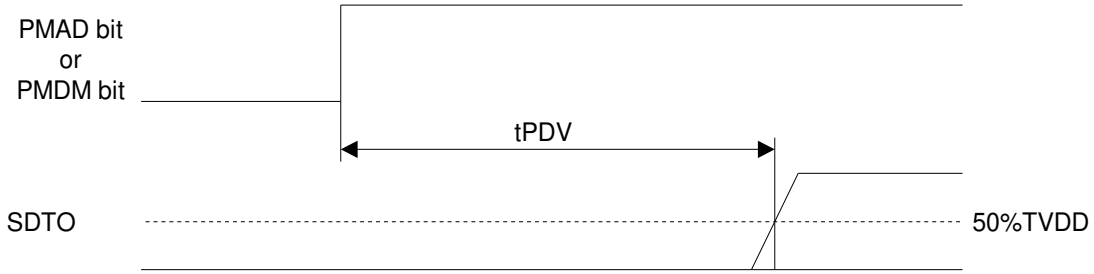


Figure 19. Power Down & Reset Timing 2

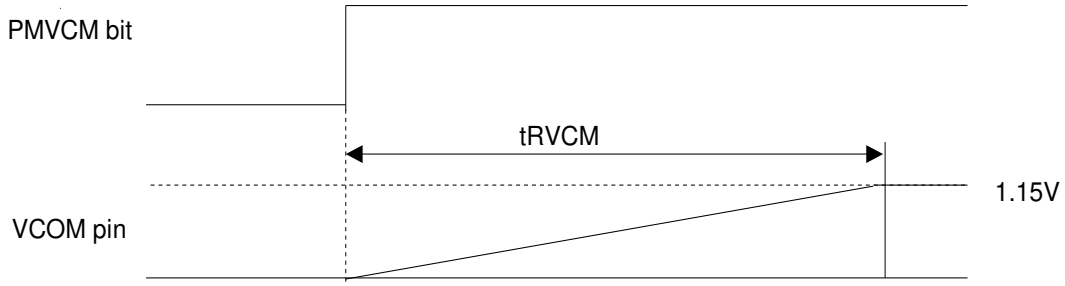


Figure 20. VCOM Rising Timing

9. Functional Descriptions

■ System Clock

There are the following four clock modes to interface with external devices (Table 2, Table 3).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	Table 5	Figure 21
PLL Slave Mode (PLL Reference Clock: BICK pin)	1	0	Table 5	Figure 22
EXT Slave Mode	0	0	X	Figure 23
EXT Master Mode	0	1	X	Figure 24

Table 2. Clock Mode Setting (x: Don't care)

Mode	MCKI pin	BICK pin	FCK pin
PLL Master Mode	Input Frequency of Table 5 (Selected by PLL3-0 bits)	Output (Selected by BCKO bit)	Output (1fs)
PLL Slave Mode (PLL Reference Clock: BICK pin)	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	Input Frequency of Table 11 (Selected by CM1-0 bits)	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	Input Frequency of Table 14 (Selected by CM1-0 bits)	Output (Selected by BCKO bit)	Output (1fs)

Table 3. Clock Pins States in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4637 is in power-down mode (PDN pin = "L") and when exits reset state, the AK4637 is in slave mode. After exiting reset state, the AK4637 goes to master mode by changing M/S bit to "1".

When the AK4637 is in master mode, the FCK and BICK pins are a floating state until M/S bit becomes "1". The FCK and BICK pins of the AK4637 must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 4. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4637 is supplied stable clocks after PLL is powered-up (PMPLL bit = “0” → “1”) or the sampling frequency is changed, are shown in Table 5.

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)	
1	0	0	0	1	BICK pin	16fs	2ms	
2	0	0	1	0	BICK pin	32fs	2ms	
3	0	0	1	1	BICK pin	64fs	2ms	
4	0	1	0	0	MCKI pin	11.2896MHz	5ms	
5	0	1	0	1	MCKI pin	12.288MHz	5ms	(default)
6	0	1	1	0	MCKI pin	12MHz	5ms	
7	0	1	1	1	MCKI pin	24MHz	5ms	
12	1	1	0	0	MCKI pin	13.5MHz	5ms	
13	1	1	0	1	MCKI pin	27MHz	5ms	
Others	Others				N/A			

Table 5. PLL Mode Setting (*fs: Sampling Frequency, N/A: Not Available)

■ PLL Unlock State

In this mode, FCK and BICK pins go to “L” until the PLL goes to lock state after PMPLL bit = “0” → “1” (Table 6).

After the PLL is locked, a first period of FCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

The BICK and FCK pins do not output invalid clocks such as PLL unlock state by setting PMPLL bit to “0”. During PMPLL bit = “0”, these pins output the same clock as EXT master mode.

PLL State	BICK pin	FCK pin
After PMPLL bit “0” → “1”	“L” Output	“L” Output
PLL Unlock (except the case above)	Invalid	Invalid
PLL Lock	Table 9	1fs Output

Table 6. Clock Operation at PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates BICK and FCK clocks. When the state of AK4637 is ADC power-down or Loopback mode, the output of BICK, FCK and SDTO pins can be stopped by CKOFF bit. When CKOFF bit = "1", BICK, FCK and SDTO pins output "L". The sampling frequency is selected by FS3-0 bits as defined in Table 7. The BICK output frequency is selected between 16fs, 32fs or 64fs, by BCKO bit (Table 9).

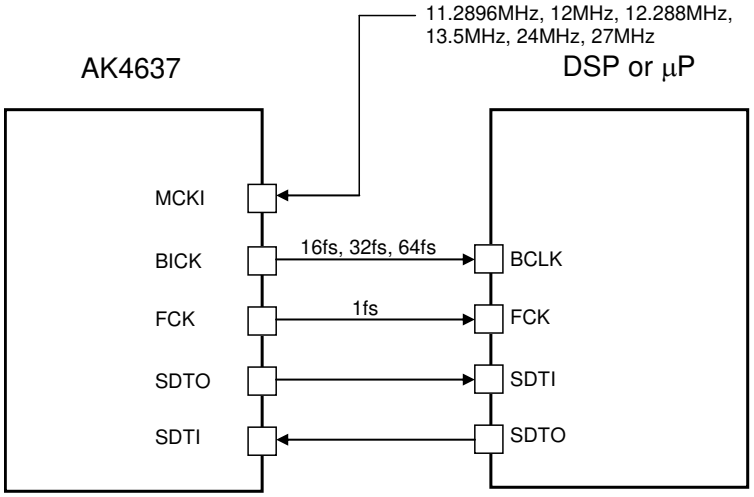


Figure 21. PLL Master Mode

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 29)	
1	0	0	0	1	8kHz mode	
2	0	0	1	0	11.025kHz mode	
3	0	0	1	1	12kHz mode	
5	0	1	0	1	16kHz mode	
6	0	1	1	0	22.05kHz mode	
7	0	1	1	1	24kHz mode	
9	1	0	0	1	32kHz mode	
10	1	0	1	0	44.1kHz mode	
11	1	0	1	1	48kHz mode	(default)
Others	Others				N/A	

Table 7. Setting of Sampling Frequency (Reference Clock = MCKI pin) (N/A: Not Available)

Note 29. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 8 for the details of sampling frequency. In master mode, FCK and BICK output frequency correspond to sampling frequencies shown in Table 8.

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz] (Note 30)
12	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
24	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
13.5	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
27	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
11.2896	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	Note 31
	22.05kHz mode	Note 31
	44.1kHz mode	Note 31
	Sampling frequency that differs from sampling frequency of mode name	

Note 30. These values are rounded off to six decimal places.
Note 31. The AK4637 must be in EXT master mode when selecting this mode.

Table 8. Sampling Frequency at PLL mode (Reference clock is MCKI) (1)

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz] (Note 30)
12.288	8kHz mode	8.000000
	12kHz mode	Note 31
	16kHz mode	16.000000
	24kHz mode	Note 31
	32kHz mode	32.000000
	48kHz mode	Note 31
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	Sampling frequency that differs from sampling frequency of mode name	

Note 30. These values are rounded off to six decimal places.
Note 31. The AK4637 must be in EXT master mode when selecting this mode.
Table 8. Sampling Frequency at PLL mode (Reference clock is MCKI) (2)

Mode	BCKO1 bit	BCKO0 bit	BICK Output Frequency	
0	0	0	16fs	(default)
1	0	1	32fs	
2	1	0	64fs	
3	1	1	N/A	

Table 9. BICK Output Frequency at Master Mode (N/A: Not available)

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the BICK pin. The required clock for the AK4637 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 5).

The BICK and FCK inputs must be synchronized. The sampling frequency can be selected by FS3-2 bits (Table 10).

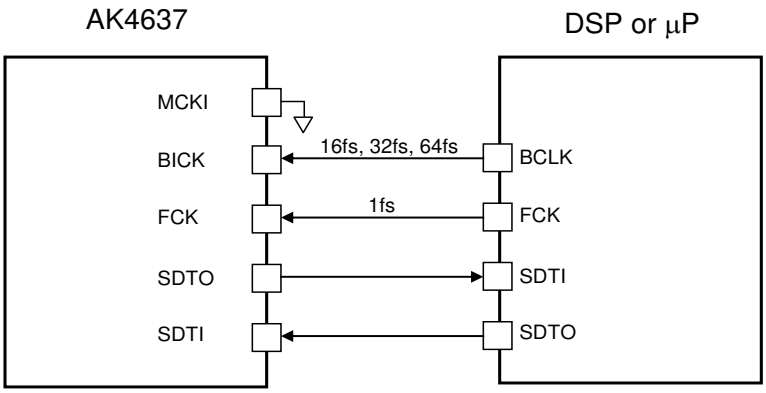


Figure 22. PLL Slave Mode (PLL Reference Clock: BICK pin)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	x	x	8kHz ≤ fs ≤ 12kHz	
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	(default)
Others	Others				N/A	

Table 10. Setting of Sampling Frequency (Reference Clock = BICK pin)
(x: Do not care, N/A: Not Available)

■ EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

When PMPLL bit is “0”, the AK4637 becomes EXT mode. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without internal PLL circuit operation. This mode is compatible with I/F of a normal audio CODEC. The external clocks required to operate this mode are MCKI (256fs, 384fs, 512fs or 1024fs), FCK (fs) and BICK (≥16fs). The master clock (MCKI) must be synchronized with FCK. The phase between these clocks is not important. The input frequency of MCKI is selected by CM1-0 bits (Table 11) and the sampling frequency is selected by FS3-2 bits (Table 12).

Mode	CM1 bit	CM0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	256fs	8kHz ≤ fs ≤ 48kHz	(default)
1	0	1	384fs	8kHz ≤ fs ≤ 48kHz	
2	1	0	512fs	8kHz ≤ fs ≤ 48kHz	
3	1	1	1024fs	8kHz ≤ fs ≤ 24kHz	

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	x	x	8kHz ≤ fs ≤ 12kHz	
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	(default)
Others	Others				N/A	

Table 12. Setting of Sampling Frequency (N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through SPP/SPN pins is shown in Table 13.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	80dB
384fs	80dB
512fs	93dB
1024fs	96dB

Table 13. Relationship between MCKI and S/N of SPP/SPN pins

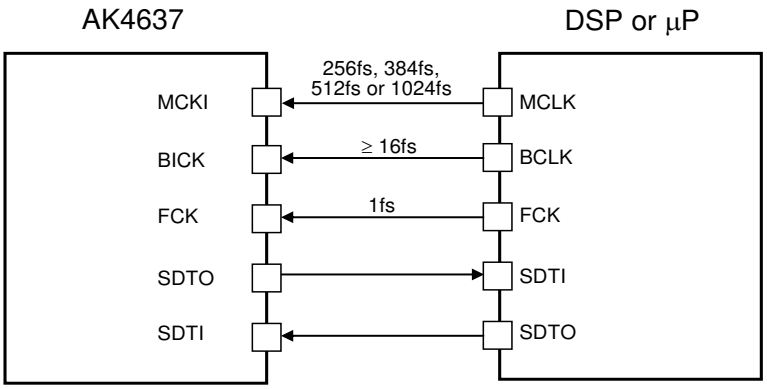


Figure 23. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4637 becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock can be input to the internal ADC and DAC directly from the MCKI pin without the internal PLL circuit operation. The external clock required to operate the AK4637 is MCKI (256fs, 384fs, 512fs or 1024fs). The input frequency of MCKI is selected by CM1-0 bits (Table 14) and the sampling frequency is selected by FS3-2 bits (Table 15). When the state of AK4637 is ADC power-down or Loopback mode, the output of BICK, FCK and SDTO pins can be stopped by CKOFF bit. When CKOFF bit = "1", BICK, FCK and SDTO pins output "L". The BICK output frequency is selected between 16fs, 32fs, 64fs, by BCKO bit (Table 17).

Mode	CM1 bit	CM0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	256fs	8kHz ≤ fs ≤ 48kHz	(default)
1	0	1	384fs	8kHz < fs ≤ 48kHz	
2	1	0	512fs	8kHz < fs ≤ 48kHz	
3	1	1	1024fs	8kHz ≤ fs ≤ 24kHz	

Table 14. MCKI Frequency at EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	x	x	8kHz ≤ fs ≤ 12kHz	
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	(default)
Others	Others				N/A	

Table 15. Setting of Sampling Frequency (x: Do not care, N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through SPP/SPN pins is shown in Table 16.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	80dB
384fs	80dB
512fs	93dB
1024fs	96dB

Table 16. Relationship between MCKI and S/N of SPP/SPN pins

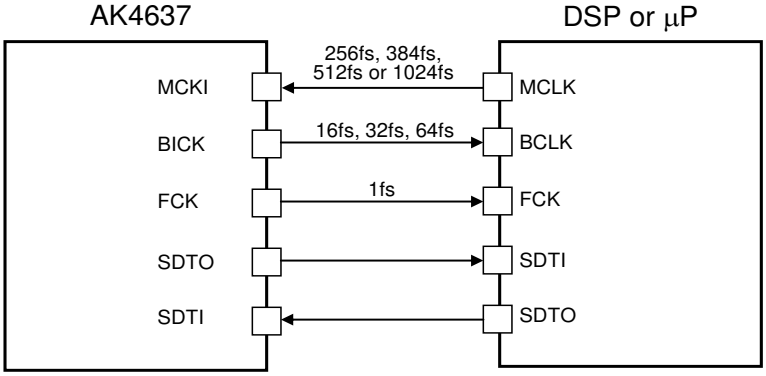


Figure 24. EXT Master Mode

Mode	BCKO1 bit	BCKO0 bit	BICK Output Frequency	
0	0	0	16fs	(default)
1	0	1	32fs	
2	1	0	64fs	
3	1	1	N/A	

Table 17. BICK Output Frequency at Master Mode

■ System Reset

Upon power-up, the AK4637 must be reset by bringing the PDN pin = “L”. This reset is released when a dummy command is input after the PDN pin = “H”. This ensures that all internal registers reset to their initial value. Dummy command is executed by writing all “0” to the register address 00H (Figure 25). It is recommended to set the PDN pin to “L” before power up the AK4637.

In I^{2}C Bus mode, the AK4637 does not return an ACK after receiving a slave address by a dummy command as shown in Figure 25. In the actual case, initialization cycle starts by 8 SCL clocks during the PDN pin = “H” regardless of the SDA line. Therefore, retry command is not required (Figure 26). Executing a write or read command to the other device that is connected to the same I^{2}C Bus also resets the AK4637.

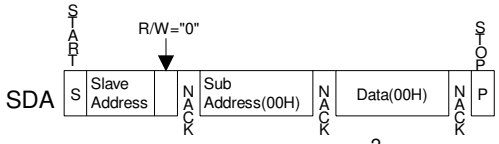


Figure 25. Dummy Command in I^{2}C Bus Mode

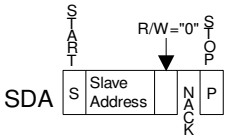


Figure 26. Reset Completion for example

The ADC starts an initialization cycle by setting PMADC bit to “1” from “0”. The initialization cycle is set by ADRST1-0 bits (Table 18). During the initialization cycle, the ADC digital data outputs of both channels are forced to “0” in 2's complement. The ADC output reflects the analog input signal after the initialization cycle is finished. When using a digital microphone (PMDML/R bits =“0” → “1”), the initialization cycle is the same as ADC’s.

Note 32. The initial data of ADC has offset data that depends on microphones and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST1-0 bits or do not use the first data of ADC outputs.

ADRST1-0 bits	Initialize Cycle				
	Cycle	fs = 8kHz	fs = 16kHz	fs = 48kHz	
00	1059/fs	132.4ms	66.2ms	22ms	(default)
01	267/fs	33.4ms	16.7ms	5.6ms	
10	531/fs	66.4ms	33.2ms	11.1ms	
11	135/fs	16.9ms	8.4ms	2.8ms	

Table 18. ADC Initialization Cycle

The DAC is initialized by setting PMDAC bit “0” → “1”. The initialization cycle is 2/fs. Therefore, the DAC outputs signals after group delay period and 2/fs when power up the device. Normally, this group delay period or 2/fs initialization cycle mentioned above is absorbed by power-up time of amplifiers after the DAC (Lineout-amp, SPK-amp).

■ Audio Interface Format

Four types of data formats are available and can be selected by setting the DIF1-0 bits (Table 19). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. FCK and BICK are output from the AK4637 in master mode, but must be input to the AK4637 in slave mode.

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	16bit DSP Mode	16bit DSP Mode	≥ 16fs	Table 20	
1	0	1	24/16bit MSB justified	16bit LSB justified	≥ 32fs	Figure 31	
2	1	0	24bit MSB justified	24bit MSB justified	≥ 48fs	Figure 32	(default)
3	1	1	24/16 bit I^2S Compatible	24/16 bit I^2S Compatible	=32fs or ≥ 48fs	Figure 33	

Table 19. Audio Interface Format

If 24-bit(or 16-bit) data that ADC outputs is converted to 8-bit data by removing LSB 16-bit(8-bit), "-1" at 24bit(16bit) data is converted to "-1" at 8-bit data. And when the DAC playbacks this 8-bit data, "-1" at 8-bit data will be converted to "-65536" at 24-bit ("-256" at 16-bit) data which is a large offset. This offset can be removed by adding the offset of "32768" at 24-bit ("128" at 16bit) to 24-bit(16-bit) data before converting to 8-bit data.

In Mode 1, 2 and 3, the SDTO is clocked out on the falling edge (" ↓ ") of BICK and the SDTI is latched on the rising edge (" ↑ ").

In Mode 0 (16bit DSP mode), the audio I/F timing is changed by BCKP and MSBS bits (Table 20).

DIF1 bit	DIF0 bit	MSBS bit	BCKP bit	Audio Interface Format	Figure	
0	0	0	0	MSB of SDTO is output by the rising edge ("↑") of the first BICK after the rising edge ("↑") of FCK. MSB of SDTI is latched by the falling edge ("↓") of the BICK just after the output timing of SDTO's MSB.	Figure 27	(default)
		0	1	MSB of SDTO is output by the falling edge ("↓") of the first BICK after the rising edge ("↑") of FCK. MSB of SDTI is latched by the rising edge ("↑") of the BICK just after the output timing of SDTO's MSB.	Figure 28	
		1	0	MSB of SDTO is output by next rising edge ("↑") of the falling edge ("↓") of the first BICK after the rising edge ("↑") of FCK. MSB of SDTI is latched by the falling edge ("↓") of the BICK just after the output timing of SDTO's MSB.	Figure 29	
		1	1	MSB of SDTO is output by next falling edge ("↓") of the rising edge ("↑") of the first BICK after the rising edge ("↑") of FCK. MSB of SDTI is latched by the rising edge ("↑") of the BICK just after the output timing of SDTO's MSB.	Figure 30	

Table 20. Audio Interface Format in Mode 0

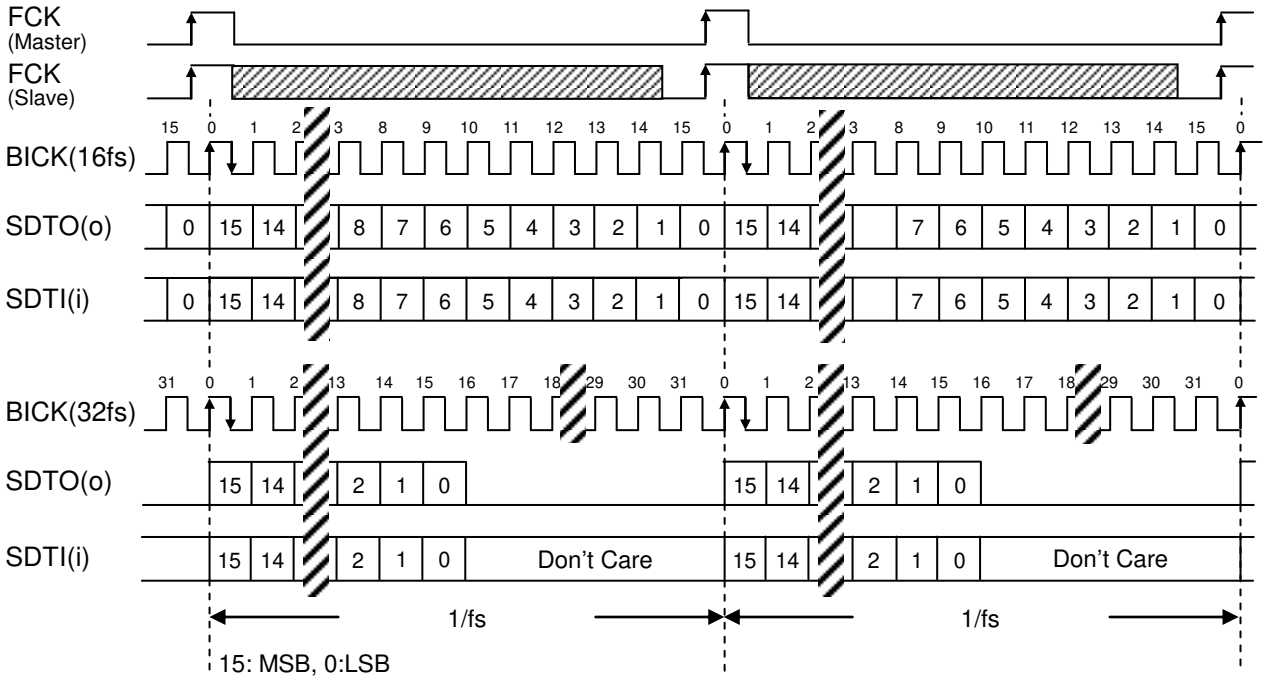


Figure 27. Mode 0 Timing (BCKP bit = "0", MSBS bit = "0")

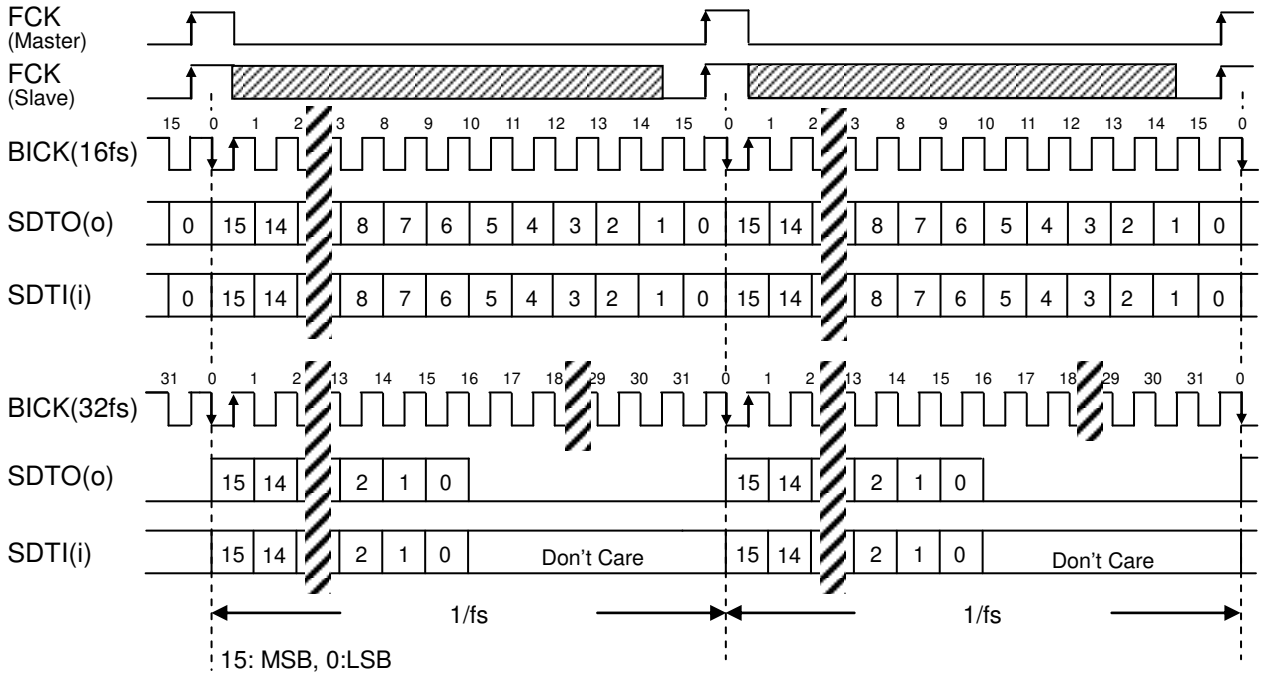


Figure 28. Mode 0 Timing (BCKP bit = "1", MSBS bit = "0")

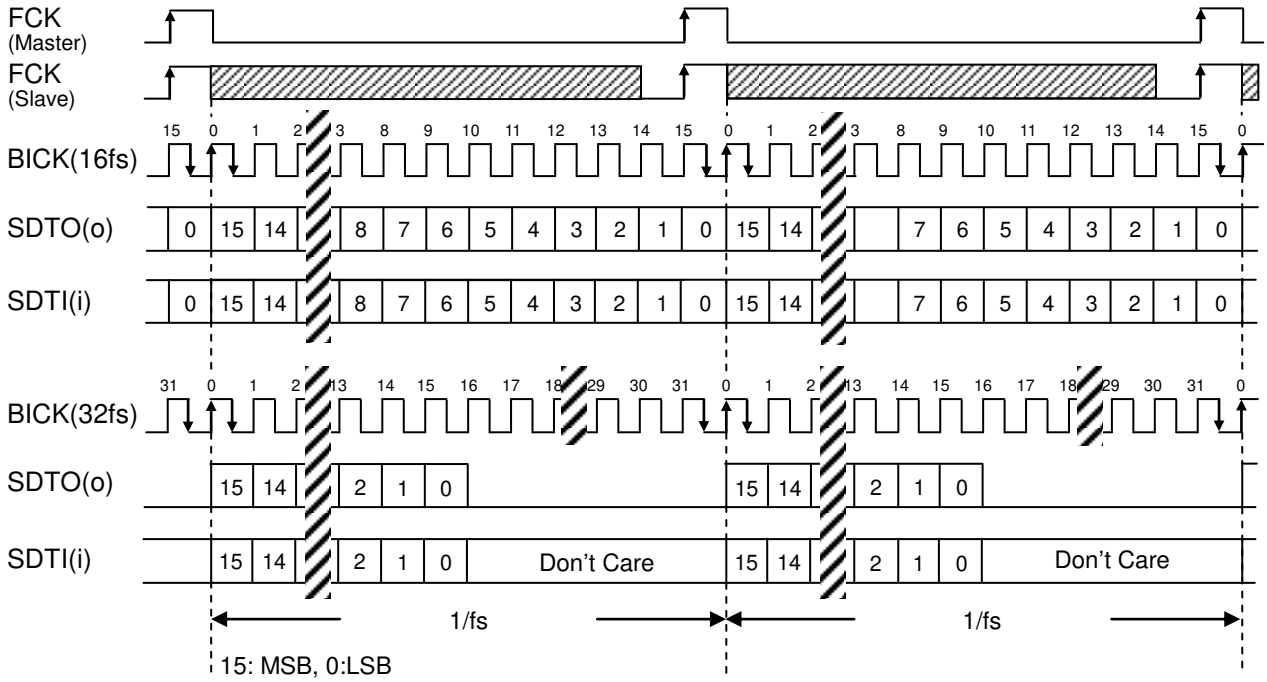


Figure 29. Mode 0 Timing (BCKP bit = "0", MSBS bit = "1")

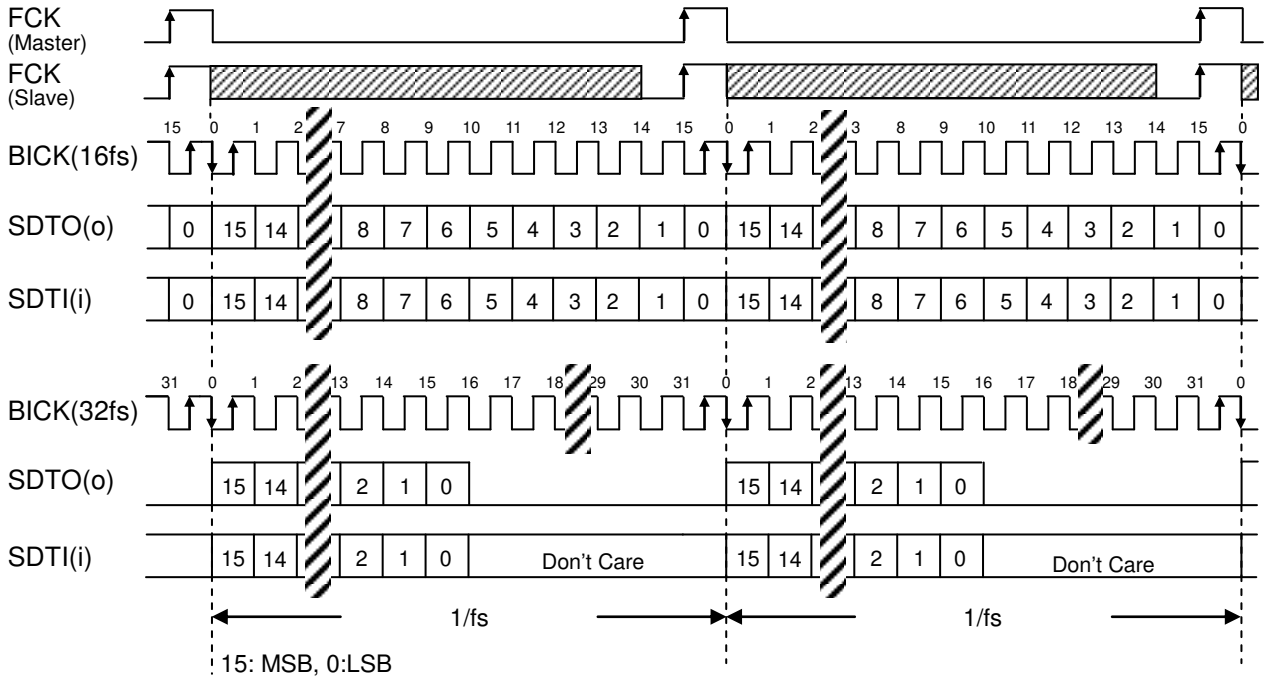


Figure 30. Mode 0 Timing (BCKP bit = "1", MSBS bit = "1")

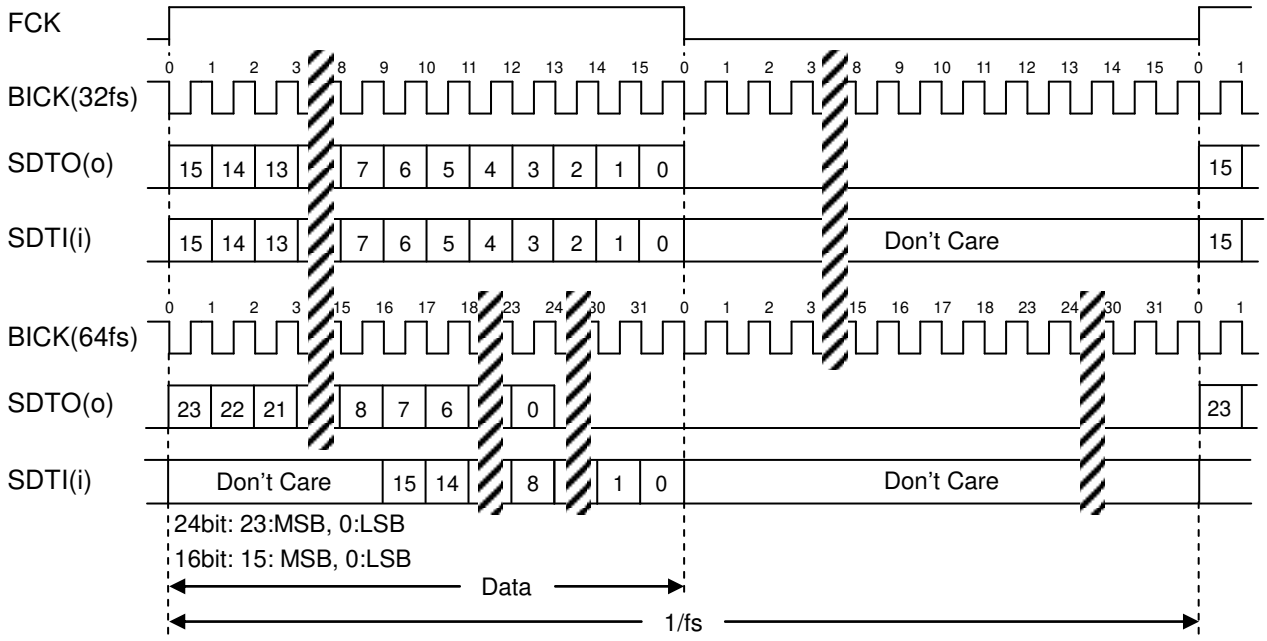


Figure 31. Mode 1 Timing

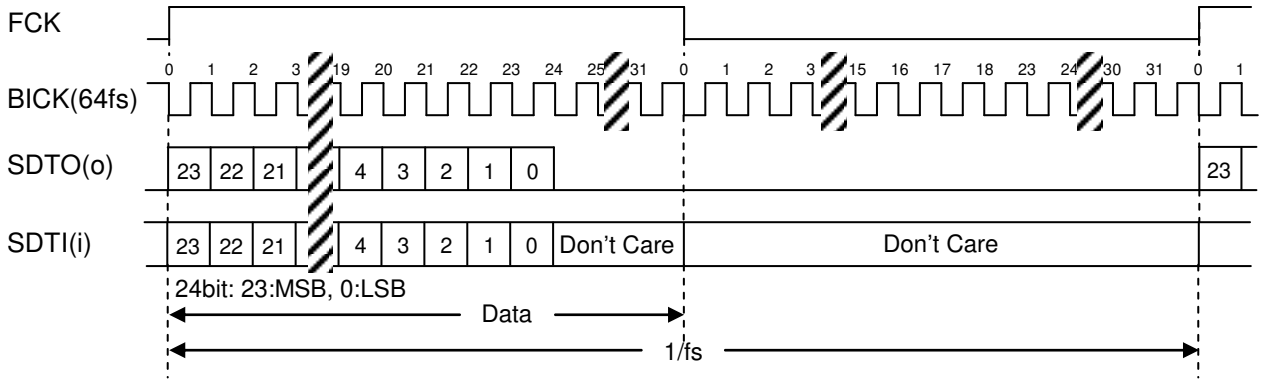


Figure 32. Mode 2 Timing

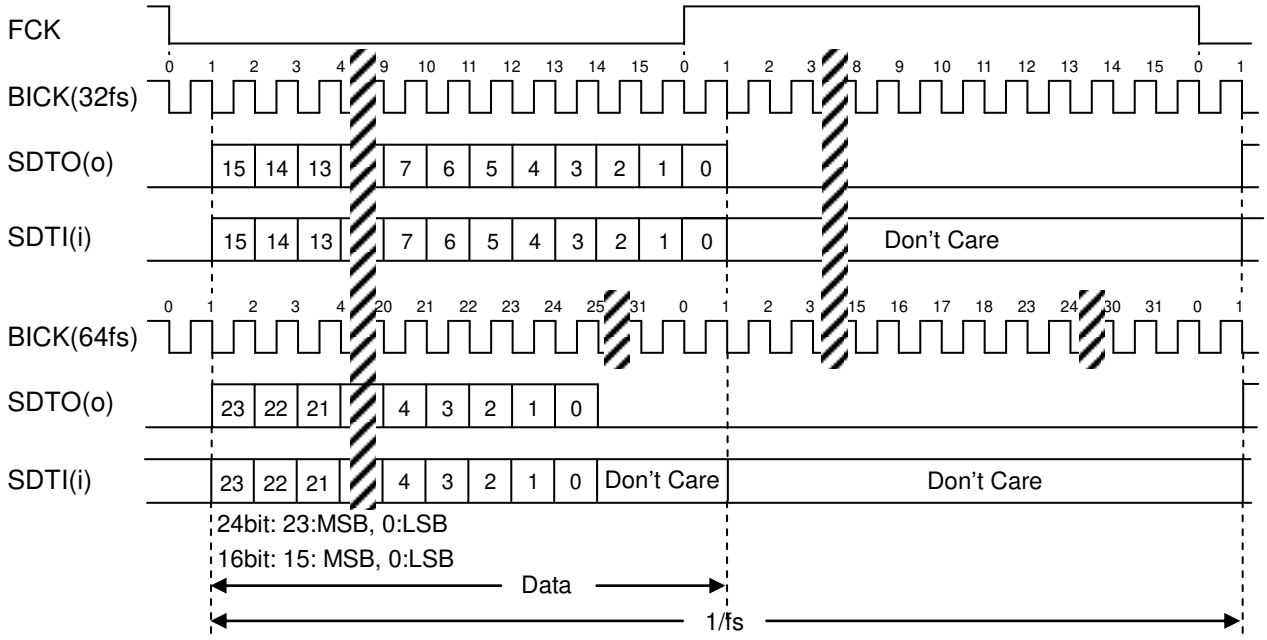


Figure 33. Mode 3 Timing

■ MIC/LINE Input Selector

The AK4637 has an input selector. MDIF bit select single-ended input and differential input. When MDIF bit = "0", the AIN pin is an input pin. Single-ended signal to the MIC-Amp can be input via the AIN pin. When MDIF bit = "1", the IN+ pin and the IN- pin are input pins. Differential signal can be input to these pins. At this time, the IN- pin cannot be used as the BEEP pin. When DMIC bit = "1", digital microphone input is selected regardless of MDIF bit.

DMIC bit	MDIF bit	MIC Input	
0	0	AIN pin	(default)
	1	IN+/– pins	
1	x	Digital MIC	

Table 21. MIC/Line In Path Select (x: Do not care, N/A: Not available)

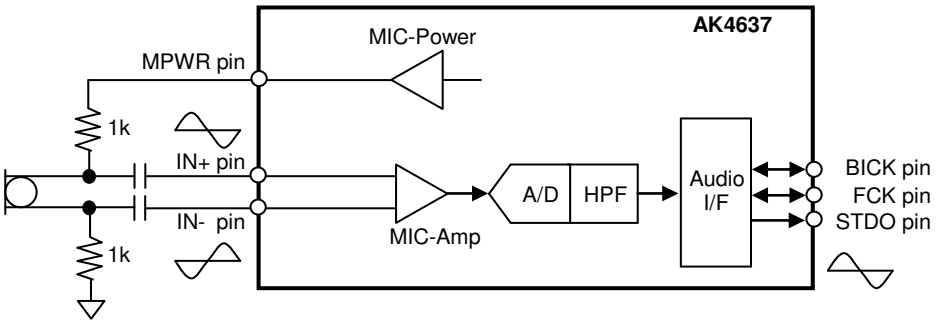


Figure 34. Differential Input Block Circuit (MDIF bit = "1")

■ Microphone Gain Amplifier

The AK4637 has a gain amplifier for microphone input. It is powered-up by PMADC bit = "1". The gain of MIC-Amp is selected by the MGAIN3-0 bits. When single-ended input, the typical input impedance is 30kΩ. When differential input, the typical input impedances are IN+=20kΩ and IN-=57kΩ@MGAIN3-0 bits = "0000" (0dB), IN+=16kΩ and IN-=244kΩ@MGAIN3-0 bits = "0110" (+18dB). A click noise may occur if the MIC-Amp gain is changed when both MIC-Amp and ADC (PMADC bit = "1") are powered up. High frequency characteristics are attenuated when MIC-Amp = +30dB. The attenuation amount of when MIC-Amp = +30dB is -0.5dB at 10kHz frequency and -1.5dB at 20kHz frequency comparing with when MIC-Amp = +18dB.

MGAIN3 bit	MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0	0dB	
0	0	0	1	+3dB	
0	0	1	0	+6dB	
0	0	1	1	+9dB	
0	1	0	0	+12dB	
0	1	0	1	+15dB	
0	1	1	0	+18dB	(default)
0	1	1	1	+21dB	
1	0	0	0	+24dB	
1	0	0	1	+27dB	
1	0	1	0	+30dB	
Others				N/A	

Table 22. Input Gain (N/A: Not available)

■ Microphone Power

When PMMP bit = “1”, the MPWR pin supplies the power for microphones. This output voltage is typically 2.4V @MICL bit =“0”, and typically 2.0V@MICL bit = “1”. The load resistance is minimum 2.0kΩ. Any capacitor must not be connected directly to the MPWR pin (Figure 35).

MICL bit	Output Voltage (typ)	
0	2.4V	(default)
1	2.0V	

Table 23. Microphone Power

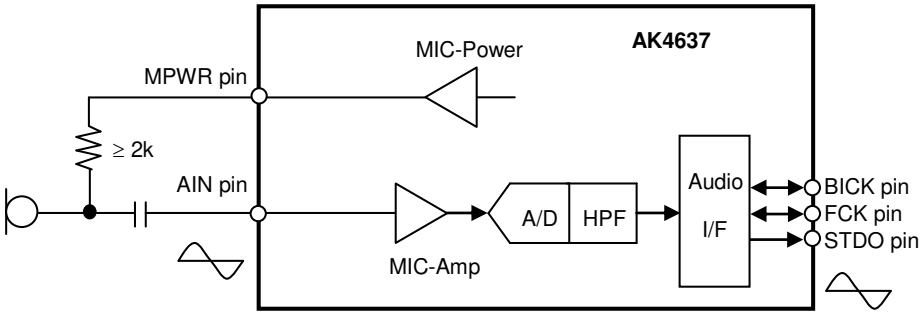


Figure 35. MIC Block Circuit (MDIF bit = “0”)

■ Digital Microphone

1. Connection to Digital Microphones

When DMIC bit is set to “1”, the AIN/IN+ and BEEP/IN- pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins, respectively. The same voltage as AVDD must be provided to the digital microphone. The Figure 36 shows mono connection examples. The DMCLK clock is input to a digital microphone from the AK4637. The digital microphone outputs 1bit data, which is generated by ΔΣModulator using DMCLK clock, to the DMDAT pin. PMDM bit control power up/down of the digital block (Decimation Filter and Digital Filter). (PMADC bit settings do not affect the digital microphone power management.) The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4637 is powered down (PDN pin= “L”), the DMCLK and DMDAT pins become floating state. Pull-down resistors must be connected to DMCLK and DMDAT pins externally to avoid this floating state. When the digital microphone is used, AVDD must be provided as 2.8~3.6V.

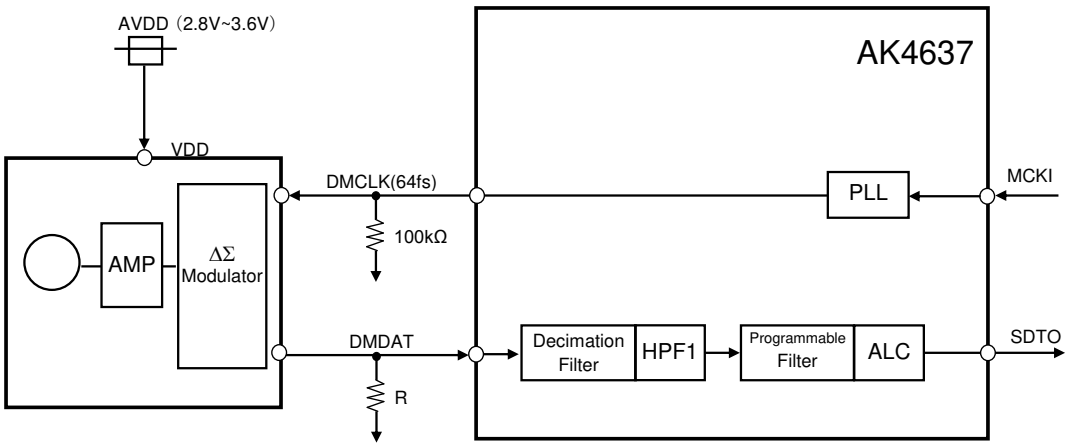


Figure 36. Connection Example of Monaural Digital Microphone

2. Interface

When DCLKP bit = “1”, data is input to the decimation filter while DMCLK = “H”. When DCLKP bit = “0”, data is input to the decimation filter while DMCLK pin= “L”. The DMCLK pin only supports 64fs. When DCLKE bit = “1”, DMCLK pin outputs 64fs. In this case, necessary clocks must be supplied to the AK4637 for ADC operation. When DCLKE bit = “0”, DMCLK pin outputs “L”. The Figure 37 and Figure 38 show the input and output timing. When DCLKP bit = “1”, Digital MIC outputs the data by the rising edge (“↑”) of DMCLK, and the AK4637 latches it by the falling edge (“↓”) of DMCLK. When DCLKP bit = “0”, Digital MIC outputs the data by the rising edge (“↓”) of DMCLK, and the AK4637 latches it by the falling edge (“↑”) of DMCLK. The output data through “the Decimation and Digital Filters” is 24bit full scale when the 1bit data density is 0%~100%.

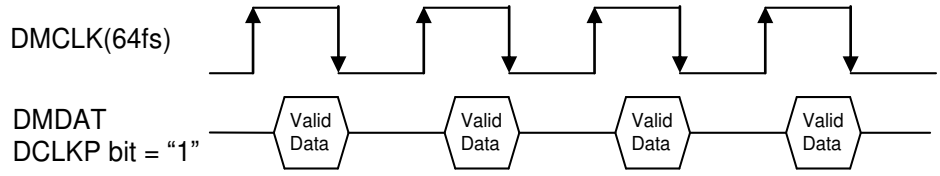


Figure 37. Data In/Output Timing with Digital Microphone (DCLKP bit = “1”)

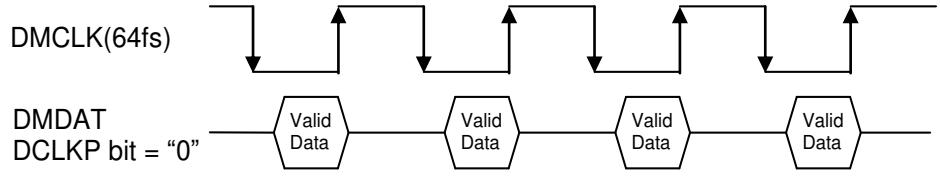
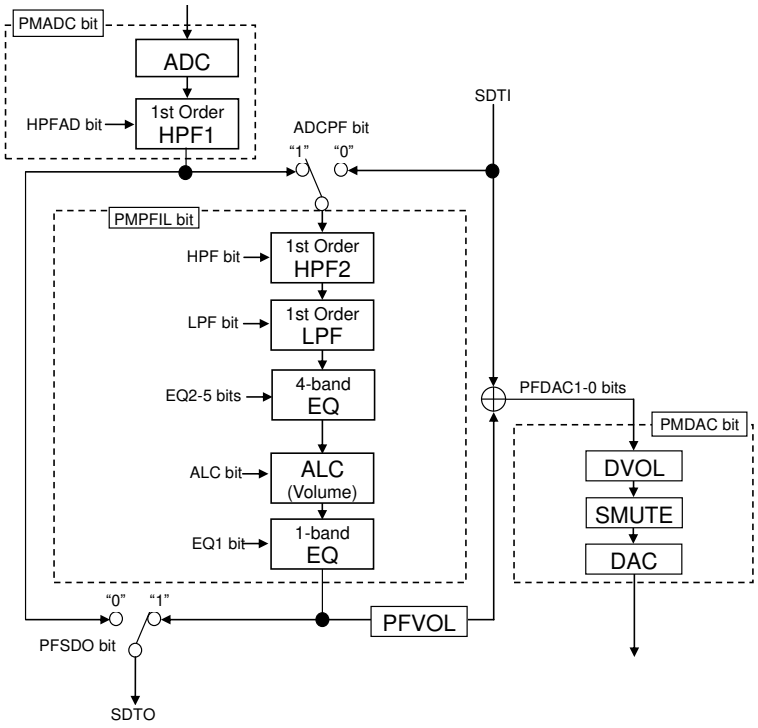


Figure 38. Data In/Output Timing with Digital Microphone (DCLKP bit = “0”)

■ Digital Block

The digital block consists of the blocks shown in Figure 39. Recording path and playback path is selected by setting ADCPF bit, PFDAC1-0 bits and PFSDO bit (Figure 40 ~ Figure 43, Table 24).



(1) ADC: Includes the Digital Filter (LPF) for ADC as shown in "Filter Characteristics".
(2) HPF1: High Pass Filter (HPF) for ADC as shown in "Digital HPF1".
(3) HPF2: High Pass Filter. (See "Digital Programmable Filter Circuit")
(4) LPF: Low Pass Filter (See "Digital Programmable Filter Circuit")
(5) 4 Band EQ: Applicable for use as Equalizer or Notch Filter.
(See "Digital Programmable Filter Circuit")
(6) ALC (Volume): Digital Volume with ALC Function.
(See "Input Digital Volume (Manual Mode)" and "ALC Operation")
(7) 1 Band EQ: Applicable for use as Notch Filter (See "Digital Programmable Filter Circuit")
(8) PFVOL: Sidetone digital volume (See "Sidetone digital Volume")
(9) DVOL: Digital volume for playback path (See "Output Digital Volume")
(10) SMUTE: Soft mute function (See "Soft Mute")

Figure 39. Digital Block Path Select

Mode Example	ADCPF bit	PFDAC1-0 bits	PFSDO bit	Figure
Recording Mode 1 & Playback Mode 2	1	00	1	Figure 40 (default)
Recording Mode 2 & Playback Mode 1	0	01	0	Figure 41
Recording Mode 2 & Playback Mode 2 (Programmable Filter Bypass Mode: PMPFIL bit = "0")	x	00	0	Figure 42
Loopback Mode	1	01	1	Figure 43

Table 24. Recording Playback Mode Example (x: Don't care)

When changing those modes, PMPFIL bit must be "0".

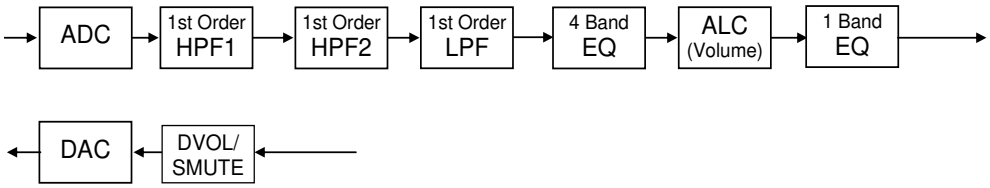


Figure 40. The Path in Recording Mode 1 & Playback Mode 2 (default)

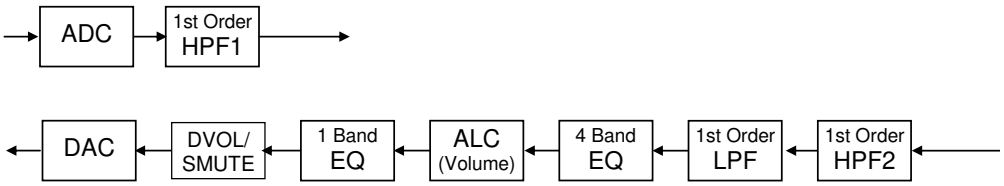


Figure 41. The Path in Recording Mode 2 & Playback Mode 1

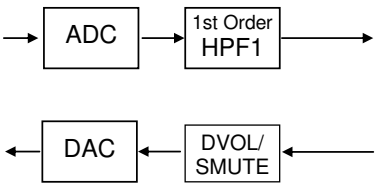


Figure 42. The Path in Recording Mode 2 & Playback Mode 2

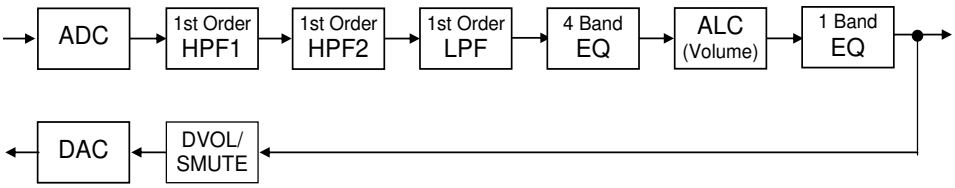


Figure 43. The Path in Loopback Mode

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies (fc) of the HPF1 are set by HPFC1-0 bits. It is proportional to the sampling frequency (fs) and the default value is 3.7Hz (@fs = 48kHz). HPFAD bit controls the ON/OFF of the HPF1 (HPF ON is recommended).

HPFC1 bit	HPFC0 bit	fc			
		fs=8kHz	fs=16kHz	fs=48kHz	
0	0	0.62Hz	1.2Hz	3.7Hz	(default)
0	1	2.47Hz	4.9Hz	14.8Hz	
1	0	19.7Hz	39.5Hz	118.4Hz	
1	1	39.5Hz	78.9Hz	236.8Hz	

Table 25. HPF1 Cut-off Frequency

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF2)

This is composed 1st order HPF. The coefficient of HPF is set by F1A13-0 bits and F1B13-0 bits. HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0" or HPF bit = "0". The HPF2 starts operation 4/fs (max) after when HPF bit = PMPFIL bit = "1" is set.

fs: Sampling Frequency
fc: Cutoff Frequency

Register Setting (Note 33)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.8Hz at 48kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0" or LPF bit = "0". The LPF starts operation 4/fs (max) after when LPF bit =PMPFIL bit= "1" is set.

fs: Sampling Frequency
fc: Cutoff Frequency

Register Setting (Note 33)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F2B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.05 (fc min = 2400Hz at 48kHz)

(3) 4-band Equalizer & 1-band Equalizer after ALC

This block can be used as equalizer or Notch Filter. 4-band equalizers (EQ2~EQ5) are switched ON/OFF independently by EQ2, EQ3, EQ4 and EQ5 bits. EQ1 bit controls ON/OFF switching of the equalizer after ALC (EQ1). When the equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0 bits, E1B15-0 bits and E1C15-0 bits set the coefficient of EQ1. E2A15-0 bits, E2B15-0 bits and E2C15-0 bits set the coefficient of EQ2. E3A15-0 bits, E3B15-0 bits and E3C15-0 bits set the coefficient of EQ3. E4A15-0 bits, E4B15-0 bits and E4C15-0 bits set the coefficient of EQ4. E5A15-0 bits, E5B15-0 bits and E5C15-0 bits set the coefficient of EQ5. The EQn (n=1, 2, 3, 4 or 5) coefficient must be set when EQn bit = "0" or PMPFIL bit = "0". EQn starts operation 4/fs(max) after when EQn = PMPFIL bit = "1" is set.

Each EQ2 ~ 5 blocks have a gain controller (EQ2G ~ EQ5G) independently after the equalizer. EQnG5-0 bits (n = 2~5) setting is reflected by writing "1" to EQCn bit (n = 2~5). EQnG5-0 bits and EQCn bit (n=2~5) can be set during operation (EQn =PMPFIL bit= "1").

fs: Sampling Frequency
fo_1 ~ fo_5: Center Frequency
fb_1 ~ fb_5: Band width where the gain is 3dB different from the center frequency
K_1 ~ K_5: Gain ($-1 \le K_n < 3$)

Register Setting (Note 33)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1 + \tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1 + \tan(\pi fb_n/fs)}, \quad C_n = -\frac{1 - \tan(\pi fb_n/fs)}{1 + \tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer Function

$$H(z) = \{1 + G_2 \times h_2(z) + G_3 \times h_3(z) + G_4 \times h_4(z) + G_5 \times h_5(z)\} \times \{1 + h_1(z)\}$$

$$(G_{2,3,4,5} = 1 \text{ or } G)$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

$$(n = 1, 2, 3, 4, 5)$$

The center frequency must be set as below.

$0.003 < fo_n / fs < 0.497$

When gain of K is set to "–1", this equalizer becomes a notch filter. When EQ2 ~EQ5 is used as a notch filter, central frequency of a real notch filter deviates from the above-mentioned calculation, if its central frequency of each band is near. The control soft that is attached to the evaluation board has functions that revises a gap of frequency and calculates the coefficient. When its central frequency of each band is near, the central frequency should be revised and confirm the frequency response.

Note 33. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]

X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement). MSB of each filter coefficient setting register is sine bit.

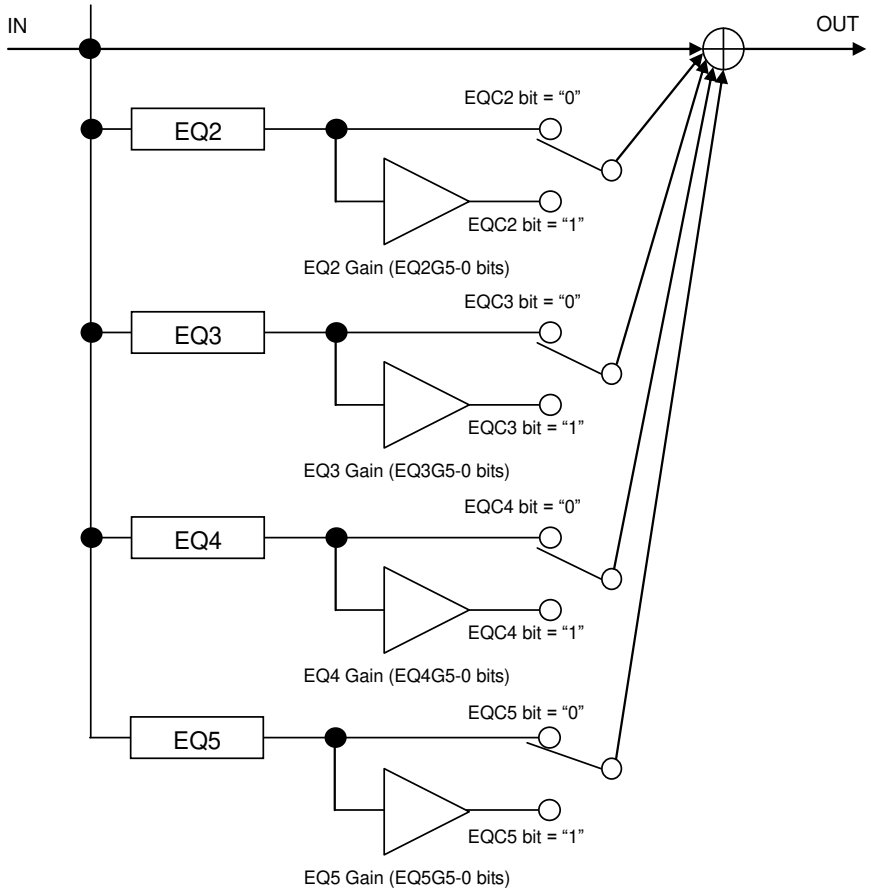


Figure 44. 4-Band EQ Structure

EQnG5-0 bits	EQG_DATA	Gain [dB]	Formula	
3FH	255	0	$20 \log_{10}$ (EQG_DATA/256)	
3EH	251	-0.17		
3DH	247	-0.31		
:				
02H	11	-27.34		
01H	7	-31.26		
00H	0	MUTE		(default)

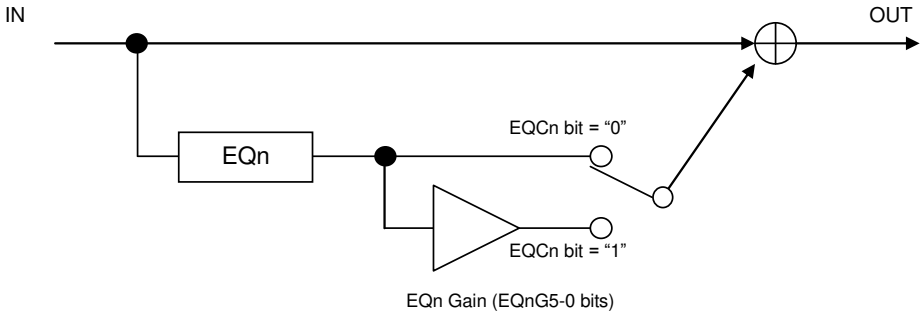
Table 26. EQn Gain Setting (n=2, 3, 4, 5)

EQnT1-0 bits	Transition Time of EQnG5-0 bits = 3FH ~ 00H			
	Setting Value	fs=8kHz	fs=48kHz	
00	256/fs	32ms	5.3ms	(default)
01	2048/fs	256ms	42.7ms	
10	8192/fs	1024ms	170.7ms	
11	16384/fs	2048ms	341.3ms	

Table 27. Transition Time of EQn Gain (n= 2, 3, 4, 5)

Common Gain Sequence Examples

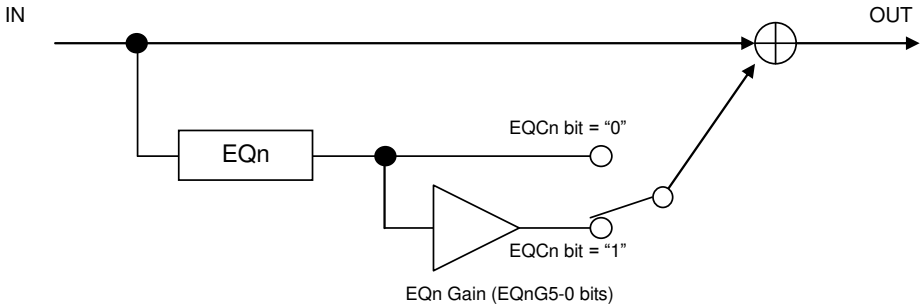
<When noise is generated>



(assuming the noise continues)

(1) Set EQCn bit: "1" → "0" (Path Setting). The gain changes immediately by this setting.
(2) Set EQnT1-0 bits: "xx" → "00" (Transition Time)
(3) Set EQnG5-0 bits: "xxH" → "3FH" (Gain Setting; should be set to 0dB)

<When noise is stopped>



(4) Set EQCn bit: "0" → "1" (Path Setting), EQnT1-0 bits Setting
(Transition Time: It should be set longer when noise is stopped.) (Note 34)
(5) Set EQnG5-0 bits (Gain Setting)
The gain of EQn is changed after a transition time set by EQnT1-0 bits.

Note 34. When changing a path of EQC2-5 by setting EQC2-5 bits "0" → "1", the gain should be transitioned to 0dB before the settings. Otherwise, pop noise may occur on the path change.

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block. When ADCPF bit is "1", the ALC circuit operates for recording path, and the ALC circuit operates for playback path when ADCPF bit is "0". ALC bit controls ON/OFF of ALC operation.

The ALC block consists of these blocks shown below. The ALC limiter detection level is monitored at the level detection2 block after EQ block. The level detection1 block also monitors clipping detection level (+0.53dBFS).

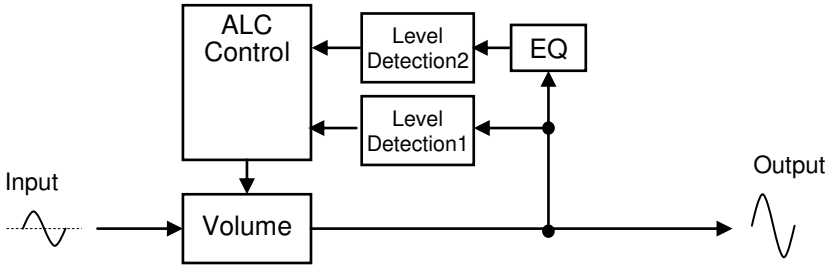


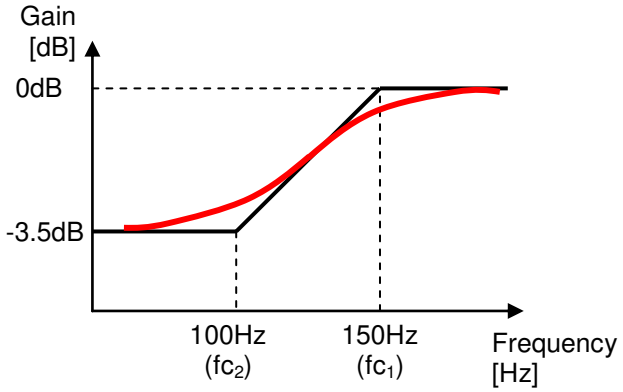
Figure 45. ALC Block

The polar (fc_1) and the zero point (fs_2) frequencies of EQ block are set by EQFC1-0 bits. Set EQFC bits according to the sampling frequency. When ALCEQ bit is OFF (ALCEQN bit = "1"), the level detection is not executed on this block.

EQFC1-0 bits	Sampling Frequency Range	Polar Frequency (fc_1)	Zero-point Frequency (fc_2)	
00	8kHz ≤ fs ≤ 12kHz	150Hz @ fs=12kHz	100Hz @ fs=12kHz	
01	12kHz < fs ≤ 24kHz	150Hz @ fs=24kHz	100Hz @ fs=24kHz	
10	24kHz < fs ≤ 48kHz	150Hz @ fs=48kHz	100Hz @ fs=48kHz	(default)
11	N/A			

Table 28. ALCEQ Frequency Setting (EQFC1-0 bits; N/A: Not available)

[ALCEQ: First order zero pole high pass filter]



Note 35. Black: Diagrammatic Line, Red: Actual Curve

Figure 46. ALCEQ Frequency Response (fs = 48kHz)

1. ALC Limiter Operation

During ALC limiter operation, when output level exceeds the ALC limiter detection level (Table 29), the VOL value is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 30). (Once this ALC limiter operation is started, attenuation will be repeated sixteen times.)

After completing the attenuate operation, unless ALC bit is changed to “0”, the operation repeats when the input signal level exceeds ALC limiter detection level.

LMTH2 bit	LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level	ALC Recovery Counter Reset Level	
0	0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
0	0	1	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –3.3dBFS	
0	1	0	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
0	1	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –5.0dBFS	
1	0	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	0	1	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –7.2dBFS	
1	1	0	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12.0dBFS	
1	1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –10.1dBFS	

Table 29. ALC Limiter Detection Level/ Recovery Counter Reset Level

Output	ATT Amount [dB]
+0.53dBFS ≤ Output Level (*)	0.38148
–1.16dBFS ≤ Output Level < +0.53dBFS	0.06812
LM-LEVEL ≤ Output Level < –1.16dBFS	0.02548

(*) Comparison with the next output data.

Table 30. ALC Limiter ATT Step

2. ALC Recovery Operation

ALC recovery operation wait for the WTM1-0 bits (Table 31) to be set after completing ALC limiter operation. If the input signal does not exceed “ALC recovery waiting counter reset level” (Table 29) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by the setting value of RGAIN2-0 bits (Table 32) up to the set reference level (Table 33) in every sampling. When the VOL value exceeds the reference level (REF value), the VOL values are not increased. The recovery speed gets slower when the VOL peak level exceeds -12dBFS to make the recovery speed for low VOL level faster relatively.

When
“ALC recovery waiting counter reset level ≤ Output Signal < ALC limiter detection level”
during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
“ALC recovery waiting counter reset level > Output Signal”,
the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When FRN bit = “0”, the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 34). When FRN bit = “1”, the fast recovery does not operate though the impulse noise is input. Limiter amount of Fast recovery is set by FRATT bit (Table 35).

WTM1 bit	WTM0 bit		ALC Recovery Cycle			
			8kHz	16kHz	48kHz	
0	0	128/fs	16ms	8ms	2.7ms	(default)
0	1	256/fs	32ms	16ms	5.3ms	
1	0	512/fs	64ms	32ms	10.7ms	
1	1	1024/fs	128ms	64ms	21.3ms	

Table 31. ALC Recovery Operation Waiting Period

RGAIN2 bit	RGAIN1 bit	RGAIN0 bit	GAIN Step [dB]	GAIN Change Timing	
0	0	0	0.00424	1/fs	(default)
0	0	1	0.00212	1/fs	
0	1	0	0.00106	1/fs	
0	1	1	0.00106	2/fs	
1	0	0	0.00106	4/fs	
1	0	1	0.00106	8/fs	
1	1	0	0.00106	16/fs	
1	1	1	0.00106	32/fs	

Table 32. ALC Recovery Gain Step

REF7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
06H	–52.125		
05H	–52.5		
04H~00H	MUTE		

Table 33. Reference Level of ALC Recovery Operation

RFST1-0 bits	Fast Recovery Gain Step [dB]	
00	0.0032	(default)
01	0.0042	
10	0.0064	
11	0.0127	

Table 34. Fast Recovery Speed Setting (FRN bit = “0”)

FRATT bit	ATT Amount [dB]	ATT Switch Timing	
0	-0.00106	4/fs	(default)
1	-0.00106	16/fs	

Table 35. Fast Recovery Reference Volume Attenuation Amount

3. The Volume at ALC Operation

The volume value during ALC operation is reflected in VOL7-0 bits. It is possible to check the current volume in 0.75dB step by reading the register value of VOL7-0 bits.

VOL7-0 bits	GAIN [dB]
FFH	+36.0 ≤ Gain
FEH	+35.25 ≤ Gain < +36.0
FCH	+34.5 ≤ Gain < +35.25
FAH	+33.75≤ Gain < +34.5
:	:
A2H	+0.75 ≤ Gain < +1.5
A0H	0.0 ≤ Gain < +0.75
9EH	-0.75 ≤ Gain < 0.0
:	:
12H	-53.25 ≤ Gain < -52.5
10H	-72 ≤ Gain < -53.25
00H	MUTE

Table 36. Value of VOL7-0 bits

4. Example of ALC Setting

Table 37 and Table 38 show the examples of the ALC setting for recording and playback path.

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH2-0	Limiter detection Level	010	−4.1dBFS	010	−4.1dBFS
FRN	Fast Recovery mode	0	Enable	0	Enable
WTM1-0	Recovery waiting period	01	32ms	11	21.3ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
RGAIN2-0	Recovery GAIN	000	0.00424dB	011	0.00106dB (2/fs)
RFST1-0	Fast Recovery GAIN	11	0.0127dB	00	0.0032dB
EQFC1-0	ALC EQ Frequency	00	fc1=100Hz, fc2=67Hz	10	fc1=150Hz, fc2=100Hz
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC	ALC enable	1	Enable	1	Enable

Table 37. Example of the ALC Setting (Recording)

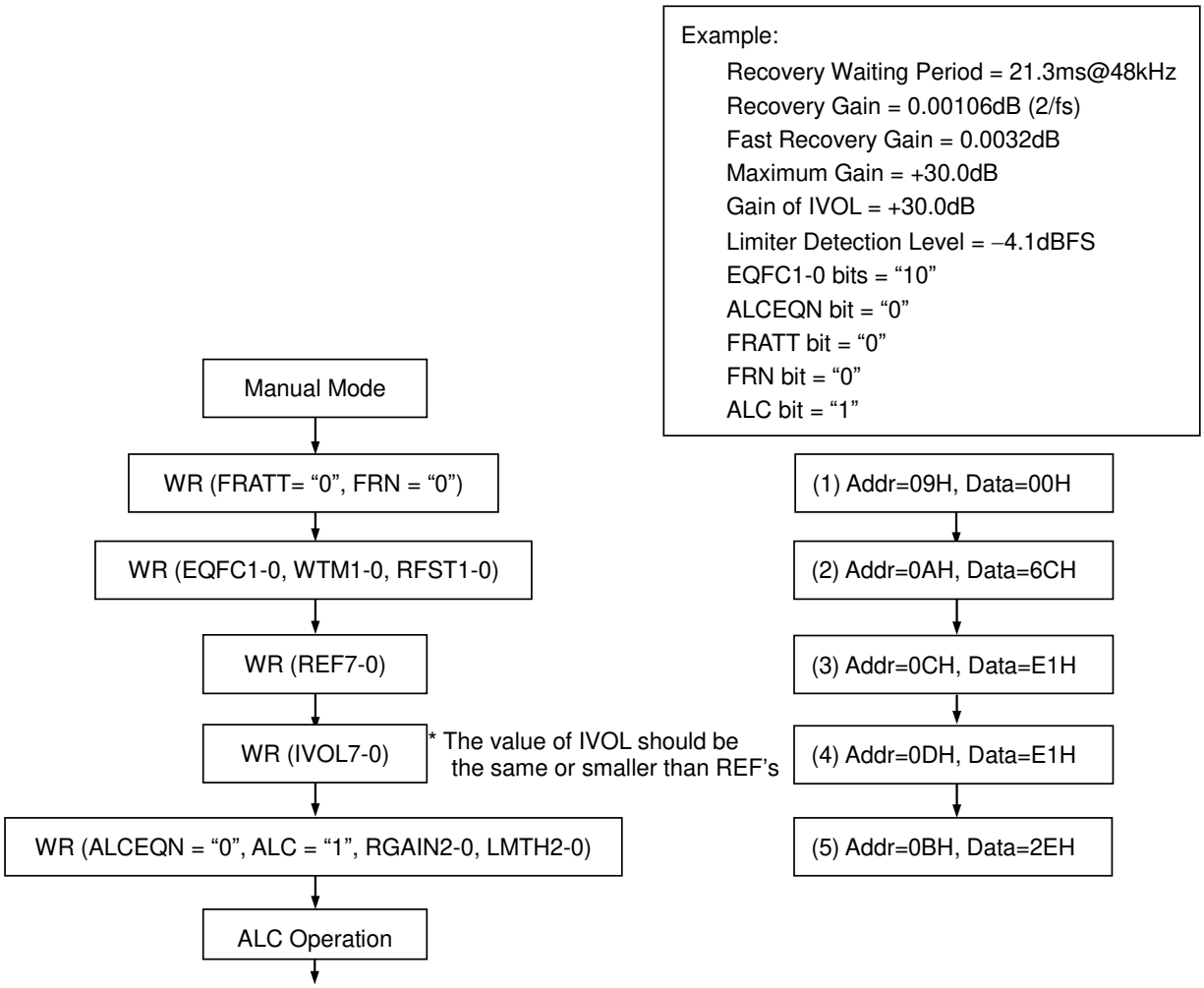
Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH2-0	Limiter detection Level	010	−4.1dBFS	010	−4.1dBFS
FRN	Fast Recovery mode	0	Enable	0	Enable
WTM1-0	Recovery waiting period	01	32ms	11	21.3ms
REF5-0	Maximum gain at recovery operation	28H	+6dB	28H	+6dB
IVL7-0, IVR7-0	Gain of IVOL	91H	0dB	91H	0dB
RGAIN2-0	Recovery GAIN	000	0.00424dB	011	0.00106dB (2/fs)
RFST1-0	Fast Recovery GAIN	11	0.0127dB	00	0.0032dB
EQFC1-0	ALC EQ Frequency	00	fc1=100Hz, fc2=67Hz	10	fc1=150Hz, fc2=100Hz
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC	ALC enable	1	Enable	1	Enable

Table 38. Example of the ALC Setting (Playback)

5. Example of registers set-up sequence of ALC Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is stopped by ALC bit = “0”. ALC output is “0” data until the AK4637 becomes manual mode after writing “0” to ALC bit.

LMTH2-0, WTM1-0, RGAIN2-0, REF7-0, RFST1-0, EQFC1-0, FRATT, FRN and ALCEQN bits



WR: Write

Figure 47. Registers Set-up Sequence at ALC Operation (Recording path)

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode when ALC bit is set to “0” while ADCPF bit is “1”. This mode is used in the cases shown below.

1. After exiting reset state, when setting up the registers for ALC operation (LMTH and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed. For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IVOL7-0 bits set the gain of the volume control (Table 39).

This volume has a soft transition function. Therefore no switching noise occurs during the transition. IVTM bit set the transition time (Table 40). When IVTM bit = “1”, it takes 944/fs (19.7ms@fs=48kHz) from F1H (+36dB) to 05H (-52.5dB). The volume is muted after transitioned to -72dB in the period set by IVTM bit when changing the volume from 05H (-52.5dB) to 00H (MUTE).

IVOL7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		(default)
E0H	+29.625		
:	:		
92H	+0.375		
91H	0.0		
90H	−0.375		
:	:		
06H	−52.125		
05H	−52.5		
04H~00H	MUTE		

Table 39. Input Digital Volume Setting

IVTM bit	Transition Time of Input Digital Volume IVOL7-0 bits = “F1H” → “05H”			
	Setting Value	fs=8kHz	fs=48kHz	
0	236/fs	29.5ms	4.9ms	
1	944/fs	118ms	19.7ms	(default)

Table 40. Transition Time of Input Digital Volume

If IVOL7-0 bits are written during PMPFIL bit = “0”, IVOL operation starts with the written values after PMPFIL bit is changed to “1”.

■ Sidetone Digital Volume

The AK4637 has the digital volume control (4 levels, 6dB step) for the programmable filter output.

PFVOL1-0 bits	Gain	
00	0dB	(default)
01	-6dB	
10	-12dB	
11	-18dB	

Table 41. Sidetone Digital Volume

■ DAC Input Selector

PFDAC1-0 bits select the signal of the DAC input or set the data mixing for each channel data.

PFDAC1 bit	PFDAC0 bit	DAC Input Signal	
0	0	SDTI	(default)
0	1	PFVOL Output	
1	0	(SDTI + PFVOL) / 2	
1	1	N/A	

Table 42. DAC Input Selector (N/A: Not available)

■ Output Digital Volume

The AK4637 has a digital output volume (205 levels, 0.5dB step, Mute). The volume is included in front of a DAC block. The input data of DAC is changed from +12 to –89.5dB or MUTE. DVOL7-0 bits control volume. This volume has soft transition function. In automatic attenuation, the volume is attenuated by soft transition in 204/fs or 816/fs to reduce switching noises. When DVTM bit = “0”, it takes 816/fs (17.0ms@fs=48kHz) from 00H (+12dB) to CCH (MUTE).

DVOL7-0 bits	Gain	Step	
00H	+12.0dB	0.5dB	(default)
01H	+11.5dB		
02H	+11.0dB		
:	:		
18H	0dB		
:			
CAH	–89.0dB		
CBH	–89.5dB		
CCH~FFH	Mute (– ∞)		

Table 43. Output Digital Volume Setting

DVTM bit	Transition Time between DVL/R7-0 bits = 00H and CCH			
	Setting	fs=8kHz	fs=48kHz	
0	816/fs	102ms	17.0ms	(default)
1	204/fs	25.5ms	4.3ms	

Table 44. Transition Time Setting of Output Digital Volume

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set "1", the output signal is attenuated by -∞ ("0") from the value (ATT DATA) set by DVOL7-0 bits during the cycle set by DVTM bit. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to ATT DATA from -∞ during the cycle set by DVTM bit. If the soft mute is cancelled within the cycle set by DVTM bit after starting the operation, the attenuation is discontinued and returned to ATT DATA. The soft mute is effective for changing the signal source without stopping the signal transaction.

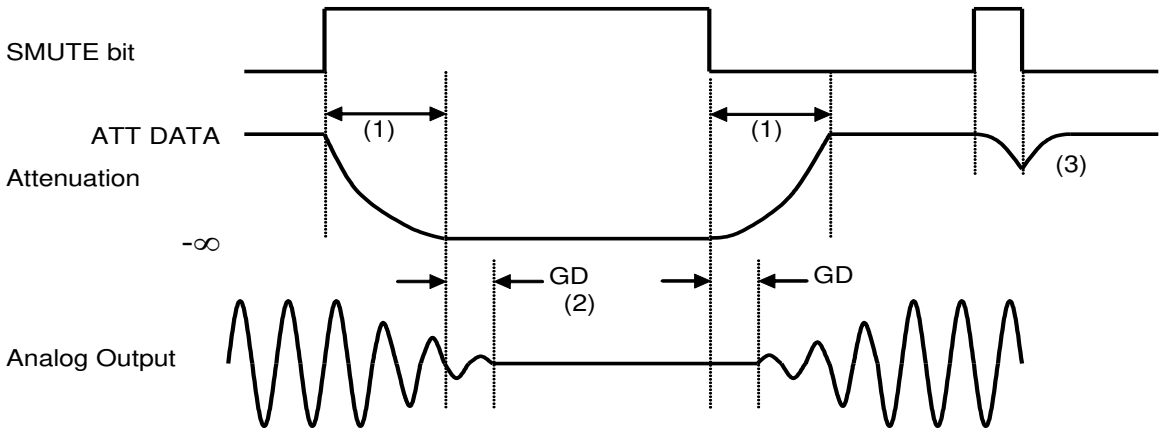


Figure 48. Soft Mute Function

(1) The input signal is attenuated to −∞ ("0") in the cycle set by DVTM bit. When ATT DATA = +12dB (DVOL7-0 bits = 00H), 816/fs = 17ms@ fs=48kHz, DVTM bit= "0".
(2) Analog output corresponding to digital input has group delay (GD).
(3) If soft mute is cancelled before attenuating to −∞, the attenuation is discounted and returned to the level set by DVOL7-0 bits within the same cycle.

■ BEEP Input

When BEEPS bit is set to “1” during PMBP = PMSL = SPLSN bits = “1”, the input signal from the BEEP pin is output to the speaker amplifier (LOSEL bit = “0”) or mono line output (LOSEL bit = “1”). When BEEP input is performed, MDIF bit must be set to “0”. BPLVL3-0 bits set the gain of BEEP-Amp. The total gain is defined according to SPKG1-0 bits setting when speaker amplifier is performed, and LVCM1-0 bits when mono line output is performed.

Input BEEP gain is controlled by BPLVL3-0 bits (Table 45).

BPLVL3 bit	BPLVL2 bit	BPLVL1 bit	BPLVL0 bit	BEEP Gain	
0	0	0	0	0dB	(default)
0	0	0	1	–6dB	
0	0	1	0	–12dB	
0	0	1	1	–18dB	
0	1	0	0	–24dB	
0	1	0	1	–30dB	
0	1	1	0	–33dB	
0	1	1	1	–36dB	
1	0	0	0	–39dB	
1	0	0	1	–42dB	
Others				N/A	

Table 45. BEEP Output Gain Setting (N/A: Not available)

BPVCM bit set the common voltage of BEEP input amplifier (Table 46).

BPVCM bit	BEEP-Amp Common Voltage (typ)	
0	1.15V	(default)
1	1.65V (Note 14, Note 36)	

Note 14. The maximum value is the smaller one of AVDD Vpp or 3.3Vpp when BPVCM bit = “1”. However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (Set by BPLVL3-0 bits)

Note 36. When the BEEP signal is output to the speaker amplifier and BPVCM bit = “1”, AVDD must be supplied 2.8V or more.

Table 46. Common Potential Setting of BEEP-Amp

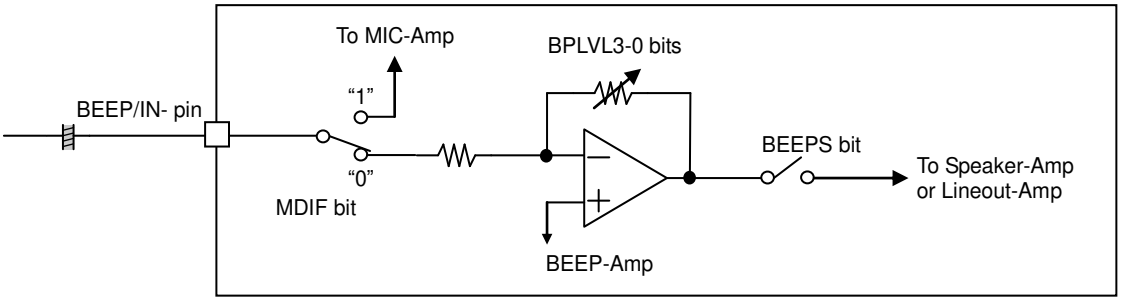


Figure 49. Block Diagram of BEEP pin

■ Speaker Output (SPP/SPN pins, LOSEL bit = “0”)

When LOSEL bit = “0”, the DAC output signal is input to the speaker amplifier. The speaker amplifier has mono output as it is BTL capable. The gain and output level are set by SPKG1-0 bits. The output level depends on AVDD and SPKG1-0 bits setting.

SPKG1-0 bits	Gain	SPK-Amp Output Level (DAC Input =0dBFS, AVDD=3.3V)	
00	+6.4dB	3.36Vpp	(default)
01	+8.4dB	4.23Vpp (Note 37)	
10	+11.1dB	5.76Vpp (Note 37)	
11	+14.9dB	8.90Vpp (AVDD=5.0V; Note 37)	

Note 37. The output level is calculated on the assumption that the signal is not clipped. However, in the actual case, the SPK-Amp output signal is clipped when DAC outputs 0dBFS signal. The SPK-Amp output level should be kept under 4.0Vpp (AVDD=3.3V) by adjusting digital volume to prevent clipped noise.

Table 47. SPK-Amp Gain

< Speaker-Amp Control Sequence >

The speaker amplifier is powered-up/down by PMSL bit. When PMSL bit is “0” at LOSEL bit = “0”, SPP pin is pulled-down to VSS1 by 100kΩ (typ) and the SPN pin is placed in a Hi-Z state. When PMSL bit is “1” and SLPSN bit is “0” at LOSEL bit = “0”, the speaker amplifier enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs AVDD/2 voltage.

When the PMSL bit is “1” at LOSEL bit = “0” after the PDN pin is changed from “L” to “H”, the SPP and SPN pins rise up in power-save mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to AVDD/2 voltage. Because the SPP and SPN pins rise up in power-save mode, pop noise can be reduced. When the AK4637 is powered-down (PMSL bit = “0”), pop noise can also be reduced by first entering power-save-mode.

PMSL bit	SLPSN bit	Mode	SPP pin	SPN pin	
0	x	Power-down	Pull-down to VSS1	Hi-Z	(default)
1	0	Power-save	Hi-Z	AVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 48 Speaker-Amp Mode Setting (x: Don’t care)

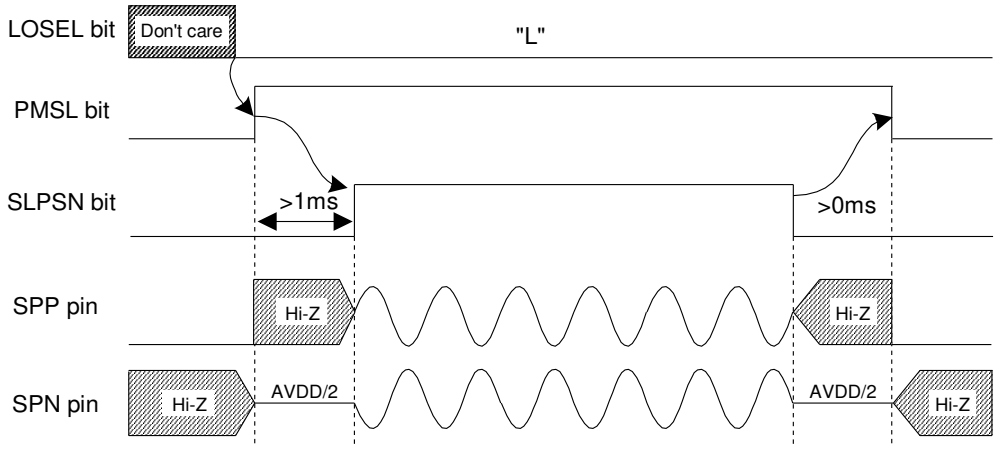


Figure 50. Power-up/Power-down Timing for Speaker-Amp

■ Thermal Shutdown Function

When the internal temperature of the device rises up irregularly (e.g. Output pins of speaker-amp are shortened), the speaker-amp and the lineout-amp are automatically powered down and then THDET bit becomes “1” (thermal shutdown). When TSDSEL bit = “0” (default), the internal temperature goes down and the thermal shutdown is released, the speaker-amp or the lineout-amp is powered up automatically and THDET bit returns to “0”. When TSDSEL bit = “1”, these blocks will not return to a normal operation until being reset by the PDN pin. THDET bit becomes “0” by this PDN pin reset.

■ Monaural Line Output (AOUT pin, LOSEL bit = “1”)

When LOSEL bit is set to “1”, the output signal of DAC is output in single-ended format via AOUT pin. The monaural line output is valid at AVDD = 2.8~3.6V. When DACL bit is “0” at LOSEL = PMSL = SLPSN bits = “1”, output signal is muted and AOUT pin output common voltage. The load impedance is 10kΩ (min.). When PMSL bit = “0” at LOSEL = SLPSN bits = “1”, the monaural line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). Pop noise at power-up/down can be reduced by changing PMSL bit when SLPSN bit = “0” at LOSEL bit = “1”. In this case, output signal line should be pulled-down to VSS1 by 22kΩ after AC coupled as Figure 52. Rise/Fall time is 300ms (max) when C=1μF and R_L=10kΩ. When LOSEL = PMSL = SLPSN bits = “1”, monaural line output is in normal operation.

LVCM1-0 bits set the gain of monaural line output.

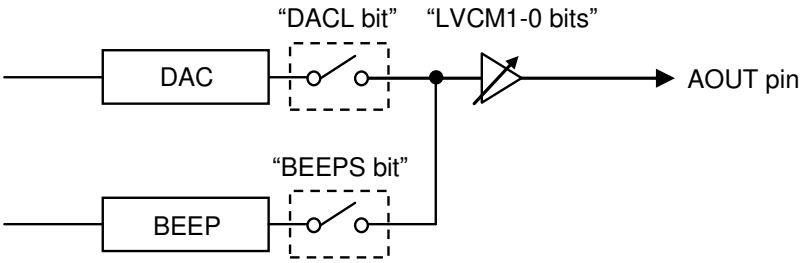


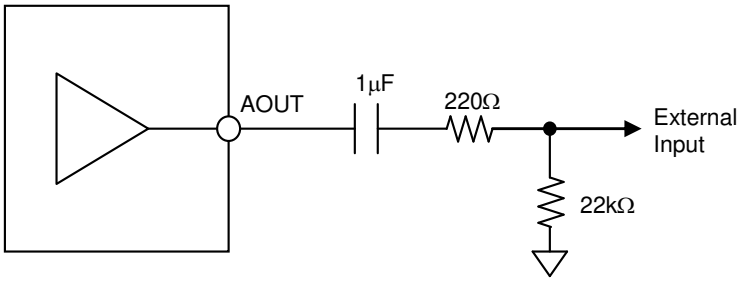
Figure 51. Monaural Line Output

PMSL bit	SLPSN bit	Mode	AOUT pin	
0	0	Power Down	Fall-down to VSS1	(default)
	1	Power Down	Pull-down to VSS1	
1	0	Power Save	Rise up to Common Voltage	
	1	Normal Operation	Normal Operation	

Table 49. Monaural Line Output Mode Select

LVCM1-0 bits	AVDD	Gain	Common Voltage (typ)	
00	2.8 ~ 3.6V	0dB	1.3V	
01	3.0 ~ 3.6V	+2dB	1.5V	(default)
10	2.8 ~ 3.6V	+2dB	1.3V	
11	3.0 ~ 3.6V	+4dB	1.5V	

Table 50. Monaural Lineout Volume Setting



Note 38. If the value of 22kΩ resistance at pop noise reduction circuit is increased, the power-up time of Monaural line output is increased but the pop noise level is not decreased. Do not use a resistor less than 22kΩ at the pop noise reduction circuit since the line output drivability is minimum 10kΩ.

Figure 52. External Circuit for Monaural Line Output (in case of using a Pop Noise Reduction Circuit)

[Monaural Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)]

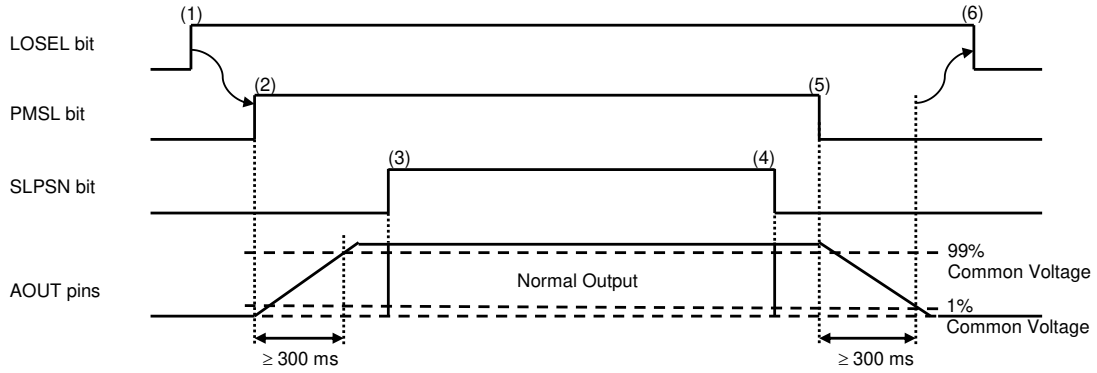


Figure 53. Monaural Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)

(1) Set LOSEL bit = “1”. Enable monaural line output.
(2) Set PMSL bit = “1”. Monaural line output exits power-down mode.
AOUT pin rises up to common voltage. Rise time to 99% common voltage is 200ms (max. 300ms) when C=1μF.
(3) Set SLPSN bit = “1” after AOUT pin rises up. Monaural line output exits power-save mode.
Monaural line output is enabled.
(4) Set SLPSN bit = “0”. Monaural line output enters power-save mode.
(5) Set PMSL bit = “0”. Monaural line output enters power-down mode.
AOUT pin falls down to 1% of the common voltage. Fall time is 200ms (max. 300ms) when C=1μF.
(6) Set LOSEL bit = “0” after wait time (≥300ms). Disable monaural line output.

[Monaural Line Output Control Sequence (SLPSN bit = “1”: in case of not using a Pop Noise Reduction Circuit)]

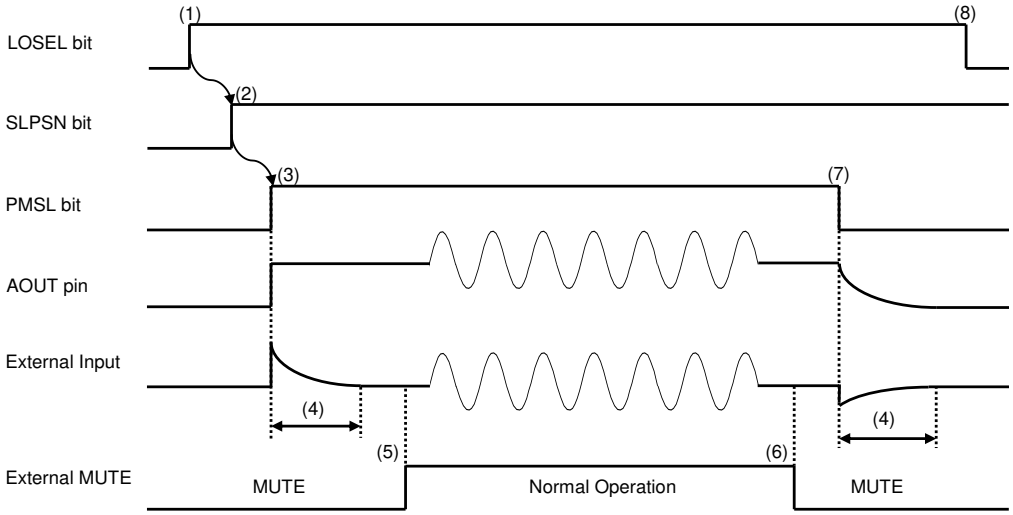


Figure 54. Monaural Line Output Control Sequence
(SLPSN bit = “1”: in case of not using a Pop Noise Reduction Circuit)

(1) Set LOSEL bit = “1”. Enable monaural line output.
(2) Set SLPSN bit = “1”. Pop noise reduction circuit is disabled.
(3) Set PMSL bit = “1”. Monaural line output is powered-up.
AOUT pin rises up to common voltage.
(4) Time constant is defined according to external capacitor (C) and resistor (R_L).
(5) Release external MUTE when the external input is stabled.
Monaural line output is enabled.
(6) Set external MUTE ON
(7) Set PMSL bit = “0”. Monaural line output is powered-down.
AOUT pin fall down.
(8) Set LOSEL bit = “0” after wait time (≥300ms). Disable monaural line output.

■ Regulator Block

The AK4637 integrates a regulator. The 3.3V (typ) power supply voltage from the AVDD pin is converted to 2.3V (typ) by the regulator and supplied to the analog blocks (MIC-Amp, ADC, DAC, BEEP). The regulator is powered up by PMVCM bit = “1”, and powered down by PMVCM = “0”. Connect a 2.2µF (± 10%) capacitor to the REGFIL pin to reduce noise on AVDD.

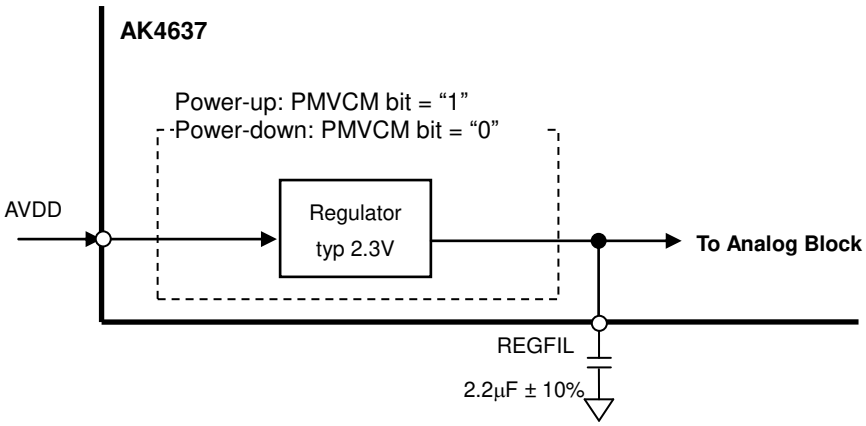


Figure 55 Regulator Block

■ Serial Control Interface

The AK4637 supports the fast-mode I²C Bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to a voltage in the range from TVDD or more to 6V or less.

1. WRITE Operations

Figure 56 shows the data transfer sequence for the I²C Bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 62). After the START condition, a slave address is sent. This address is seven bits of the slave address are fixed as "0010010" and the next bit is a data direction bit (R/W) (Figure 57). If the slave address matches that of the AK4637, the AK4637 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 63). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4637. The format is MSB first, and those most significant 1bit is fixed to zero (Figure 58). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 59). The AK4637 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 62).

The AK4637 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4637 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. The address counter will "roll over" to 00H and the previous data will be overwritten if the address exceeds "3FH" prior to generating a stop condition.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 64) except for the START and STOP conditions.

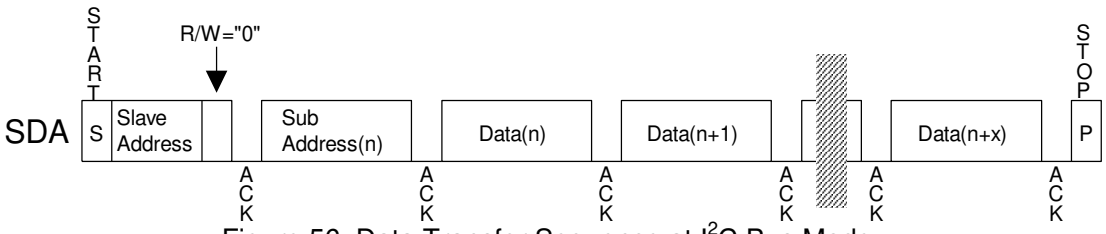


Figure 56. Data Transfer Sequence at I²C Bus Mode

0	0	1	0	0	1	0	R/W

Figure 57. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 58. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 59. The Third Byte

2. READ Operations

Set the R/W bit = “1” for the READ operation of the AK4637. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. The address counter will “roll over” to 00H and the data of 00H will be read out if the address exceeds “3FH” of Register map prior to generating a stop condition.

The AK4637 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4637 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4637 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4637 ceases the transmission.

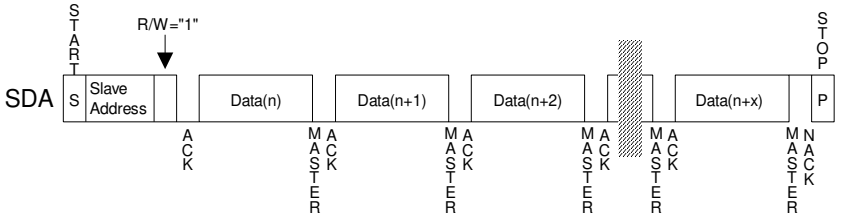


Figure 60. Current Address Read

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4637 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4637 ceases the transmission.

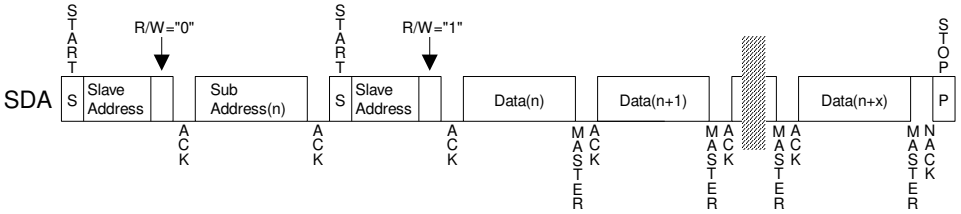


Figure 61. Random Address Read

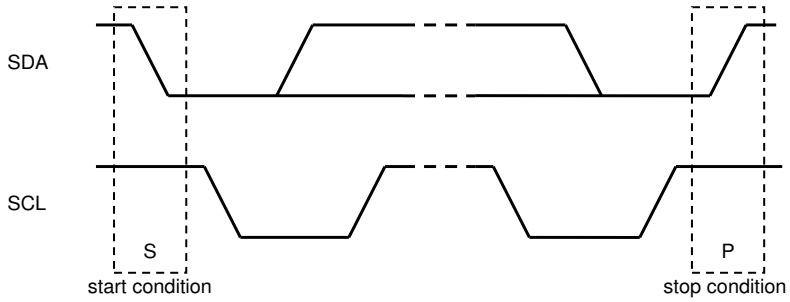


Figure 62. Start Condition and Stop Condition

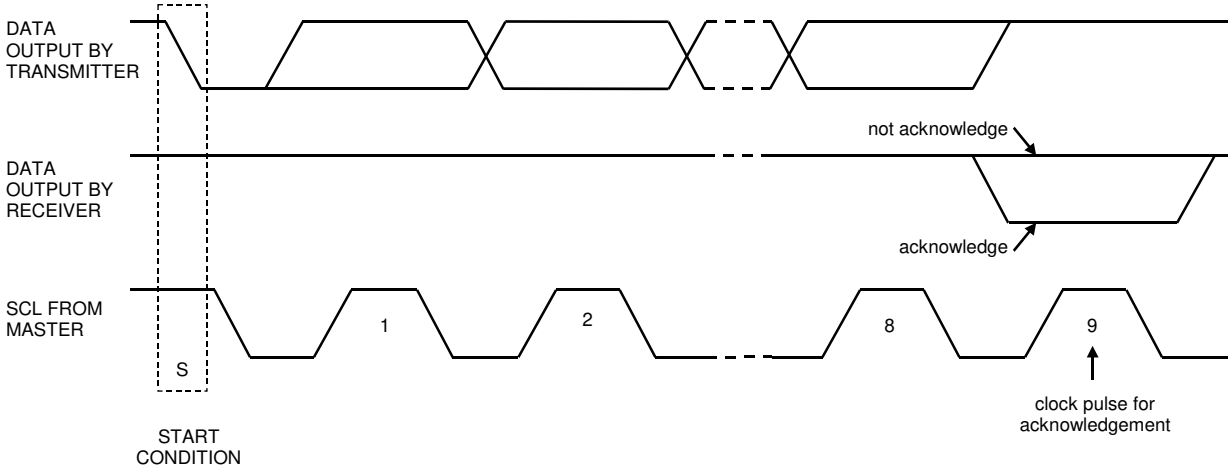


Figure 63. Acknowledge (I^2C Bus)

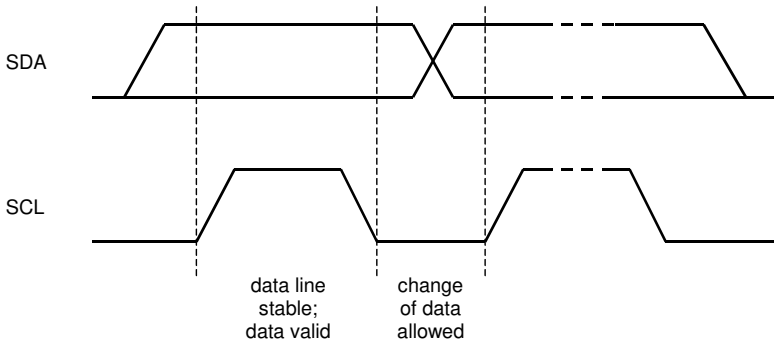


Figure 64. Bit Transfer (I^2C Bus)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	LOSEL	PMDAC	0	PMADC
01H	Power Management 2	0	0	0	0	M/S	PMPLL	PMSL	0
02H	Signal Select 1	SLPSN	MGAIN3	DACS	0	PMMP	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SPKG1	SPKG0	0	MICL	0	0	0	MDIF
04H	Signal Select 3	LVCM1	LVCM0	DACL	0	0	0	0	0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	0	CKOFF	BCKO1	BCKO0
06H	Mode Control 2	CM1	CM0	0	0	FS3	FS2	FS1	FS0
07H	Mode Control 3	TSDSEL	THDET	SMUTE	0	MSBS	BCKP	DIF1	DIF0
08H	Digital MIC	0	0	0	PMDM	DCLKE	0	DCLKP	DMIC
09H	Timer Select	ADRST1	ADRST0	FRATT	FRN	0	0	0	DVTM
0AH	ALC Timer Select	0	IVTM	EQFC1	EQFC0	WTM1	WTM0	RFST1	RFST0
0BH	ALC Mode Control 1	ALCEQN	LMTH2	ALC	RGAIN2	RGAIN1	RGAIN0	LMTH1	LMTH0
0CH	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0DH	Input Volume Control	IVOL7	IVOL6	IVOL5	IVOL4	IVOL3	IVOL2	IVOL1	IVOL0
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0FH	BEEP Control	0	BPVCM	BEEPS	0	BPLVL3	BPLVL2	BPLVL1	BPLVL0
10H	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
11H	EQ Common Gain Select	0	0	0	EQC5	EQC4	EQC3	EQC2	0
12H	EQ2 Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
13H	EQ3 Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
14H	EQ4 Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
15H	EQ5 Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0
16H	Digital Filter Select 1	0	0	0	0	0	HPFC1	HPFC0	HPFAD
17H	Digital Filter Select 2	0	0	0	0	0	0	LPF	HPF
18H	Digital Filter Mode	0	0	PFVOL1	PFVOL0	PFDAC1	PFDAC0	ADCPF	PFSDO
19H	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1AH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1BH	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1CH	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
1DH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
1EH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
1FH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
20H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
21H	Digital Filter Select 3	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
22H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
23H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
24H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
25H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
26H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
27H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
28H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
29H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
2AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
2BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
2CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
2DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
2EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
2FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
31H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
32H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
33H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
34H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
35H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
36H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
37H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
38H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
39H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
3AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
3BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
3CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
3DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
3EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
3FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

Note 39. PDN pin = “L” resets the registers to their default values.
Note 40. The bits defined as 0 must contain a “0” value.
Note 41. Writing access to 40H ~ 7FH is prohibited.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	LOSEL	PMDAC	0	PMADC
R/W		R/W	R/W	R/W	R	R/W	R/W	R	R/W
Default		0	0	0	0	0	0	0	0

PMADC: Microphone Amplifier and ADC Power Management
0: Power-down (default)
1: Power-up
When the PMADC bit is changed from “0” to “1”, the initialization cycle (1059/fs=22ms @48kHz, ADRST1-0 bits = “00”) starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power down (default)
1: Power up

LOSEL: Monaural Line Output Select
0: Speaker Output (SPP/SPN pins) (default)
1: Monaural Line Output (AOUT pin)

PMBP: BEEP Input Select and Power Management
0: Power down (IN- pin) (default)
1: Power up (BEEP pin)

PMVCM: VCOM and Regulator (2.3V) Power Management
0: Power down (default)
1: Power up

PMPFIL: Programmable Filter Block Power Management
0: Power down (default)
1: Power up

The AK4637 can be powered down by writing “0” to the address “00H” and PMPLL, PMMP, PMSL and PMDM bits. In this case, register values are maintained.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	0	0	M/S	PMPLL	PMSL	0
R/W		R	R	R	R	R/W	R/W	R/W	R
Default		0	0	0	0	0	0	0	0

PMSL: Speaker Amplifier or Monaural Line Output Power Management
0: Power down (default)
1: Power up

PMPLL: PLL Power Management
0: EXT Mode and Power down (default)
1: PLL Mode and Power up

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SLPSN	MGAIN3	DACS	0	PMMP	MGAIN2	MGAIN1	MGAIN0
R/W		R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

MGAIN3-0: Microphone Amplifier Gain Control (Table 22)
Default: “0110” (+18dB)

PMMP: MPWR pin Power Management
0: Power down: Hi-Z (default)
1: Power up

DACS: Signal Switch Control from DAC to Speaker Amplifier
0: OFF (default)
1: ON

SLPSN: Speaker Amplifier or Monaural Line Output Power-Save Mode
LOSEL bit = “0” (Speaker Output Select)
0: Power Save Mode (default)
1: Normal Operation
When SLPSN bit is “0”, Speaker Amplifier is in power-save mode. In this mode, the SPP pin goes to Hi-Z and the SPN pin outputs AVDD/2 voltage. When PMSL bit = “1”, SLPSN bit is enabled. After the PDN pin is set to “L”, Speaker Amplifier is in power-down mode since PMSL bit is “0”.

LOSEL bit = “1” (Monaural Line Output Select)
0: Power Save Mode (default)
1: Normal Operation
When SLPSN bit is “0”, Monaural line output is in power-save mode. In this mode, the AOUT pin output 1.5V or 1.3V. When PMSL bit = “1”, SLPSN bit is enabled. After the PDN pin is set to “L”, Monaural line output is in power-down mode since PMSL bit is “0”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	SPKG1	SPKG0	0	MICL	0	0	0	MDIF
R/W		R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MDIF: ADC Input Source Select (Table 21)
0: AIN pin Single-ended Input (default)
1: IN+/– pins Full-differential Input

MICL: MPWR pin Output Voltage Select
0: typ 2.4V (default)
1: typ 2.0V

SPKG1-0: Speaker Amplifier Output Gain Select (Table 47)
Default: “00” (+6.4dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Signal Select 3	LVCM1	LVCM0	DACL	0	0	0	0	0
R/W		R/W	R/W	R/W	R	R	R	R	R
Default		0	1	0	0	0	0	0	0

DACL: Signal Switch Control from DAC to Monaural Line Amplifier
0: OFF (default)
1: ON

LVCM1-0: Monaural Line Output Gain and Common Voltage Setting (Table 50)
Default: “01” (+2dB, 1.5V)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	0	CKOFF	BCKO1	BCKO0
R/W		R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Default		0	1	0	1	0	0	0	0

BCKO: BICK Output Frequency Setting in Master Mode (Table 9, Table 17)
00: 16fs (default)
01: 32fs
10: 64fs
11: N/A

CKOFF: FCK, BICK, SDTO Output Stop Setting in Master Mode
0: FCK, BICK, SDTO Output (default)
1: FCK, BICK, SDTO Output Stop

PLL3-0: PLL Reference Clock Select (Table 5)
Default: “0101” (MCKI, 12.288MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mode Control 2	CM1	CM0	0	0	FS3	FS2	FS1	FS0
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	1	1

FS3-0: Sampling frequency Setting (Table 7, Table 10, Table 12, Table 15)
Default: "1011" (fs=48kHz)

CM1-0: MCKI Input Frequency Setting in EXT mode (Table 11, Table 14)
Default: "00" (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Mode Control 3	TSDSEL	THDET	SMUTE	0	MSBS	BCKP	DIF1	DIF0
R/W		R/W	R	R/W	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF2-0: Audio Interface Format (Table 19)
Default: "10" (MSB justified)

BCKP: BICK Polarity at DSP Mode (Table 20)
"0": SDTO is output by the rising edge ("↑") of BICK and SDTI is latched by the falling edge ("↓"). (default)
"1": SDTO is output by the falling edge ("↓") of BICK and SDTI is latched by the rising edge ("↑").

MSBS: FCK Phase at DSP Mode (Table 20)
"0": The rising edge ("↑") of FCK is half clock of BICK before the channel change. (default)
"1": The rising edge ("↑") of FCK is one clock of BICK before the channel change.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

THDET: Thermal Shutdown Detection Result
0: Normal Operation (default)
1: During Thermal Shutdown

TSDSEL: Thermal Shutdown Mode Select
0: Automatic Power up (default)
1: Manual Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Digital MIC	0	0	0	PMDM	DCLKE	0	DCLKP	DMIC
R/W		R	R	R	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

DMIC: Digital Microphone Connection Select
0: Analog Microphone (default)
1: Digital Microphone

DCLKP: Data Latching Edge Select
0: Data is latched on the DMCLK rising edge (“↑”). (default)
1: Data is latched on the DMCLK falling edge (“↓”).

DCLKE: DMCLK pin Output Clock Control
0: “L” Output (default)
1: 64fs Output

PMDM: Input Signal Select with Digital Microphone
0: OFF (default)
1: ON
ADC digital block is powered-down by PMDM bit = “0” when selecting a digital microphone input (DMIC bit = “1”).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Timer Select	ADRST1	ADRST0	FRATT	FRN	0	0	0	DVTM
R/W		R/W	R/W	R/W	R/W	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

DVTM: Output Digital Volume Soft Transition Time Setting (Table 44)
0: 816/fs (default)
1: 204/fs
This is the transition time between DVOL7-0 bits = 00H and CCH.

FRN: ALC Fast Recovery Function Enable
0: Enable (default)
1: Disable

RFATT: Fast Recovery Reference Volume Attenuation Amount (Table 35)
0: -0.00106dB (4/fs) (default)
1: -0.00106dB (16/fs)

ADRST1-0: ADC Initialization Cycle Setting (Table 18)
Default: “00” (1059/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Timer Select	0	IVTM	EQFC1	EQFC0	WTM1	WTM0	RFST1	RFST0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	0	0	0	0	0

RFST1-0: ALC First Recovery Speed (Table 34)
Default: “00” (0.0032dB)

WTM1-0: ALC Recovery Waiting Period (Table 31)
Default: “00” (128/fs)

EQFC1-0: ALCEQ Frequency Setting (Table 28)
Default: “10” (Extreme value=150Hz, Zero point=100Hz @ fs = 48kHz)

IVTM: Input Digital Volume Soft Transition Time Setting (Table 40)
0: 236/fs
1: 944/fs (default)
A transition time when changing IVOL7-0 bits to F1H from 05H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 1	ALCEQN	LMTH2	ALC	RGAIN2	RGAIN1	RGAIN0	LMTH1	LMTH0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH2-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 29)
Default: “000”

RGAIN2-0: ALC Recovery Gain Step (Table 32)
Default: “000” (0.00424dB)

ALC: ALC Enable
0: ALC Disable (default)
1: ALC Enable

ALCEQN: ALC EQ Enable
0: ALC EQ On (default)
1: ALC EQ Off

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 33)
Default: “E1H” (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Input Volume Control	IVOL7	IVOL6	IVOL5	IVOL4	IVOL3	IVOL2	IVOL1	IVOL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVOL7-0: Digital Input Volume; 0.375dB step, 242 Level (Table 39)
Default: “E1H” (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
R/W		R	R	R	R	R	R	R	R
Default		-	-	-	-	-	-	-	-

VOL7-0: Current ALC volume value; 0.375dB step, 242 Level. Read operation only. (Table 36)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Beep Control	0	BPVCM	BEEPS	0	BPLVL3	BPLVL2	BPLVL1	BPLVL0
R/W		R	R/W	R/W	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPLVL3-0:BEEP Output Level Setting (Table 45)
Default: “0000” (0dB)

BEEPS: Signal Switch Control from the BEEP pin to Speaker Amplifier
0: OFF (default)
1: ON

BPVCM: Common Voltage Setting of BEEP Input Amplifier (Table 46)
0: 1.15V (default)
1: 1.65V

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

DVOL7-0: Digital Output Volume (Table 43)
Default: “18H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	EQ Common Gain Select	0	0	0	EQC5	EQC4	EQC3	EQC2	0
R/W		R	R	R	R/W	R/W	R/W	R/W	R
Default		0	0	0	0	0	0	0	0

EQC2: Equalizer 2 Common Gain Selector
0: Disable (default)
1: Enable
When EQC2 bit = "1", the common gain setting (EQ2G) is reflected.

EQC3: Equalizer 3 Common Gain Selector
0: Disable (default)
1: Enable
When EQC3 bit = "1", the common gain setting (EQ3G) is reflected.

EQC4: Equalizer 4 Common Gain Selector
0: Disable (default)
1: Enable
When EQC4 bit = "1", the common gain setting (EQ4G) is reflected.

EQC5: Equalizer 5 Common Gain Selector
0: Disable (default)
1: Enable
When EQC5 bit = "1", the common gain setting (EQ5G) is reflected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	EQ2 Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
13H	EQ3 Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
14H	EQ4 Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
15H	EQ5 Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ2T1-0, EQ3T1-0, EQ4T1-0, EQ5T1-0: Transition Time of EQ2~EQ5 Gain (Table 27)
Default: "00H" (256/fs)

EQ2G5-0, EQ3G5-0, EQ4G5-0, EQ5G5-0: Gain setting of EQ2~EQ5 (Table 26)
Default: "00H" (Mute)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Digital Filter Select 1	0	0	0	0	0	HPFC1	HPFC0	HPFAD
R/W		R	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

HPFAD: HPF1 Control after ADC
0: OFF
1: ON (default)
When HPFAD bit is “1”, the settings of HPFC1-0 bits are enabled. When HPFAD bit is “0”, the audio data passes the HPFAD block by 0dB gain.
When PMADC bit = “1”, set HPFAD bit to “1”.

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) (Table 25)
Default: “00” (3.7Hz @ fs = 48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	Digital Filter Select 2	0	0	0	0	0	0	LPF	HPF
R/W		R	R	R	R	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

HPF: HPF2 Coefficient Setting Enable
0: OFF (default)
1: ON
When HPF bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is “0”, the audio data passes the HPF2 block by is 0dB gain.

LPF: LPF Coefficient Setting Enable
0: OFF (default)
1: ON
When LPF bit is “1”, the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is “0”, the audio data passes the LPF block by 0dB gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	Digital Filter Mode	0	0	PFVOL1	PFVOL0	PFDAC1	PFDAC0	ADCPF	PFSDO
R/W		R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

PFSDO: SDTO Output Signal Select
0: ADC (+ 1st order HPF) Output
1: Programmable Filter / ALC Output (default)

ADCPF: Programmable Filter / ALC Input Signal Select
0: SDTI
1: ADC Output (default)

PFDAC1-0: DAC Input Signal Select (Table 42)
Default: 00 (SDTI)

PFVOL1-0: Sidetone Digital Volume (Table 41)
Default: 00 (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1AH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1BH	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1CH	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		F1A13-0 bits = 0x1FB0, F1B13-0 bits = 0x209F							

F1A13-0, F1B13-0: HPF2 Coefficient (14bit x 2)
Default: F1A13-0 bits = 0x1FB0, F1B13-0 bits = 0x209F (fc = 150Hz@fs=48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
1EH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
1FH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
20H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: LPF Coefficient (14bit x 2)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
21H	Digital Filter Select 3	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is “1”, the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is “0”, the audio data passes the EQ1 block by 0dB gain.

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is “1”, the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is “0”, the audio data passes the EQ2 block by 0dB gain.

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is “1”, the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is “0”, the audio data passes the EQ3 block by 0dB gain.

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is “1”, the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is “0”, the audio data passes the EQ4 block by 0dB gain.

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is “1”, the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is “0”, the audio data passes the EQ5 block by 0dB gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
23H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
24H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
25H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
26H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
27H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
28H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
29H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
2AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
2BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
2CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
2DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
2EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
2FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
30H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
31H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
32H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
33H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
34H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
35H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
36H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
37H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
38H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
39H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
3AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
3BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
3CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
3DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
3EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
3FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

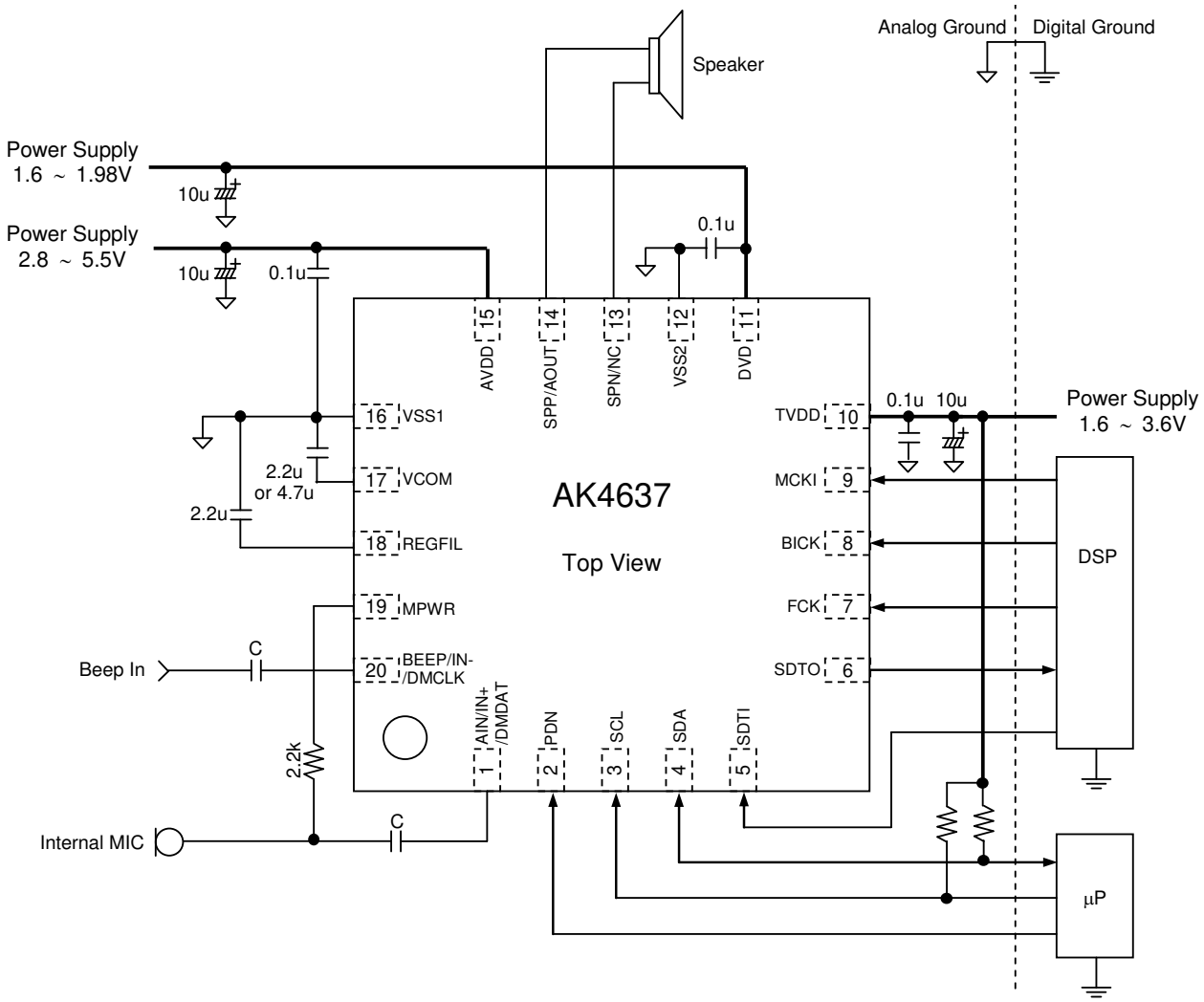
E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

10. Recommended External Circuits

Figure 65 shows the system connection diagram. An evaluation board (AKD4637) is available for fast evaluation as well as suggestions for peripheral circuitry.



Notes:

- VSS1 and VSS2 of the AK4637 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- When the AK4637 is used in master mode, FCK pin is floating before M/S bit is changed to “1”. Therefore, a pull-up or pull-down resistor around 100kΩ must be connected to FCK pin of the AK4637.
- The pull-up resistors of the SCL and SDA pins must be connected to a voltage in the range from TVDD or more to 6V or less.
- 0.1µF capacitors at power supply pins. Other capacitors do not have specific types.

Figure 65. System Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4637 requires careful attention to power supply and grounding arrangements. AVDD is usually supplied from the system's analog supply, and DVDD and TVDD are supplied from the system's digital power supply. If AVDD, DVDD and TVDD are supplied separately, the power-up sequence is not critical. The PDN pin should be held "L" when power supplies are tuning on. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

To avoid pop noise on line output when power up/down, the AK4637 should be operated along the following recommended power-up/down sequence.

1) Power-up
   - The PDN pin should be held "L" when power supplies are turning on. The AK4637 can be reset by keeping the PDN pin "L" for 200ns or longer after all power supplies are applied and settled.
2) Power-down
   - Each of power supplies can be powered OFF after the PDN pin is set to "L".

VSS1 and VSS2 of the AK4637 should be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

2. Internal Regulated Voltage Power Supply

REGFIL is a power supply of the analog circuit (typ. 2.3V). A 2.2μF ±10% capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK4637. No load current may be drawn from the REGFIL pin. All digital signals, especially clocks, should be kept away from the REGFIL pin in order to avoid unwanted coupling into the AK4637.

3. Reference Voltage

VCOM is a signal ground of this chip. A 2.2μF ±10%(AVDD ≤ 3.6V) or 4.7μF±10%(AVDD > 3.6V) capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK4637. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4637. Attention must be paid to the printing pattern and the material of the capacitors to prevent superimposed noises and voltage drops since the VCOM voltage is the reference of many functions.

4. Analog Inputs

The microphone and line inputs support single-ended or full-differential format. When single-ended input, the input signal range scales with nominally at typ. 2.07Vpp (@ MGAIN = 0dB), centered around the internal signal ground (typ. 1.15V). Usually the input signal is AC coupled with a capacitor. The cut-off frequency is $fc = 1/(2\pi RC)$.

5. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit data). The speaker amplifier (SPP and SPN pins) is BTL output, and they should be connected directly to a speaker. There is no need for AC coupling capacitors. The monaural line output (AOUT pin) is single-ended and centered on 1.5V (LVCM0 bit = "1": default). This pin must be AC-coupled using a capacitor.

11. Control Sequence

■ Clock Set Up

When ADC, DAC or Programmable Filter is powered-up, the clocks must be supplied. Turn off the power management bits first when switching the master clock. The power management bits should be turned on after the master clock is stabilized.

1. PLL Master Mode

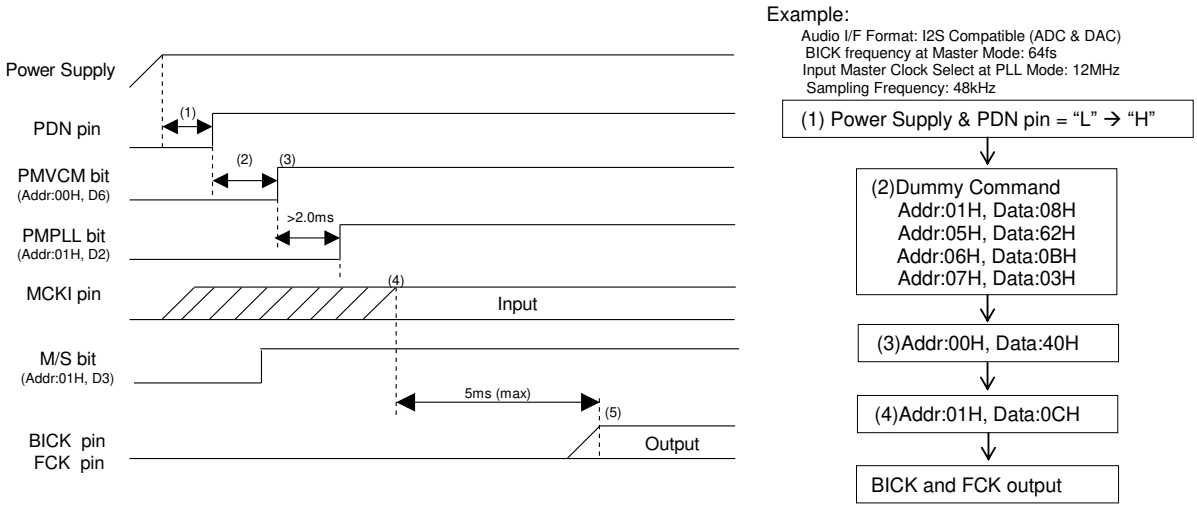


Figure 66. Clock Set Up Sequence (1)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4637.

(2) After Dummy Command (Addr:00H, Data:00H) input, M/S, PLL3-0, BCKO1-0, FS3-0, MSBS, BCKP and DIF1-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM is 2.2μF (AVDD ≤ 3.6V), 4.7μF(AVDD > 3.6V) and the REGFIL pin is 2.2μF.

(4) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source, and PLL lock time is 5ms (max)

(5) The AK4637 starts to output the BICK and FCK clocks after the PLL became stable. Then normal operation starts.

2. PLL Slave Mode (BICK pin)

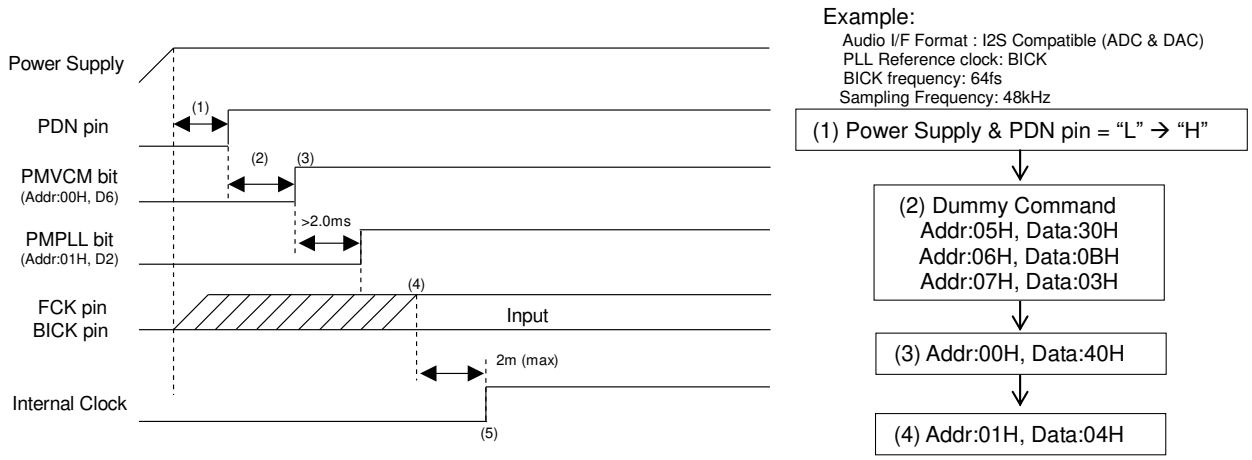


Figure 67. Clock Set Up Sequence (2)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4637.

(2) After Dummy Command (Addr:00H, Data:00H) input, DIF1-0, PLL3-0, and FS3-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM is 2.2μF (AVDD ≤ 3.6V), 4.7μF(AVDD > 3.6V) and the REGFIL pin is 2.2μF.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied. PLL lock time is 2ms (max) when BICK is a PLL reference clock.

(5) Normal operation starts after that the PLL is locked.

3. EXT Slave Mode

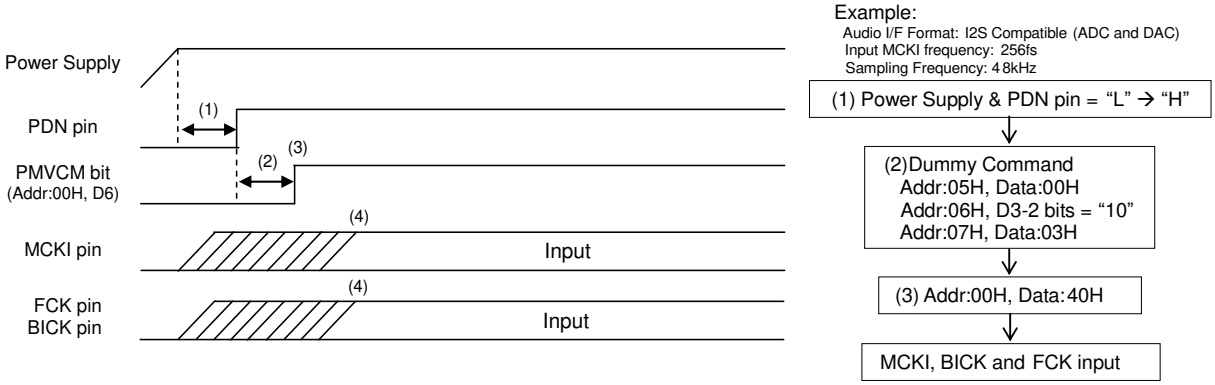


Figure 68. Clock Set Up Sequence (3)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4637.

(2) After Dummy Command (Addr:00H, Data:00H) input, CM1-0, FS3-2, MSBS,BCKP and DIF1-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM is 2.2μF (AVDD ≤ 3.6V), 4.7μF(AVDD > 3.6V) and the REGFIL pin is 2.2μF.

(4) Normal operation starts after the MCKI, FCK and BICK are supplied.

4. EXT Master Mode

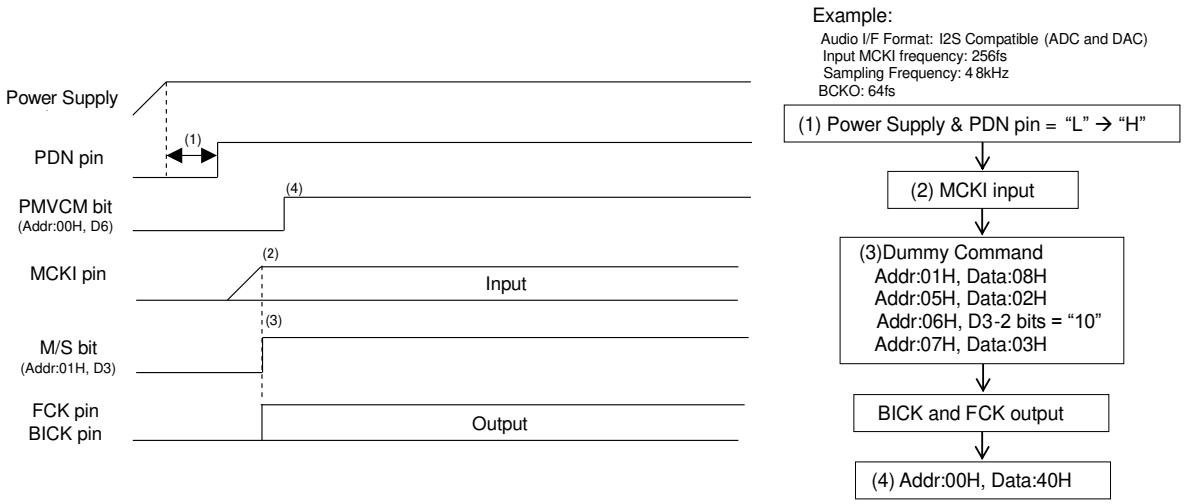


Figure 69. Clock Set Up Sequence (4)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4637.

(2) MCKI is supplied.

(3) After Dummy Command (Addr:00H, Data:00H) input, BCKO1-0, CM1-0, FS3-2, MSBS,BCKP and DIF1-0 bits are set. M/S bit should be set to "1". Then FCK and BICK are output.

(4) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when both capacitances of an external capacitor for the VCOM is 2.2μF (AVDD ≤ 3.6V), 4.7μF(AVDD > 3.6V) and REGFIL pins are 2.2μF.

■ Microphone Input Recording

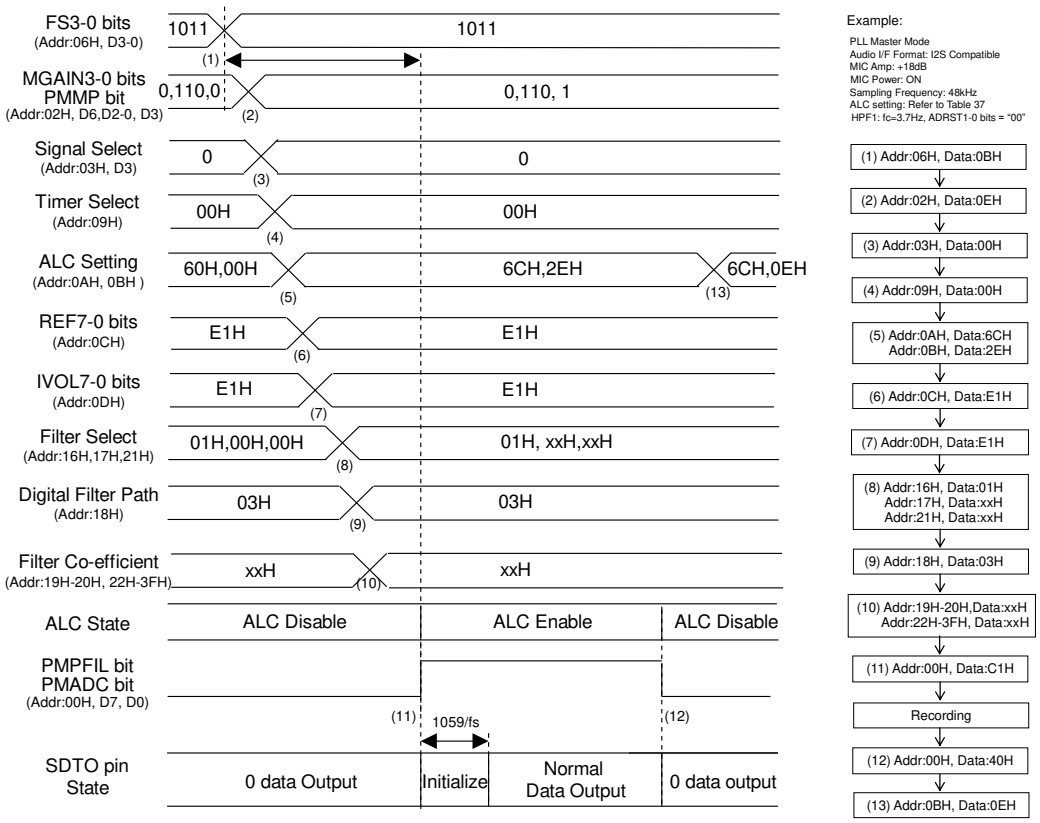


Figure 70. Microphone Input Recording Sequence

<Sequence>

This sequence is an example of ALC setting at fs= 48kHz. For changing the parameter of ALC, please refer to Table 37. At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4637 is in PLL mode, Microphone, ADC and Programmable Filter of (12) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up Microphone Amp and Microphone Power. (Addr = 02H)
(3) Set up Input Signal. (Addr = 03H)
(4) Set up FRN, FRATT and ADRST1-0 bits (Addr = 09H)
(5) Set up ALC mode. (Addr = 0AH, 0BH)
(6) Set up REF value at ALC (Addtr = 0CH)
(7) Set up IVOL value at ALC operation start (Addr = 0DH)
(8) Programmable Filter ON/OFF Setting (Addr: 16H, 17H, 21H)
(9) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 18H)
(10) Set up Coefficient Programmable Filter (Addr: 19H ~ 20H, 22H ~ 3FH)
(11) Power Up Microphone Amp, ADC and Programmable Filter: PMADC =PMPFIL bits = "0" → "1"
The initialization cycle time of ADC is 1059/fs=22ms @ fs=48kHz, ADRST1-0 bit = "00". ADC outputs "0" data during the initialization cycle. After the ALC bit is set to "1", the ALC operation starts from IVOL value of (7).
(12) Power Down Microphone Amp, ADC and Programmable Filter: PMADC = PMPFIL bits = "1" → "0"
(13) ALC Disable: ALC bit = "1" → "0"

■ Digital Microphone Input

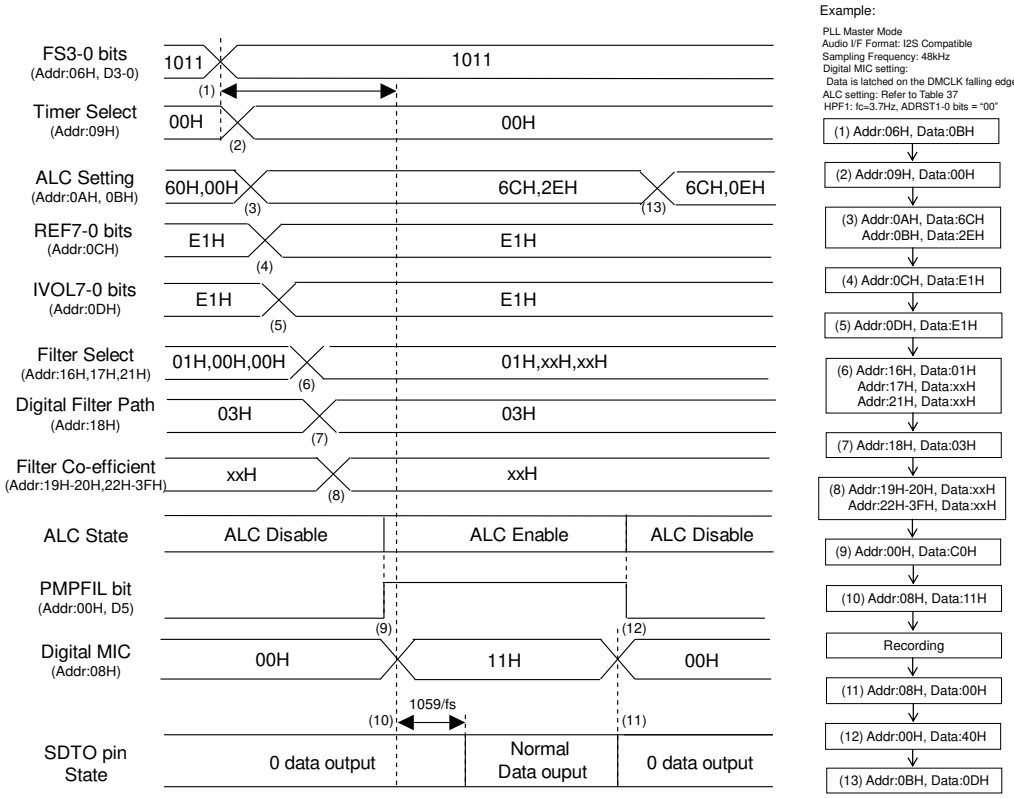


Figure 71. Digital Microphone Input Recording Sequence

<Sequence>

This sequence is an example of ALC setting at fs=48kHz. For changing the parameter of ALC, please refer to Table 37. At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4637 is PLL mode, Digital Microphone of (11) and Programmable Filter of (10) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up FRN, FRATT and ADRST1-0 bits (Addr = 09H)
(3) Set up ALC mode. (Addr = 0AH, 0BH)
(4) Set up REF value for ALC (Addtr = 0CH)
(5) Set up IVOL value at ALC operation start (Addr = 0DH)
(6) Set up Programmable Filter ON/OFF (Addr = 16H, 17H, 21H)
(7) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 18H)
(8) Set up Coefficient of Programmable Filter (Addr:19H ~ 20H, 22H ~ 3FH)
(9) Power Up Programmable Filter: PMPFIL bit = "0" → "1"
(10) Set Up & Power Up Digital Microphone: DMIC = PMDM bits = "0" → "1"
The initialization cycle time of ADC is 1059/fs=22ms@ fs=48kHz, ADRST1-0 bit = "00". ADC outputs "0" data during initialization cycle. After the ALC bit is set to "1", the ALC operation starts from IVOL value of (5).
(11) Power Down Digital Microphone: PMDM bit = "1" → "0"
(12) Power Down Programmable Filter: PMPFIL bit = "1" → "0"
(13) ALC Disable: ALC bit = "1" → "0"

■ Speaker Amplifier Output

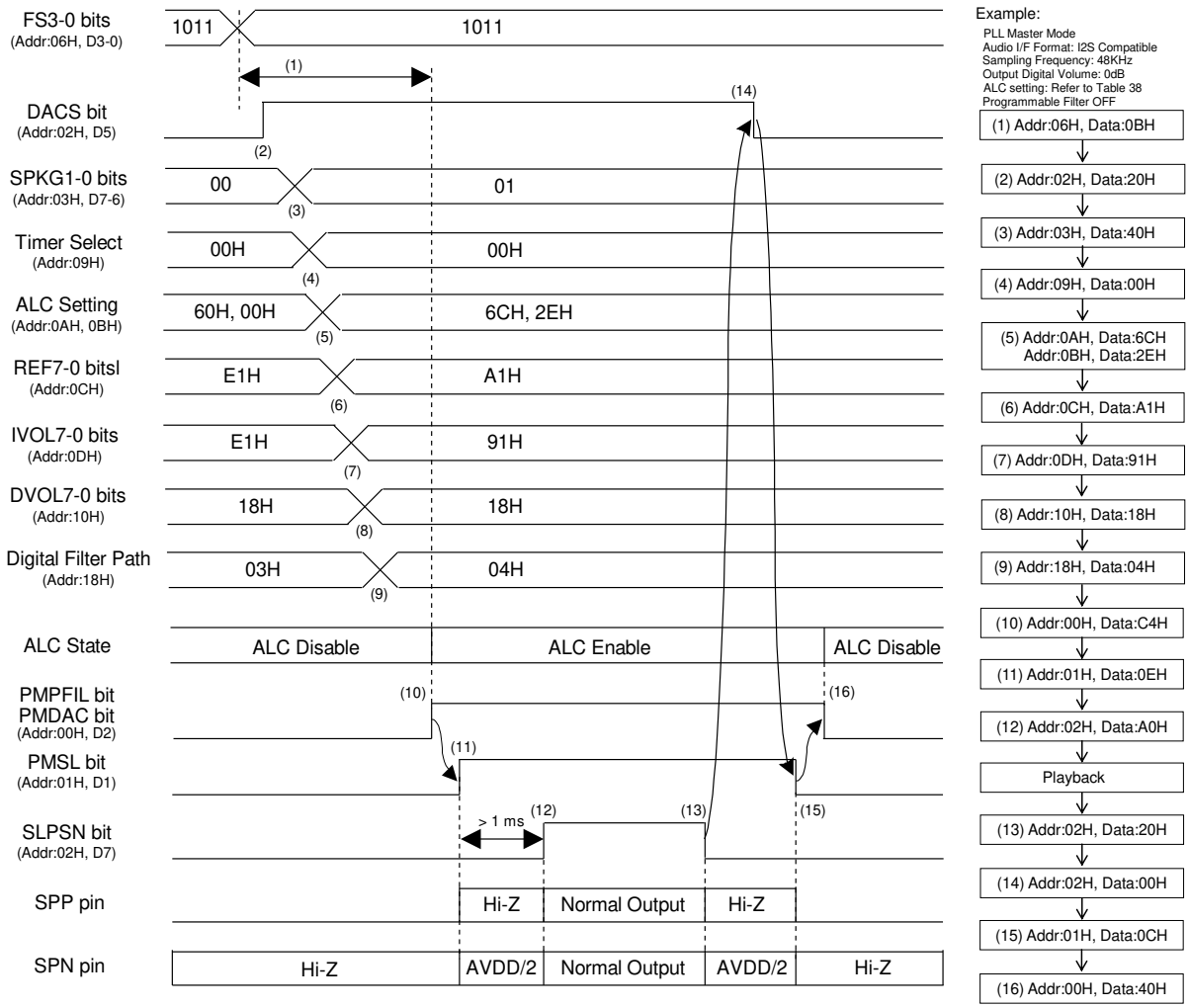


Figure 72. Speaker-Amp Output Sequence

<Sequence>

At first, clocks must be supplied according to “Clock Set Up” sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4637 is in PLL mode, DAC, Programmable Filter and Speaker-Amp of (10) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up the path of DAC → SPK-Amp: DACS bit = “0” → “1” (Addr = 02H)
(3) SPK-Amp gain setting: SPKG1-0 bits = “00” → “01” (Addr = 03H)
(4) Set up FRN, FRATT and ADRST1-0 bits (Addr = 09H)
(5) Set up ALC mode (Addr = 0AH, 0BH)
(6) Set up REF value of ALC (Addr = 0CH)
(7) Set up IVOL value of ALC operation start (Addr = 0DH)
(8) Set up the output digital volume. (Addr = 10H)
(9) Set up Programmable Filter Path: PFDAC1-0 bits=“01”, PFSDO=ADCPF bits=“0” (Addr = 18H)
(10) Power up DAC and Programmable Filter: PMDAC=PMPFIL bits=“0”→“1” (Addr = 00H)
(11) Power up Speaker-Amp: PMSL bit=“0”→“1” (Addr = 01H)
(12) Exit the power-save mode of Speaker-Amp: SLPSN bit = “0” → “1” (Addr = 02H)
(13) Enter Speaker-Amp Power Save Mode: SLPSN bit = “1” → “0” (Addr = 02H)
(14) Disable the path of DAC → SPK-Amp: DACS bit = “1” → “0” (Addr = 02H)
(15) Power down Speaker-Amp: PMSL bit= “1”→“0” (Addr =01H)
(16) Power down DAC and Programmable Filter: PMDAC=PMPFIL bits= “1”→“0” (Addr = 00H)

■ Beep Signal Output from Speaker Amplifier

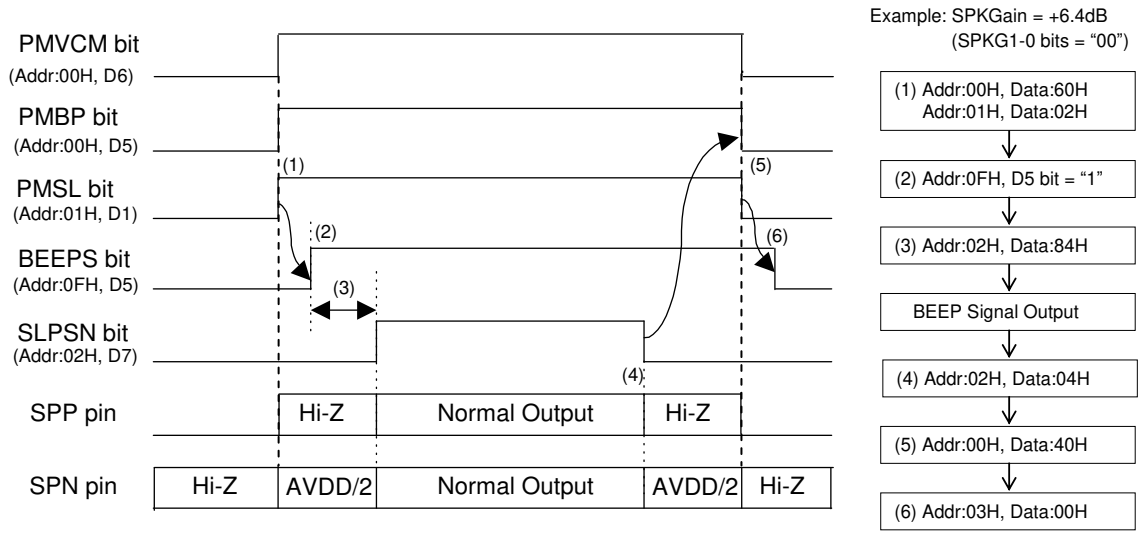


Figure 73. "BEEP-Amp → Speaker-Amp" Output Sequence

<Sequence>

Clock input is not necessary when the AK4637 is operating only on the path of "BEEP-Amp" → "SPK-Amp".

(1) Power up VCOM, MIN-Amp and Speaker: PMVCM = PMBP = PMSL bits = "0" → "1"
(2) Set up the path of BEEP → SPK-Amp: BEEPS bit = "0" → "1"
(3) Exit the power save mode of Speaker-Amp: SLPSN bit = "0" → "1"
Period (3) should be set according to the time constant of a capacitor and a resistor that are connected to the BEEP pin. Pop noise may occur if the SPK-Amp output is enabled before the BEEP-Amp input is stabilized. The BEEP Amp is powered up after VCOM voltage rise. The maximum rise-up time of VCOM is 2msec.
(4) Enter Speaker-Amp Power-save mode: SLPSN bit = "1" → "0"
(5) Power Down BEEP-Amp and Speaker: PMBP = PMSL bits = "1" → "0"
(6) Disable the path of BEEP → SPK-Amp: BEEPS bit = "1" → "0"

■ Lineout Output

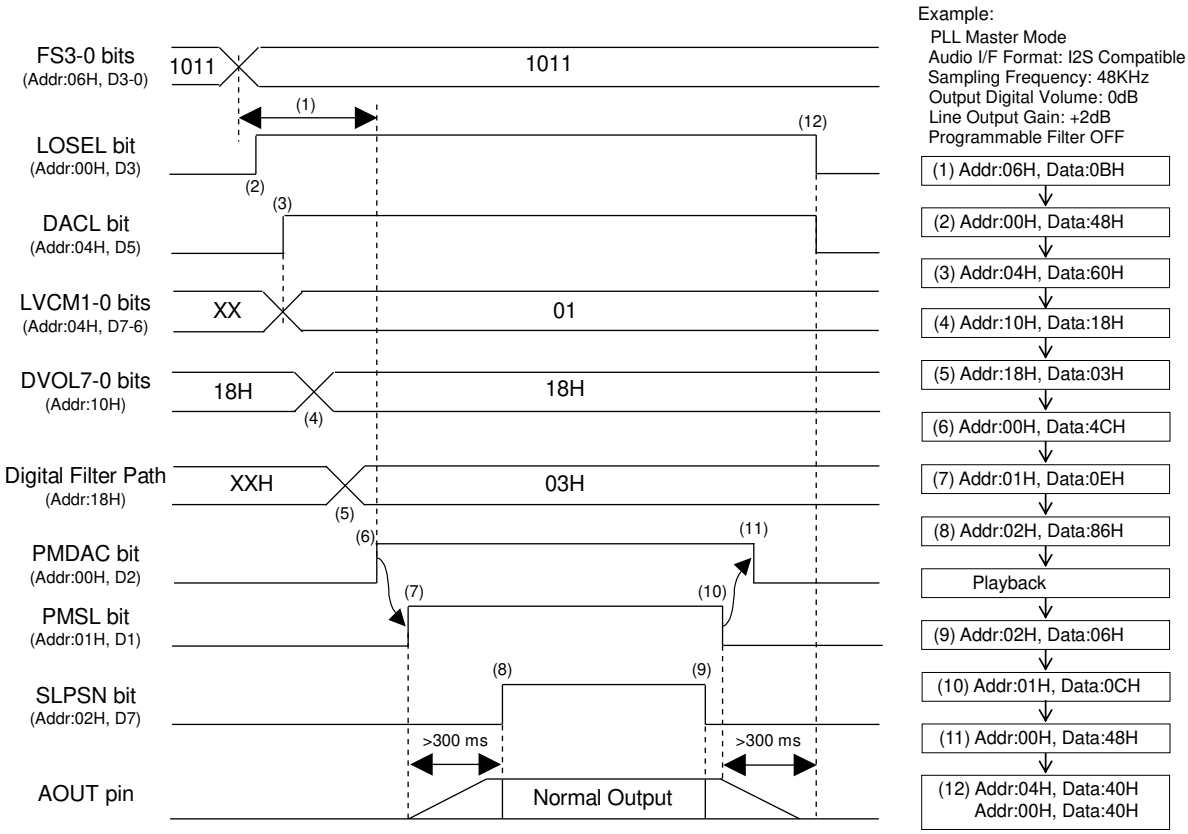


Figure 74. Lineout Sequence

<Sequence>

At first, clocks must be supplied according to “Clock Set Up” sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4637 is in PLL mode, DAC and Lineout Output of (6) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Enter Lineout Output Mode: LOSEL bit = “0” → “1” (Addr = 00H)

(3) Set up the path of DAC → Lineout, and Lineout gain setting:
DACL bit = “0” → “1”, LVCM1-0 bits = “xx” → “01” (Addr = 04H)

(4) Set up the output digital volume. (Addr = 10H)

(5) Set up Programmable Filter Path: PFDAC1-0 bit=“00”, PFSDO=ADCPF bits = “1” (Addr = 18H)

(6) Power up DAC: PMDAC bit = “0” → “1” (Addr = 00H)

(7) Power up Lineout Output: PMSL bit = “0” → “1” (Addr =01H)
The AOUT pin starts rising after PMSL bit = “1”. The maximum rise-up time to 99% VCOM voltage is 300ms when C = 1μF and R_L=10kΩ.

(8) Exit the power-save mode of Lineout Output: SLPSN bit = “0” → “1” (Addr = 04H)
SLPSN bit should be set after the AOUT pin is risen up. The AOUT pin starts to output sound data after SLPSN bit = “0” → “1”.

(9) Enter Lineout Output Power Save Mode: SLPSN bit = “1” → “0” (Addr = 04H)

(10) Power down Lineout Output: PMSL bit = “1” → “0” (Addr = 01H)

(11) Power down DAC: PMDAC bit = “1” → “0” (Addr = 00H)
The AOUT pin is powered down after PMSL bit = “0”. The maximum power down time to 1% VCOM voltage is 300ms.

(12) Exit the path of DAC → Lineout: DACL bit = “1” → “0” (Addr = 04H)
Exit Lineout Output Mode: LOSEL bit = “1” → “0” (Addr = 00H)
DACL and LOSEL bits should be set after the AOUT pin is powered down.

■ Stop of Clock

When ADC, DAC or Programmable Filter is powered-up, the clocks must be supplied.

1. PLL Master Mode

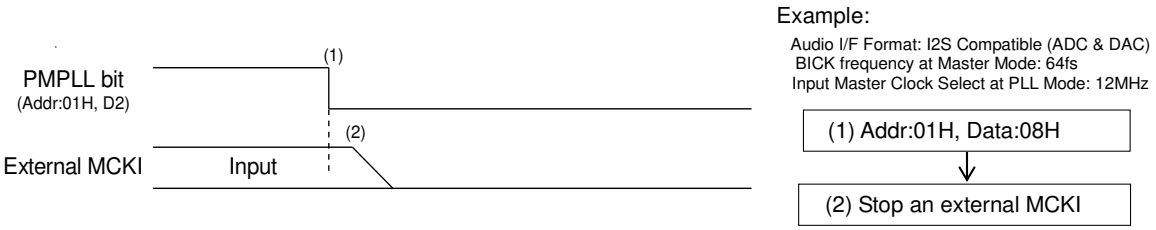


Figure 75. Clock Stopping Sequence (1)

<Sequence>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop an external master clock.

2. PLL Slave Mode (BICK pin)

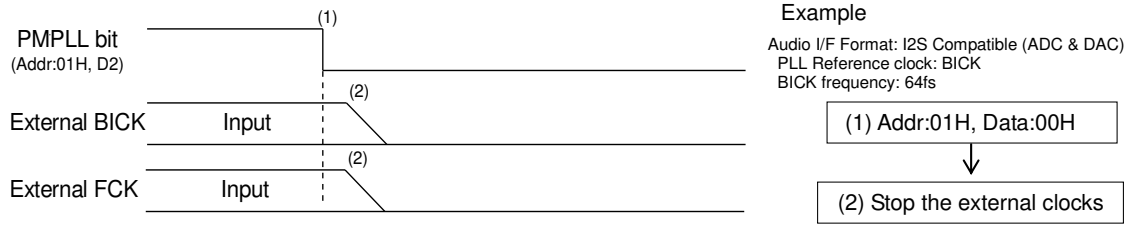


Figure 76. Clock Stopping Sequence (2)

<Sequence>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop an external master clock.

3. EXT Slave Mode

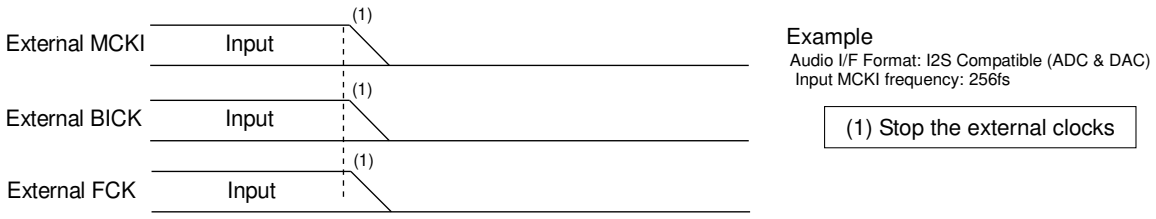


Figure 77. Clock Stopping Sequence (3)

<Sequence>
(1) Stop the external MCKI, BICK and FCK clocks.

4. EXT Master Mode

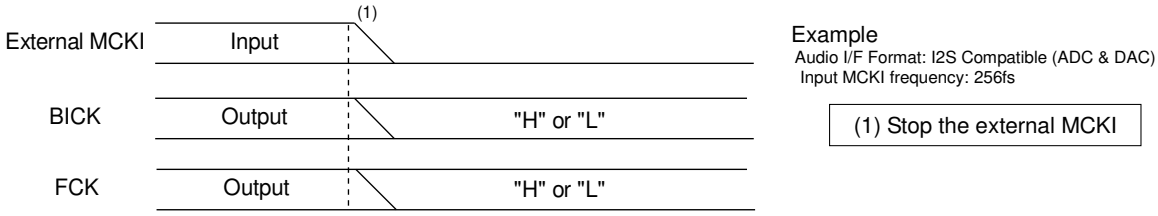


Figure 78. Clock Stopping Sequence (4)

<Sequence>
(1) Stop an external master clock. BICK and FCK are fixed to “H” or “L”.

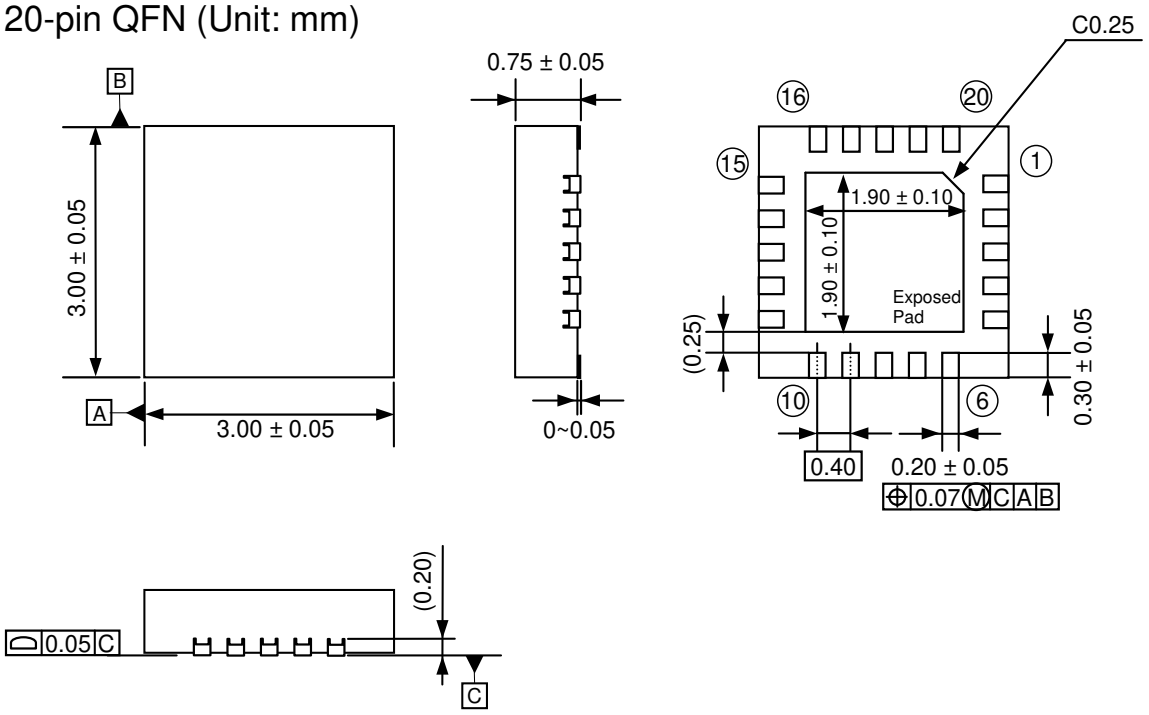
■ Power Down

Power supply current cannot be shut down by stopping clocks and setting PMVCM bit = “0”. Power supply current can be shut down (typ. 1μA) by stopping clocks and setting the PDN pin = “L”. When the PDN pin = “L”, all registers are initialized.

12. Package

■ Outline Dimensions

20-pin QFN (Unit: mm)

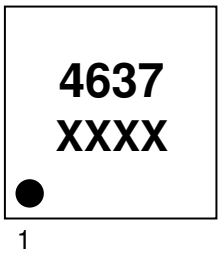


Note. The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material & Lead finish

Package molding compound: Epoxy Resin, Halogen (Br and Cl) free
Lead frame material: Cu Alloy
Pin surface treatment: Solder (Pb free) plate

■ Marking



XXXX: Date code (4 digit)
Pin #1 indication

13. Ordering Guide

AK4637EN	−40 ~ +85°C	20-pin QFN (0.4mm pitch)
AKD4637EN	Evaluation board for AK4637EN	

14. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
15/09/30	00	First Edition		

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