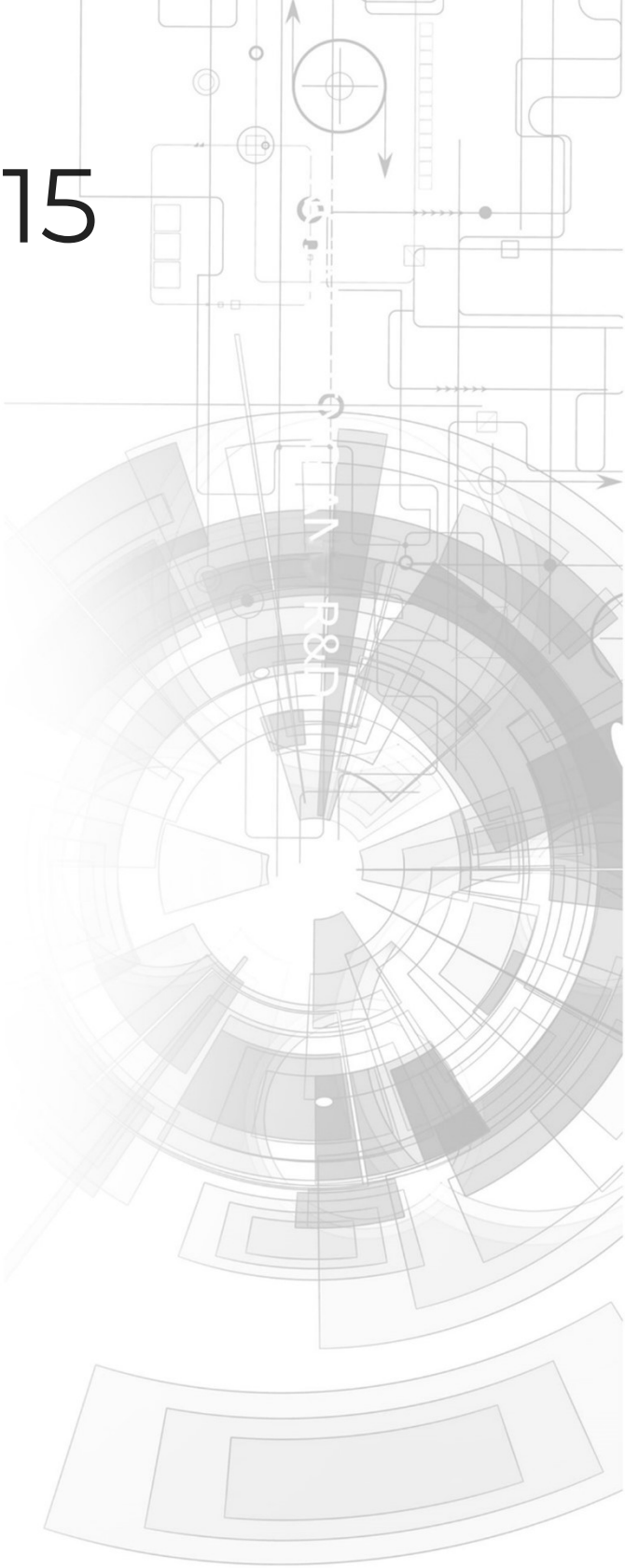
4DOLED-282815



Datasheet

Revision 1.1

Contents

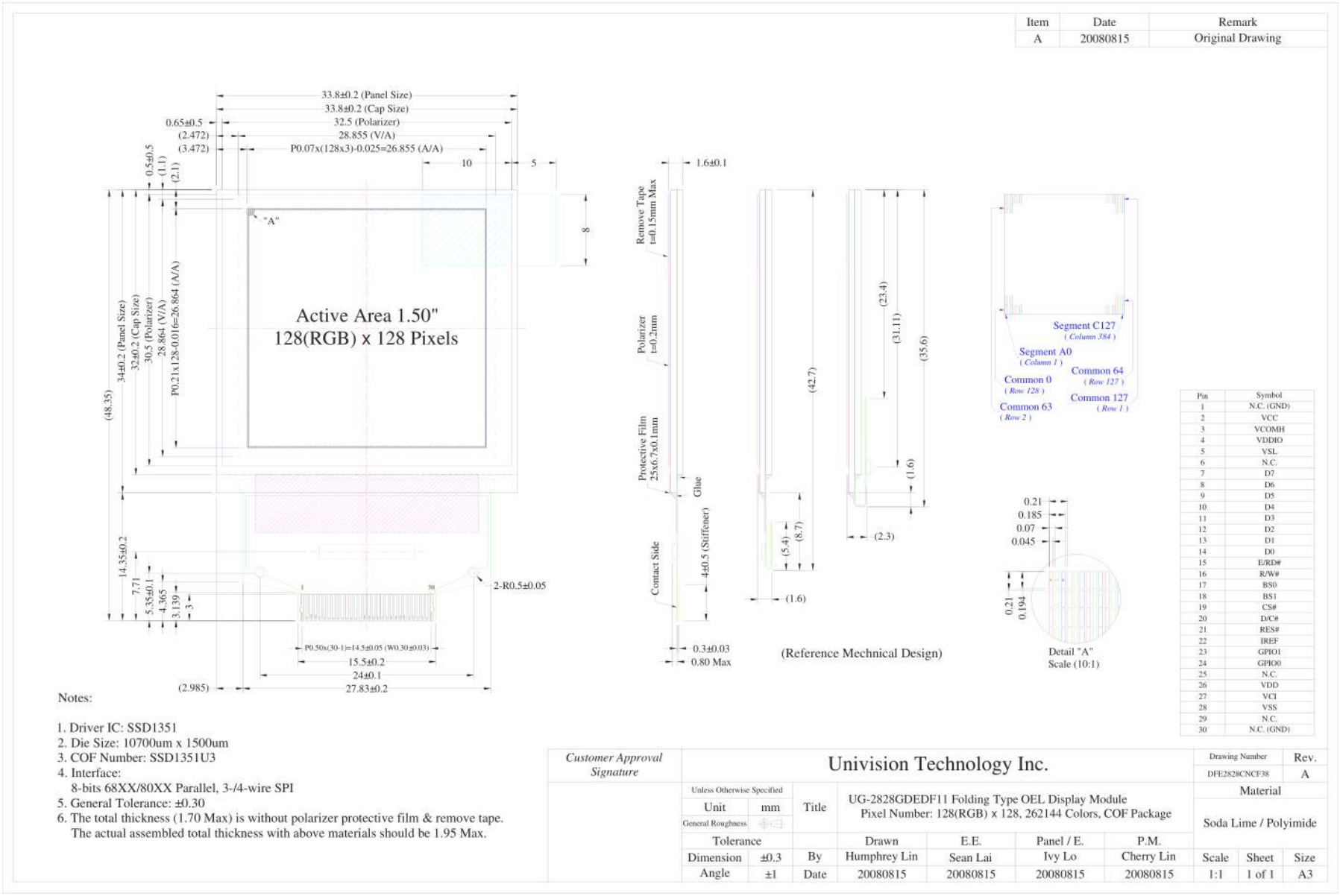
1. General Specification

The 4DOLED-282815 is a 1.5" 128x128 pixel resolution 262K colour Passive Matrix OLED display. This OLED is the same display used in the micro-OLED range of modules. It allows a very cost-effective means of adding a full-colour small display to any product or your next microcontroller project.

Specifications

ITEM	CONTENTS	UNIT
Display Mode	Passive Matrix	
Size	1.5	Inch
Color Depth	262K	
Drive Duty	1/128	Duty
Display Size	33.80 x 34.00 x 1.60	mm
Active Area (W × H)	26.855 x 26.864	mm
Dot Pitch (W × H)	0.07 x 0.21	mm
Number of Dots (Pixels)	128 (RGB) × 128	
Pixel Size	0.045 x 0.194	mm
Weight	3.75	g

1.1. Mechanical Details



1.2. Pin Definition

Power Supply

Pin Number	Symbol	I/O	Function
27	VCI	P	**Power Supply for Operation** This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDDIO.
26	VDD	P	**Power Supply for Core Logic Circuit** This is a voltage supply pin which is regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
4	VDDIO	P	**Power Supply for I/O Pin** This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals) pull high, they should be connected to VDDIO.
28	VSS	P	**Ground of Logic Circuit** This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
2	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be connected to external source.

Driver

Pin Number	Symbol	I/O	Function
22	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5µA maximum.
3	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
5	VSL	I	**Voltage Output Low Level for SEG Signal** This is segment voltage reference pin. External VSL is set as default. This pin has to connect with resistor and diode to ground.

External IC Control

Pin Number	Symbol	I/O	Function
24 23	GPIO0 GPIO1	I/O	**General Purpose Input/Output** This pin could be left open individually or has signal inputted/outputted. It is able to use as the external DC/DC converter circuit enabled/disabled control or other applications.

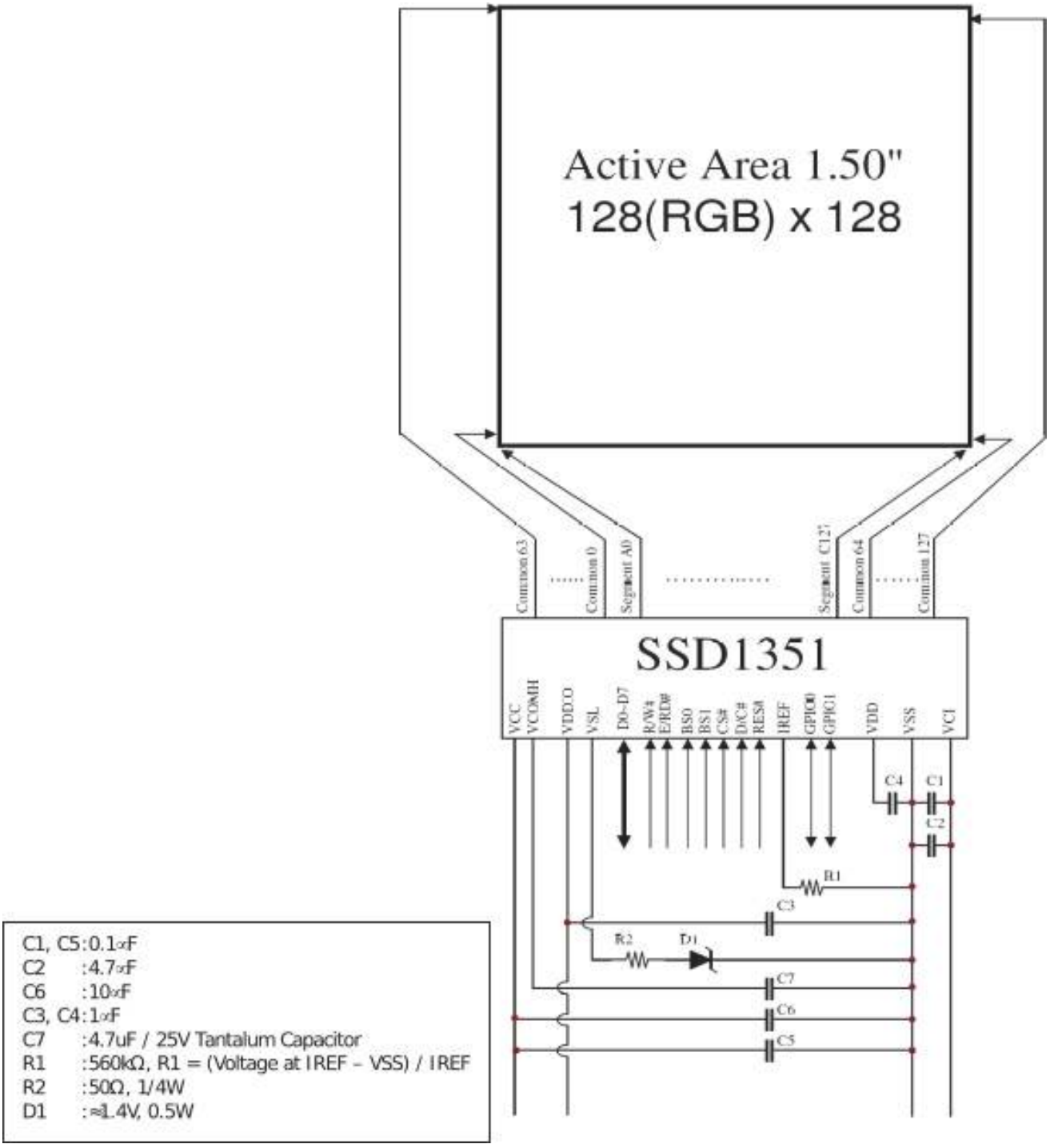
Interface

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>17
18</td><td>BS0
BS1</td><td>O</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:<table><tr><td></td><td>BS0</td><td>BS1</td></tr><tr><td>3-wire SPI</td><td>1</td><td>0</td></tr><tr><td>4-wire SPI</td><td>0</td><td>0</td></tr><tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr><tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr></table></td></tr>
<tr><td>21</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>20</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. When 3-wire serial mode is selected, this pin must be connected to VSS. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams under the AC Characteristics section.</td></tr>
<tr><td>15</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>16</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>7~14</td><td>D7~D0#</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.</td></tr>
</table>

Reserve

Pin Number	Symbol	I/O	Function
1, 35	N.C. (GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.
6, 25, 29	N.C.	-	**Reserved Pin** Reserved Pin The N.C. pins between function pins are reserved for compatible and flexible design.

1.3. Block Diagram



MCU Interface Selection: Based on BS0 and BS1 connection, as shown below in the table.
Pins connected to MCU interface : D7~D0, E/RD#, R/W#, CS#, D/C#, and RES#

EIM=1(default)

BS0	BS1	Interface mode	Data Bus								Control Bus				
			D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E/RD#	RES#
0	0	4-wire SPI	0	0	0	0	0	NC	SDIN	SCLK	CS#	D/C#	0	0	RES#
0	1	3-wire SPI	0	0	0	0	0	NC	SDIN	SCLK	CS#	0	0	0	RES#
1	0	8bit 8080	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	WR#	RD#	RES#
1	1	8bit 6800	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	R	RES#

Note

- "0" is connected to VSS.
- "1" is connected to VDD.
- "NC" is not connected.

2. Absolute Maximum Ratings

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage for Operation	VCI	-0.3	4	V	1, 2
Supply Voltage for Logic	VDD	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	VDDIO	-0.5	VCI	V	1, 2
Supply Voltage for Display	VCC	-0.5	16	V	1, 2
Operating Temperature	TOP	-40	70	°C	3
Storage Temperature	TSG	-40	85	°C	3
Life Time (90 cd/m2)		10,000	-	hour	4
Life Time (70 cd/m2)		15,000	-	hour	4
Life Time (50 cd/m2)		20,000	-	hour	4

Note

1. All the above voltages are based on "VSS = 0V".
2. When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to the Optics & Electrical Characteristics section. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.
3. The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.
4. VCC = 13.0V, Ta = 25°C, 50% Checkerboard.
   Software configuration follows the Actual Application Example section initialization.
   End of a lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high-temperature conditions.

3. Optics & Electrical Characteristics

3.1. Optics Characteristics

The optical measurement was taken at VCI = 2.8V, and VCC = 13.0V. Software configuration follows the Actual Application Example section initialization.

Optical Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness	Lbr	Note 5	70	90	-	cd/m2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E. (Red)	(x) (y)	C.I.E. 1931	0.60 0.30	0.64 0.34	0.68 0.38	
C.I.E. (Green)	(x) (y)	C.I.E. 1931	0.27 0.58	0.31 0.62	0.35 0.66	
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.10 0.12	0.14 0.16	0.18 0.20	
Dark Room Contrast	CR		-	> 10,000:1	-	
Viewing Angle			-	Free	-	degree

3.2. DC Characteristics

DC Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Operation	VCI		2.4	2.8	3.5	V
Supply Voltage for Operation	VDD		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	VDDIO		1.65	1.8	VCI	V
Supply Voltage for Display	VCC	Note 5	12.5	13.0	13.5	V
High Level Input	VIH		0.8 x VDDIO	-	VDDIO	V
Low Level Input	VIL		0	-	0.2 X VDDIO	V
High Level Output	VOH1	Iout =100µA, 3.3MHz	0.9 x VDDIO	-	VDDIO	V
Low Level Output	VOL1	Iout =100µA, 3.3MHz	0	-	0.1 x VDDIO	V
Operating Current for VCC	ICI		-	240	300	µA
Operating Current for VCC	ICC	Note 6	-	13.3	17.0	mA
		Note 7	-	23.2	29.0	mA
		Note 8	-	33.4	42.0	mA
Sleep Mode Current for VCI	ICI, SLEEP		-	2	10	µA
Sleep Mode Current for VCC	ICC, SLEEP		-	2	10	µA

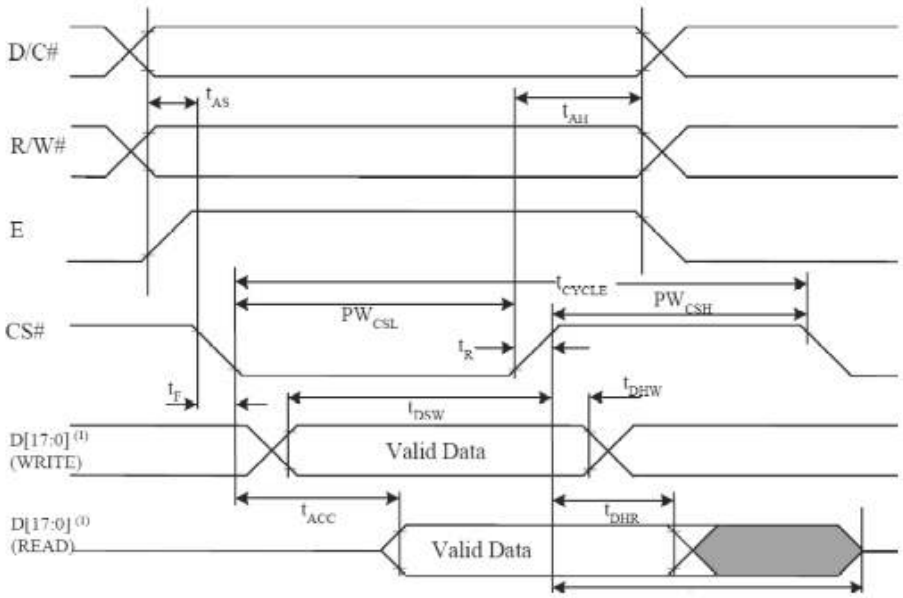
Note

1. Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to change in the panel characteristics and the customer's request.
2. VCI = 2.8V, VCC = 13.0V, 30% Display Area Turn on.
3. VCI = 2.8V, VCC = 13.0V, 50% Display Area Turn on.
4. VCI = 2.8V, VCC = 13.0V, 100% Display Area Turn on.

Software configuration follows the Actual Application Example section initialization.

3.3. AC Characteristics

3.3.1. 68XX-Series MPU Parallel Interface Timing Characteristics

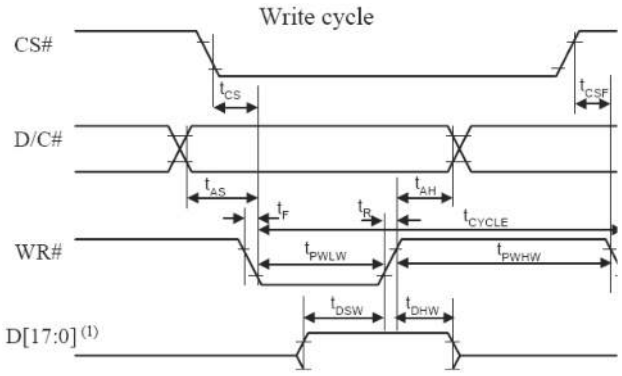


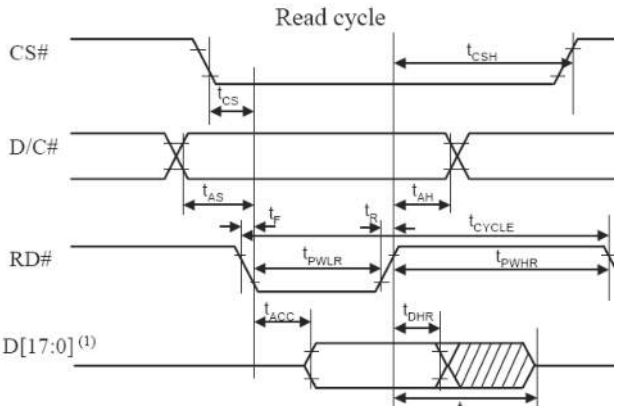
- When 8-bit Used: D[7:0] Instead

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	300	-	ns
tAS	Address Setup Time	10	-	ns
tAH	Address Hold Time	0	-	ns
tDSW	Write Data Setup Time	40	-	ns
tDHW	Write Data Hold Time	7		
tDHR	Read Data Hold Time	20	-	ns
tOH	Output Disable Time	-	70	ns
tACC	Access Time	-	140	ns
PWCSL	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PWCSH	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
tF	Rise Time	-	15	ns
tR	Fall Time	-	15	ns

(VCI - VSS = 2.4V to 3.5V, VDDIO - VSS = 1.65V to VCI, Ta = 25°C)

3.3.2. 80XX-Series MPU Parallel Interface Timing Characteristics



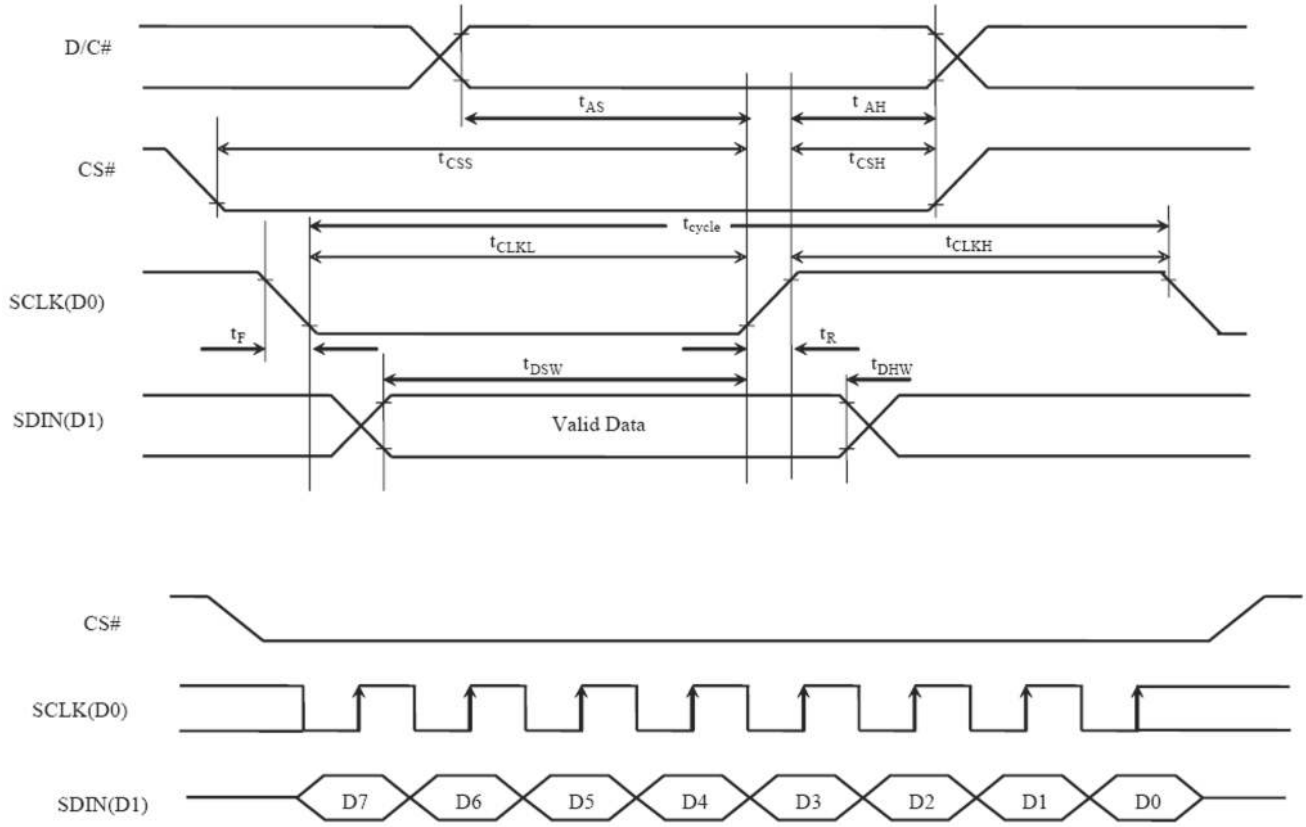


80XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description		Min	Max	Unit	Port
tAH8	Address Setup Timing		5	-	ns	CSB RS
tAS8	Address Hold Timing		5	-	ns	
tCYC8	System Cycle Timing	(Read)	200	-	ns	RDB
tRDLR6	Read "L" Pulse Width		90	-	ns	
tRDHR6	Read "H" Pulse Width		90	-	ns	
tCYC8	System Cycle Timing	(Write)	100	-	ns	
tWRLW8	Write "L" Pulse Width		45	-	ns	
tWRHW8	Write "H" Pulse Width		45	-	ns	
tRDD8	Read Data Output Delay Time	* CL = 15pF	-	60	ns	D[17:9]
tRDH8	Data Hold Timing		0	60	ns	
tDS8	Write Data Setup Timing		30	-	ns	
tDH8	Write Data Hold Timing		10	-	ns	

(VCI - VSS = 2.4V to 3.5V, VDDIO - VSS = 1.65V to VCI, Ta = 25°C)

3.3.3. 4-Wire SPI Timing Characteristics

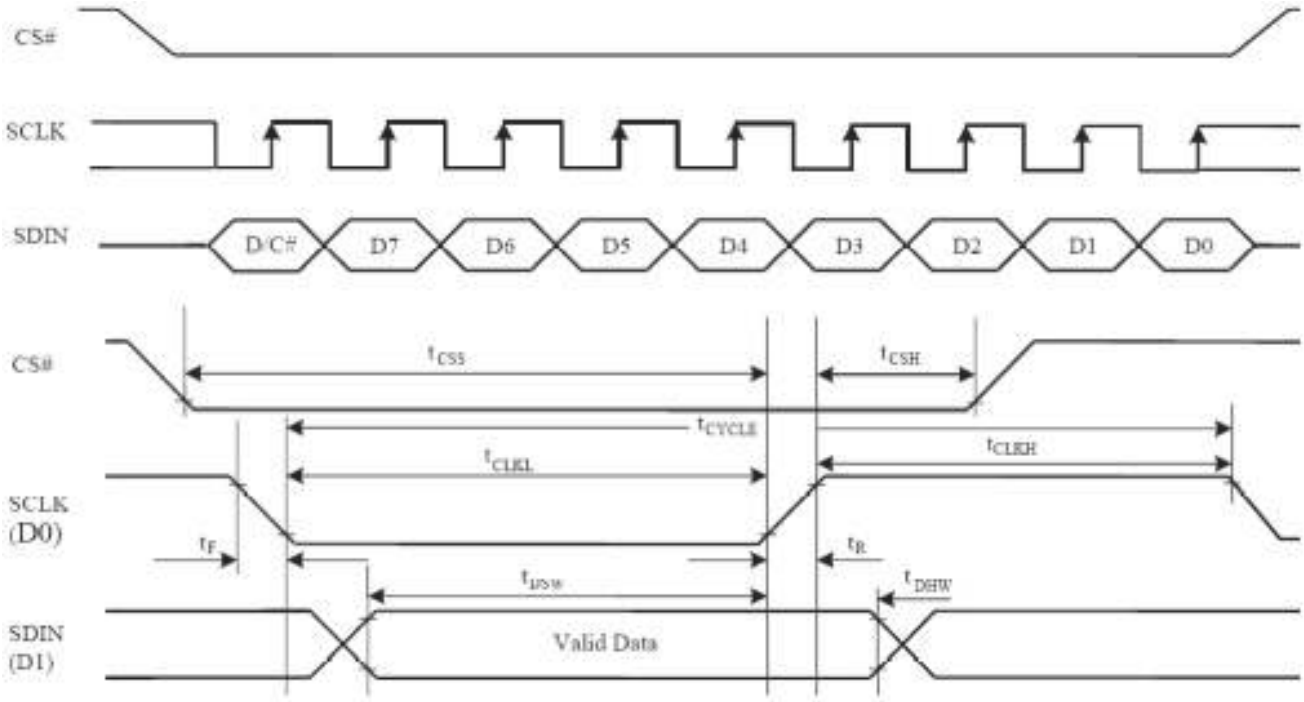


4-Wire SPI Timing Characteristics

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	50	-	ns
tAS	Address Setup Time	15	-	ns
tAH	Address Hold Time	15	-	ns
tCSS	Chip Select Setup Time	20	-	ns
tCSH	Chip Select Hold Time	10	-	ns
tDSW	Write Data Setup Time	15	-	ns
tDHW	Write Data Hold Time	15	-	ns
tCLKL	Clock Low Time	20	-	ns
tCLKH	Clock High Time	20	-	ns
tR	Rise Time	-	15	ns
tF	Fall Time	-	15	ns

(VCI - VSS = 2.4V to 3.5V, VDDIO - VSS = 1.65V to VCI, Ta = 25°C)

3.3.4. 3-Wire SPI Timing Characteristics



3-Wire SPI Timing Characteristics

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	50	-	ns
tCSS	Chip Select Setup Time	20	-	ns
tCSH	Chip Select Hold Time	10	-	ns
tDSW	Write Data Setup Time	15	-	ns
tDHW	Write Data Hold Time	15	-	ns
tCLKL	Clock Low Time	20	-	ns
tCLKH	Clock High Time	20	-	ns
tR	Rise Time	-	15	ns
tF	Fall Time	-	15	ns

(VCI - VSS = 2.4V to 3.5V, VDDIO - VSS = 1.65V to VCI, Ta = 25°C).

4. Initialisation Codes

SET_COLUMN_ADDRESS	0x15	
SET_ROW_ADDRESS	0x75	
WRITE_GRAM	0x5C	
READ_GRAM	0x5D	
STOP_MOVING	0x9E	
START_MOVING	0x9F	
REMAP_COLOUR_SETTINGS	0xAO	
DISPLAY_START_LINE	0xA1	
DISPLAY_OFFSET	0xA2	
DISPLAY_OFF	0xA4	Entire Display Off, All Pixels Turn Off
DISPLAY_ALL_ON	0xA5	Entire Display On, All Pixels Turn On at GS Level 63
DISPLAY_NORMAL	0xA6	Normal Display
DISPLAY_INVERSE	0xA7	Inverse Display
FUNCTION_SELECTION	0xAB	
DISPLAY_NOP	0xAD	
DISPLAY_SLEEP_OFF	0xAE	
DISPLAY_SLEEP_ON	0xAF	
DISPLAY_NOP2	0xB0	
PHASE_PRECHARGE	0xB1	
DISPLAY_ENHANCE	0xB2	
CLOCK_FREQUENCY	0xB3	
SEGMENT_LOW_VOLTAGE	0xB4	
SET_GPIO	0xB5	
SECOND_PRECHARGE	0xB6	
SET_GRAYSCALE_LUT	0xB8	
RESET_GRAYSCALE_LUT	0xB9	
PRECHARGE_VOLTAGE_RGB	0xBB	
SET_VCOMH	0xBE	
CONTRAST_RGB	0xC1	
CONTRAST_MASTER	0xC7	
DUTY_CYCLE	0xCA	same (set mux ration)
OLED_NOP2	0xD1	
OLED_NOP3	0xE3	
COMMAND_LOCK	0xFD	

Init Code

Format: (Command, Data1, ... DataN)

```
COMMAND_LOCK, 0x12,                     // Unlock Driver IC (0x12/0x16/0xB0/0xB1)
COMMAND_LOCK, 0xB1,                     // Unlock All Commands (0x12/0x16/0xB0/0xB1)
DISPLAY_OFF,                            // Display Off (0x00/0x01)
CLOCK_FREQUENCY, 0xF1,                  // Set Clock as 120 Frames/Sec
DUTY_CYCLE, 0x7F,                       // 1/96 Duty (0x0F~0x7F)
DISPLAY_OFFSET, 0,                      // Shift Mapping RAM Counter (0x00~0x7F)
DISPLAY_START_LINE, 0x00,               // Set Mapping RAM Display Start Line (0x00~0x7F)
REMAP_COLOUR_SETTINGS, 0x74,            // Set Horizontal Address Increment
    // Column Address 0 Mapped to SEG0
    // Color Sequence D[15:0]=[RRRRR:GGGGGG:BBBBB]
    // Scan from COM127 to COM0
    // Enable COM Split Odd Even
    // 65536 Colors Mode (0x74)
    // * 262,144 Colors Mode (0xB4)
SET_GPIO, 0x00,                         // Set Low Voltage Level of SEG Pin
FUNCTION_SELECTION,
0x01,               // Enable Internal VDD Regulator, Select 8-bit Parallel Interface
SEGMENT_LOW_VOLTAGE, 0xA0, 0xB5, 0x55,  // Enable External VSL, Set Segment Low Voltage
CONTRAST_RGB, 0xC8, 0x80, 0x8A,         // Set Contrast of Color A (Red)
                                        //                 Color B (Green)
                                        //                 Color C (Blue)
CONTRAST_MASTER, 0x0F,                  // Set Scale Factor of Segment Output Current Control
(0-15)
RESET_GRAYSCALE_LUT,                    // just use internal table for Gray Scale Table
PHASE_PRECHARGE, 0x32,                  // Set Phase 1 as 5 Clocks & Phase 2 as 3 Clocks
PRECHARGE_VOLTAGE_RGB, 0x17,            // Set Pre-Charge Voltage Level as 0.50*VCC
DISPLAY_ENHANCE, 0xA4, 0x00, 0x00,      // UNDOCUMENTED COMMAND Enhance Display Performance
SECOND_PRECHARGE, 0x01,                 // Set Second Pre-Charge Period as 1 Clock
SET_VCOMH, 0x05,                        // Set Common Pins Deselect Voltage Level as 0.82*VCC
DISPLAY_NORMAL,                         // Normal Display Mode (0x02)
DISPLAY_SLEEP_ON,                       // not sleeping
```

5. Functional Specification

5.1. Commands

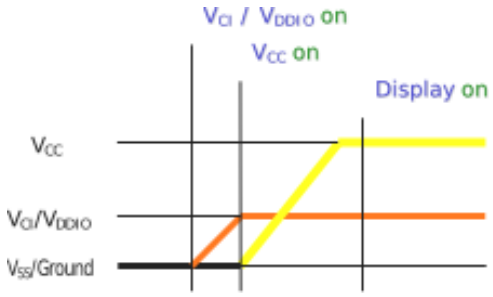
Refer to the Technical Manual for the SSD1351

5.2. Power down and Power up Sequence

To protect the OEL panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

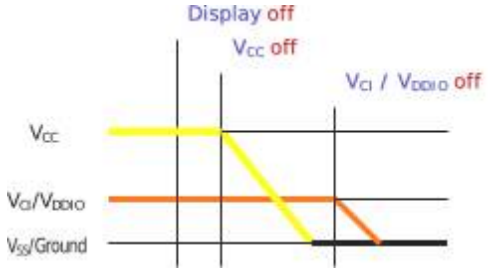
5.2.1. Power up Sequence

1. Power up VCI & VDDIO
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 200ms (When VCC is stable)
7. Send Display on command



5.2.2. Power down Sequence

1. Send Display off command
2. Power down VCC
3. Delay 100ms (When VDDH is reach 0 and the panel is completely discharged)
4. Power down VCI / VDDIO



Note

1. Since an ESD protection circuit is connected between VCI, VDDIO and VCC inside the driver IC, VCC becomes lower than VCI whenever VDD & VDDIO is ON and VCC is OFF.
2. VCC should be kept float (disabled) when it is OFF.
3. Power Pins (VDD, VDDIO, VCC) can never be pulled to the ground under any circumstance.

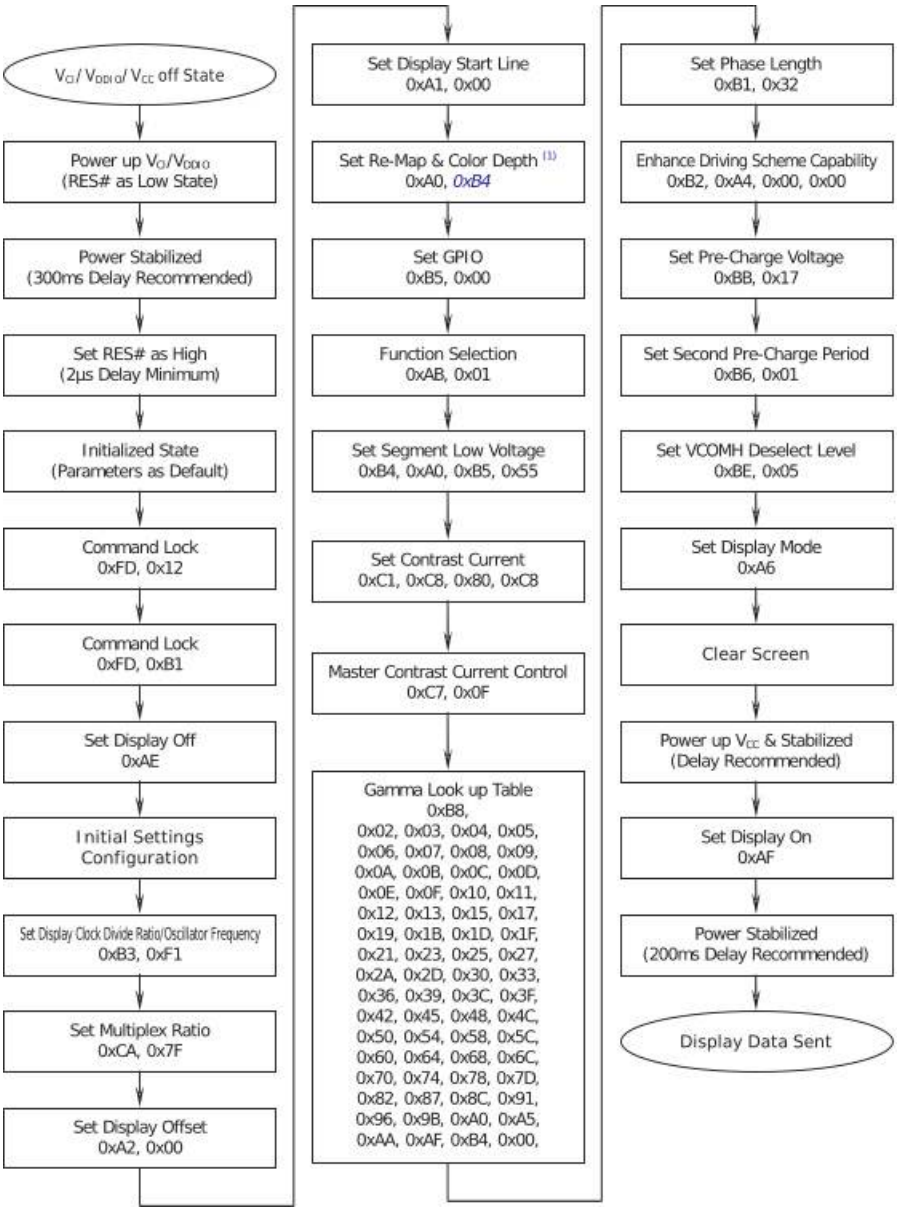
5.3. Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128(RGB) x 128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. The display start line is set at the display RAM address 0
5. The column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Command A2h, B1h, B3h, BBh, BEh are locked by command FDh

5.4. Actual Application Example

Command usage and explanation of an actual example



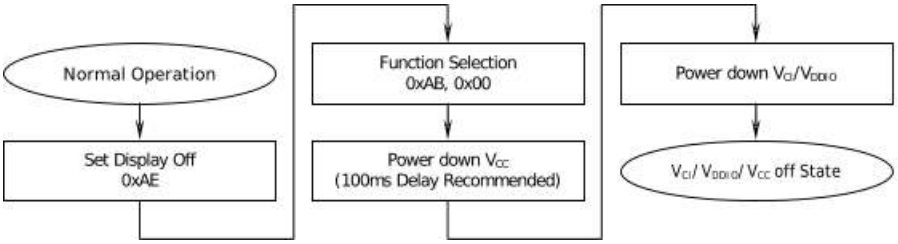
Power up Sequence

Note

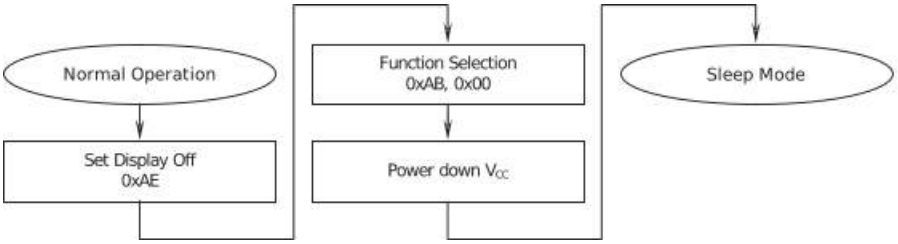
This command could be programmable to fit various applications.

- 0xB4 → 262,144 Colors Mode
- 0x74 → 65,536 Colors Mode
- Others → Please contact us for further information.

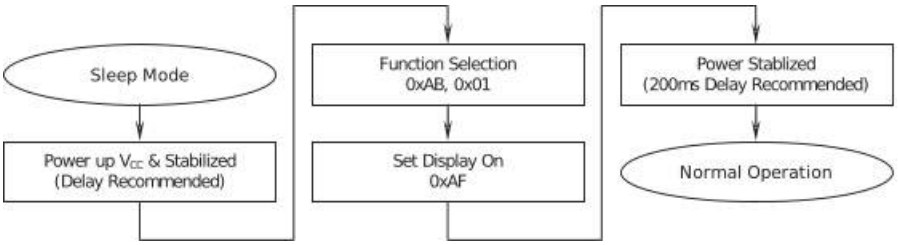
If the noise accidentally occurs at the displaying window during the operation, please reset the display to recover the display function.



Power down Sequence



Entering Sleep Mode



Exiting Sleep Mode

6. Reliability

6.1. Contents of Reliability Tests

Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 240 hrs	
Thermal Shock	-40°C <-> 85°C, 24 cycles 60 mins dwell	

- The samples used for the above tests do not include polarizers
- No moisture condensation is observed during tests.

6.2. Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs before conducting the failure test at 23±5°C; 55±15% RH.

7. Outgoing Quality Control Specifications

Environment Required

The customer's test & measurement are required to be conducted under the following conditions:

Temperature: 23 ± 5°C

Humidity: 55 ± 15% RH

Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥ 50cm

Distance between the Panel & Eyes of the Inspector: ≥ 30cm

A finger glove (or finger cover) must be worn by the inspector.

The inspection table or jig must be anti-electrostatic.

Sampling Plan

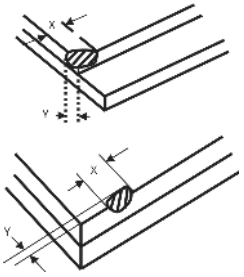
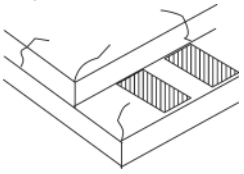
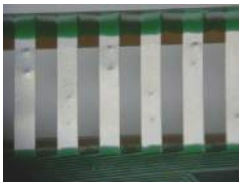
Level II, Normal Inspection, Single Sampling, MIL-STD-105E.

Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

7.1. Cosmetic Check (Display Off) in Non-Active Area

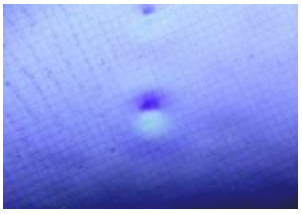
Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

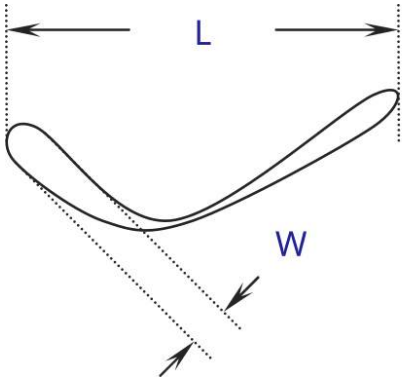
7.2. Cosmetic Check (Display Off) in Active Area

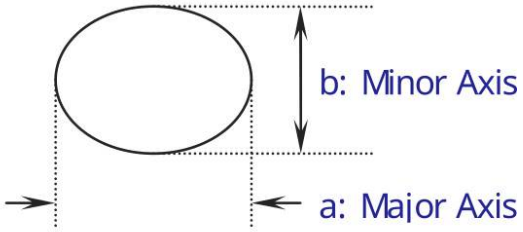
It is recommended to execute in a clean room environment (class 10k) if necessary.

Cosmetic Check (Display Off) in Active Area

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L≤2 n≤1 L>2 n=0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n≤1 0.25 < Φ
n=0		
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 -> Ignore if no Influence on Display 0.5 < Φ n=0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

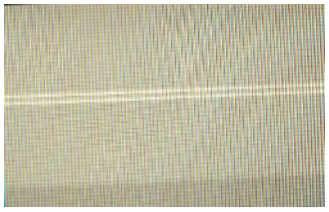
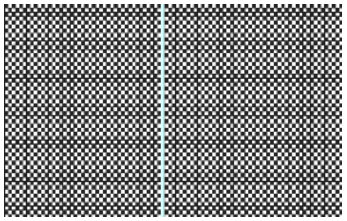
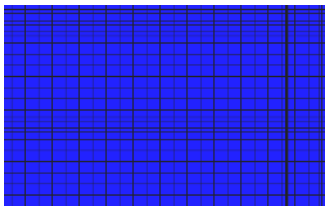
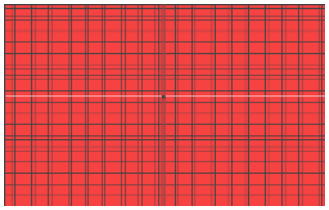
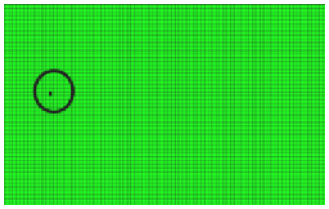
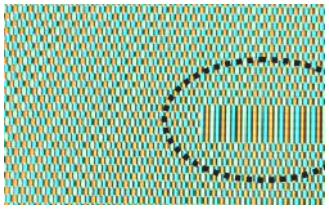
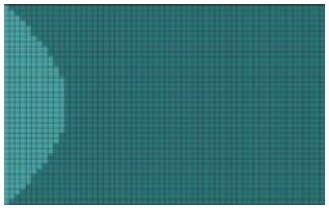
- Protective film should not be torn off when cosmetic check.
- Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2





7.3. Pattern Check (Display On) in Active Area

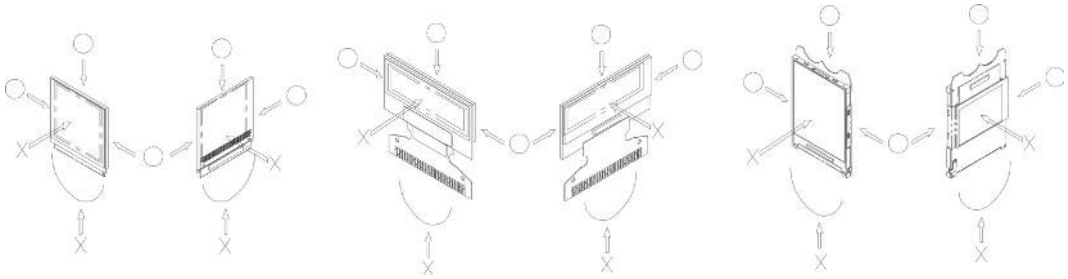
Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	Not Allowable
Bright Line	Major	
Missed Line	Major	 
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major	

8. Precautions When Using These OEL Display Modules

8.1. Handling Precautions

1. Since the display panel is made of glass, do not apply mechanical impacts such as dropping from a high position.
2. If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale or lick the organic substance.
3. If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4. The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5. When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using the following adhesion tape.
6. Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using a cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
7. Water
8. Ketone
9. Aromatic Solvents
10. Hold the OEL display module very carefully when placing the OEL display module into the system housing. Do not apply excessive stress or pressure to the OEL display module. And, do not overbend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



11. Do not apply stress to the driver IC and the surrounding molded sections.
12. Do not disassemble nor modify the OEL display module.
13. Do not apply input signals while the logic power is off.
14. Pay sufficient attention to the working environments when handling OEL display modules to prevent the occurrence of element breakage accidents by static electricity.
    - Be sure to make human body grounding when handling OEL display modules.
    - Be sure to ground tools to use or assemble such as soldering irons.

- To suppress the generation of static electricity, avoid carrying out assembly work under dry environments.
- The protective film is applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

15. The protection film is applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period, the residue adhesive material of the protection film may remain on the surface of the display panel after removing the film. In such cases, remove the residue material by the method introduced in the Reliability section).
16. If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded be careful to avoid the above.

8.2. Storage Precautions

1. When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sunlight nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you store these modules in the packaged state when they were shipped from WiseChip Semiconductor Inc.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2. If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3. Designing Precautions

1. The absolute maximum ratings are the ratings that cannot be exceeded for the OEL display module, and if these values are exceeded, panel damage may happen.
2. To prevent the occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, make the signal line cable as short as possible.
3. We recommend you install an excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4. Pay sufficient attention to avoid the occurrence of mutual noise interference with the neighboring devices.
5. As for EMI, take necessary measures on the equipment side.
6. When fastening the OEL display module, fasten the external plastic housing section.
7. If the power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.

8. The electric potential to be connected to the rear face of the IC chip should be as follows: SEPS525
9. Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4. Precautions when disposing of the OEL display modules

1. Request qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5. Other Precautions

1. When an OEL display module is operated for a length of time a fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, the normal state can be restored. Also, there will be no problem with the reliability of the module.
2. To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
3. Pins and electrodes
4. Pattern layouts such as the FPC
5. With this OEL display module, the OEL driver is exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
6. Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
7. Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
8. Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It, therefore, is necessary to take appropriate measures to suppress noise generation or to protect from the influences of noise on the system design.
9. We recommend you construct its software to make periodical refreshments of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

9. Revision History

Document Revision

REVISION	DATE	COMMENT
1.0	20/09/2018	Initial Version
1.1	20/01/2023	Modified datasheet for web-based documentation