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FDMC035N10X1

N-Channel PowerTrench® MOSFET

100 V, 5.5 A, 37 mΩ

Features

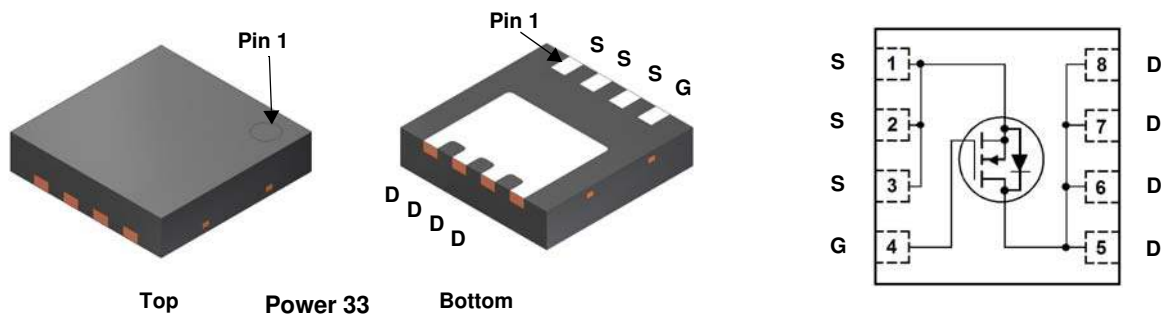
- Max $r_{DS(on)}$ = 37 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$
- Max $r_{DS(on)}$ = 41 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 5.0\text{ A}$
- Low Profile - 0.8 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced PowerTrench® technology. This very high density process is especially tailored to minimize on-state resistance and optimized for hot swap application.

Applications

- DC - DC Conversion
- PSE Switch



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Rating	Units
V_{DS}	Drain to Source Voltage		100	V
V_{GS}	Gate to Source Voltage		± 20	V
I_D	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	5.5	A
	-Pulsed	(Note 4)	130	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	181	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	50	W
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		2.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC035N10	FDMC035N10X1	Power 33	13"	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		107		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	2.5	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 5.5 \text{ A}$		30	37	m Ω
		$V_{GS} = 6 \text{ V}, I_D = 5.0 \text{ A}$		32	41	
		$V_{GS} = 10 \text{ V}, I_D = 5.5 \text{ A}, T_J = 125^\circ\text{C}$		60	75	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 5.5 \text{ A}$		18		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1\text{MHz}$		1910	2675	pF
C_{oss}	Output Capacitance			109		pF
C_{rss}	Reverse Transfer Capacitance			64		pF
R_g	Gate Resistance		0.1	2.6	5.2	Ω

Switching Characteristics

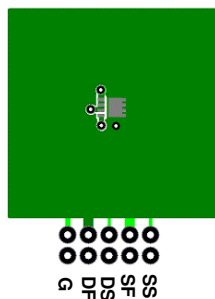
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 5.5 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		12	21	ns	
t_r	Rise Time			7	13	ns	
$t_{d(off)}$	Turn-Off Delay Time			56	90	ns	
t_f	Fall Time			14	25	ns	
Q_g	Total Gate Charge		$V_{GS} = 0 \text{ V to } 10 \text{ V}$		41	58	nC
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 6 \text{ V}$	$V_{DD} = 50 \text{ V},$ $I_D = 5.5 \text{ A}$		27	38	nC
Q_{gs}	Gate to Source Charge				6.3		nC
Q_{gd}	Gate to Drain "Miller" Charge				11		nC

Drain-Source Diode Characteristics

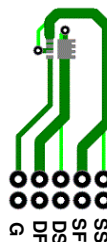
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 5.5 \text{ A}$ (Note 2)		0.8	1.3	V
t_{rr}	Reverse Recovery Time	$I_F = 5.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		42	68	ns
Q_{rr}	Reverse Recovery Charge			58	92	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5 \text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $53^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad

2. Pulse Test: Pulse Width < $300 \mu\text{s}$, Duty cycle < 2.0%.

3. E_{AS} of 181 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3 \text{ mH}, I_{AS} = 11 \text{ A}, V_{DD} = 100 \text{ V}, V_{GS} = 10 \text{ V}$. 100% test at $L = 0.1 \text{ mH}, I_{AS} = 35 \text{ A}$.

4. Pulsed I_D please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

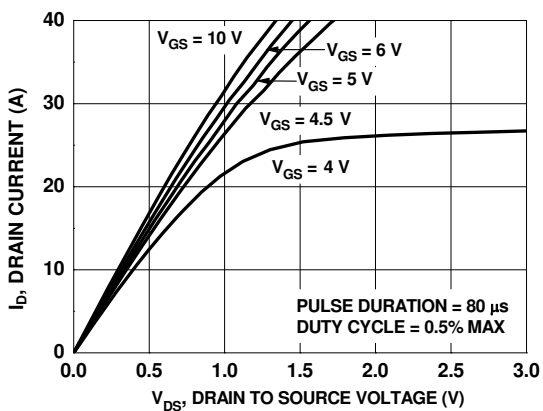


Figure 1. On Region Characteristics

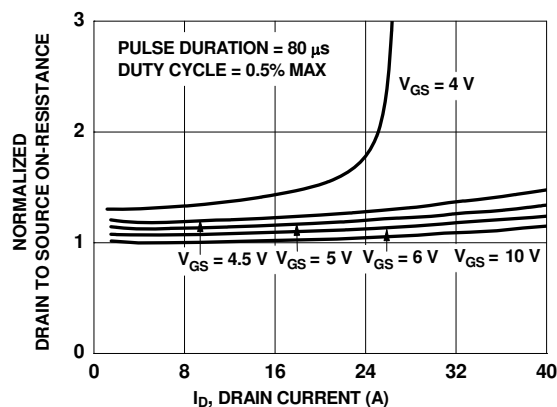


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

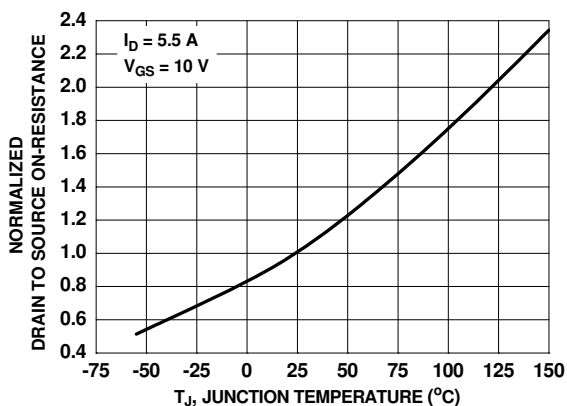


Figure 3. Normalized On Resistance vs. Junction Temperature

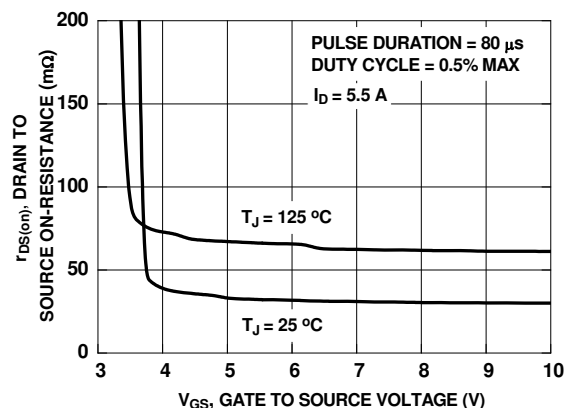


Figure 4. On-Resistance vs. Gate to Source Voltage

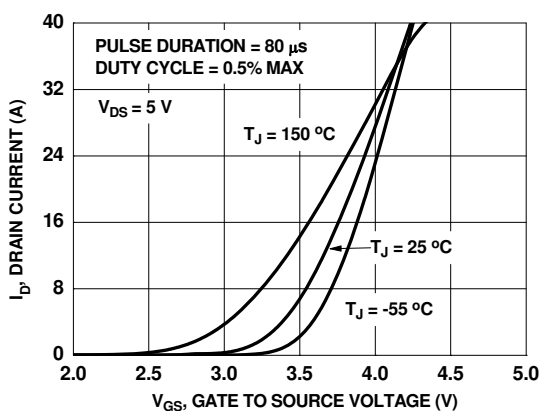


Figure 5. Transfer Characteristics

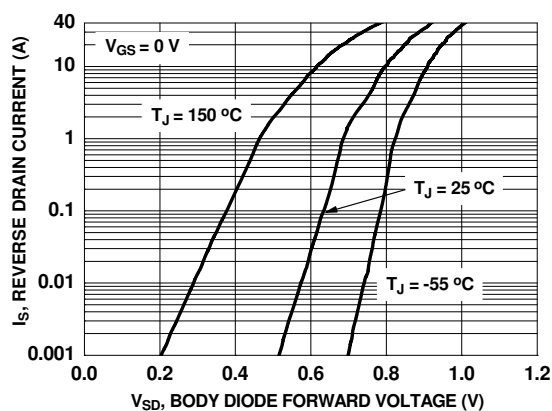


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

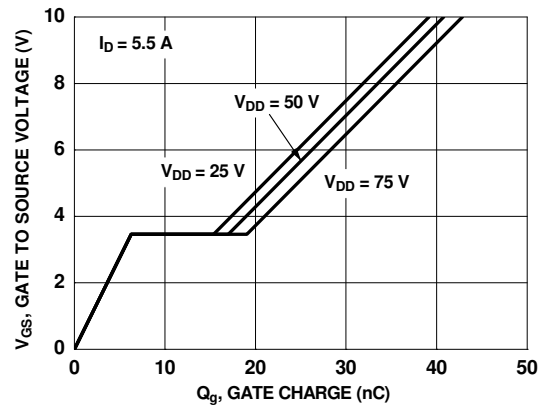


Figure 7. Gate Charge Characteristics

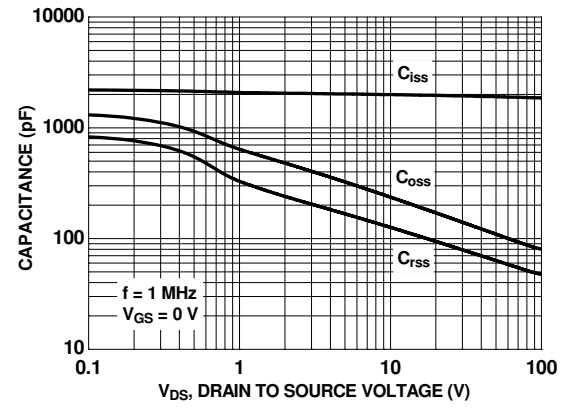


Figure 8. Capacitance vs. Drain to Source Voltage

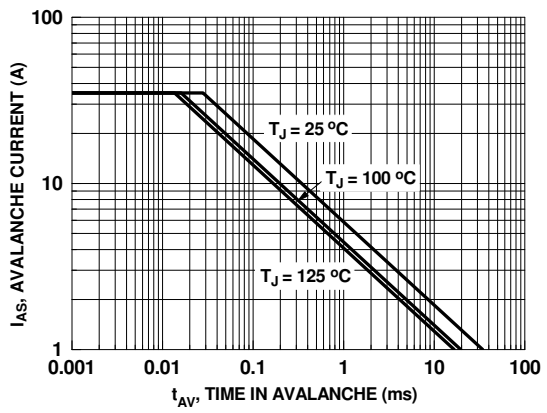


Figure 9. Unclamped Inductive Switching Capability

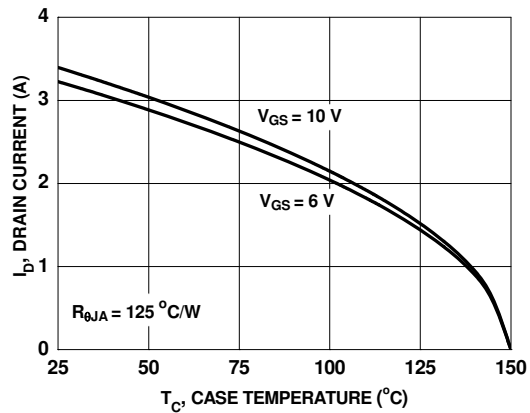


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

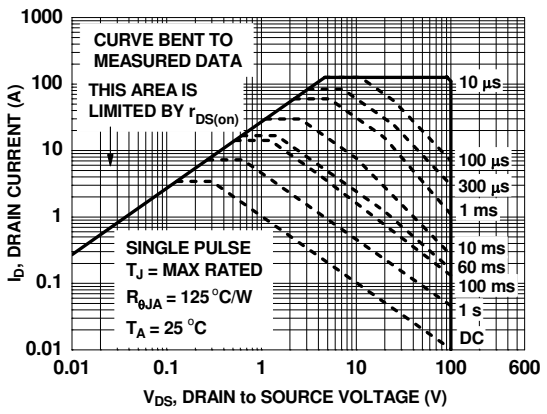


Figure 11. Forward Bias Safe Operating Area

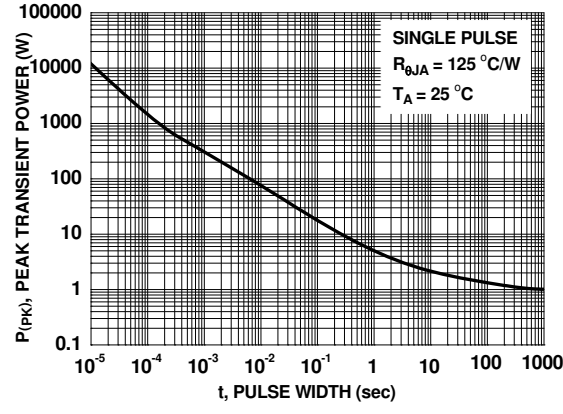


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

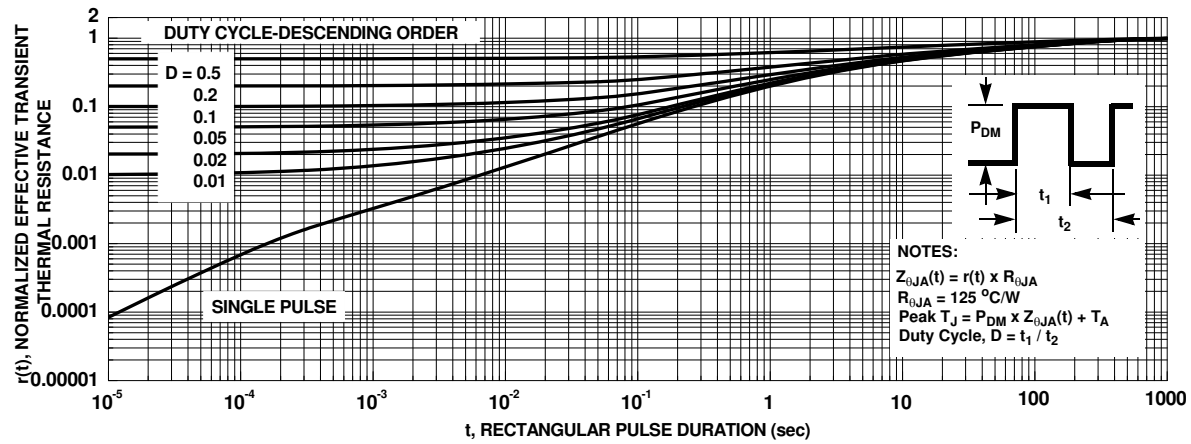
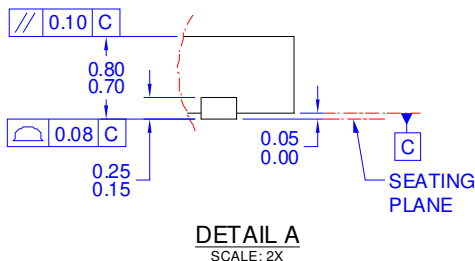
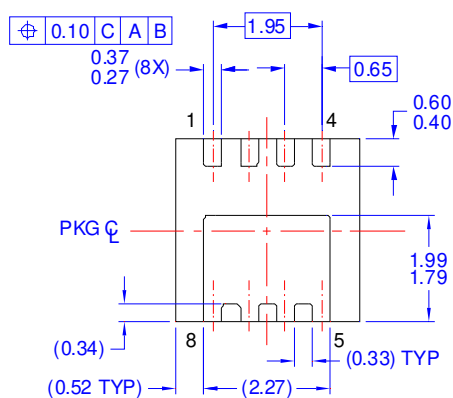
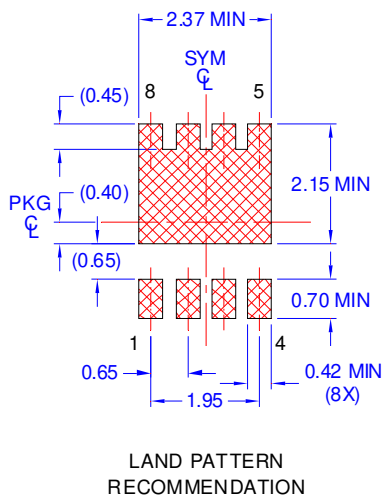
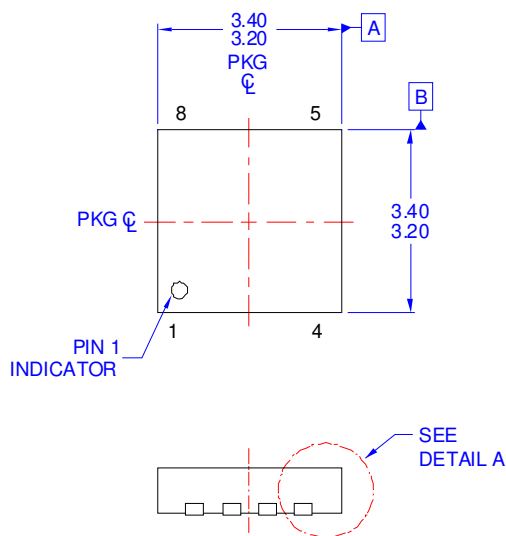


Figure 13. Junction to Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) DRAWING FILE NAME: MKT-PQFN08SREV1

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