Single-Phase Synchronous Buck PWM Controller

General Description

The RT8120 is a single-phase synchronous buck PWM DC-DC controller designed to drive two N-MOSFET. It provides a highly accurate, programmable output voltage precisely regulated to low voltage requirements with an internal 0.8V ±1% (option for 0.6V ±1.5%) reference. The RT8120 uses a single feedback loop voltage mode PWM control for fast transient response. An oscillator with fixed frequency 300kHz reduces the external inductor and capacitor component size for saving PCB board area. The RT8120 provides fast transient response to satisfy high current output applications while minimizing external components. It is suitable for high performance graphic processors, DDR and VTT power. The RT8120 incorporates an externally compensated error amplifier and an internal soft-start and output enable. The RT8120 comes in SOP-8 and SOP-8 (Exposed Pad) packages.

Ordering Information

RT8120□□□

- Package Type
  - S : SOP-8
  - SP : SOP-8 (Exposed-Pad-Option 1)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
  - Z : ECO (Ecological Element with Halogen Free and Pb free)
- Reference Voltage
  - A/C : 0.6V
  - B/D : 0.8V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

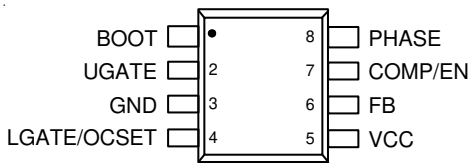
- **Wide Input Voltage Range : 3V to 13.2V**
- **Embedded Switching Boot Diode**
- **0.8V ±1%, 0.6V ±1.5% Internal Reference**
- **Shoot-Through Protection and Short Pulse Free Technology for Gate Drivers**
- **Fixed Frequency 300kHz**
- **Internal Soft-Start**
- **Over Current Protection by Sensing MOSFET $R_{DS(ON)}$**
- **Enable/Shutdown Control**
- **Drives Two N-MOSFETs**
- **Full Duty Cycle : 0% to 85%**
- **Fast Transient Response**
- **Voltage Mode PWM Control with External Feedback Loop Compensation**
- **Pinless LGATE Over Current Setting (LGOCS)**
- **Under Voltage Protection**
- **SOP-8 and SOP-8 (Exposed Pad) Packages**
- **RoHS Compliant and Halogen Free**

Applications

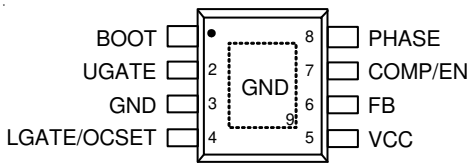
- System (Graphic, MB) with 5V or 12V Power
- Graphic Cards (AGP 8X, 4X, PCI Express*16)
- 3.3V to 12V Input DC-DC Regulators
- Low Voltage Distributed Power Supplies

Pin Configuration

(TOP VIEW)



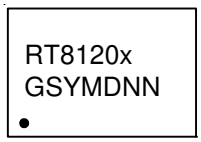
SOP-8



SOP-8 (Exposed Pad)

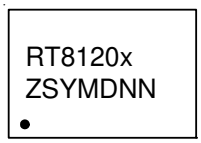
Marking Information

RT8120xGS



RT8120xGS : Product Number
YMDNN : Date Code

RT8120xZS



RT8120xZS : Product Number
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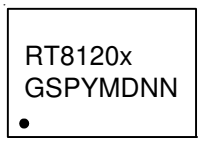
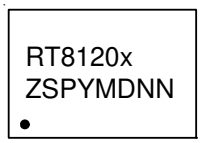
RT8120xGSP



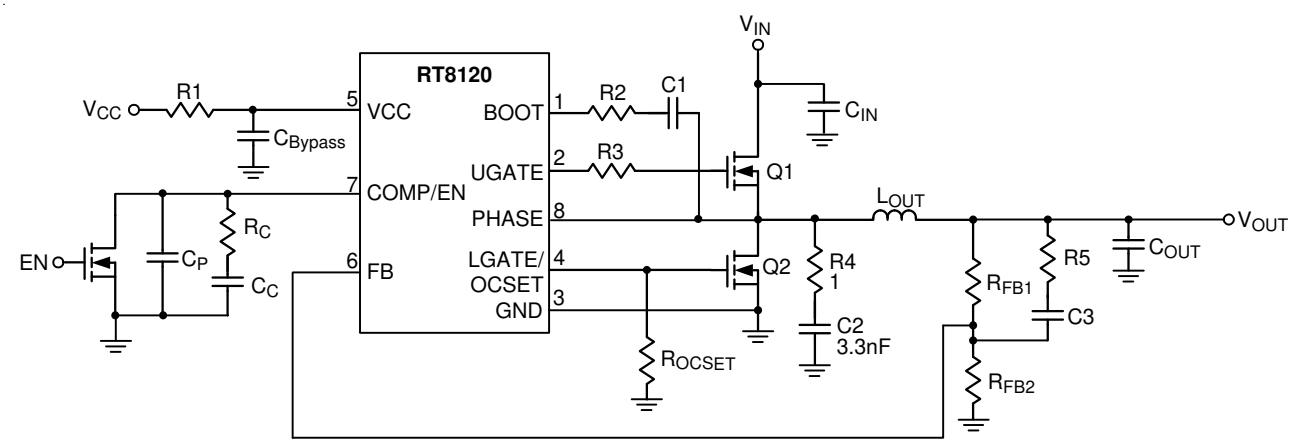
RT8120xGSP : Product Number
YMDNN : Date Code

RT8120xZSP

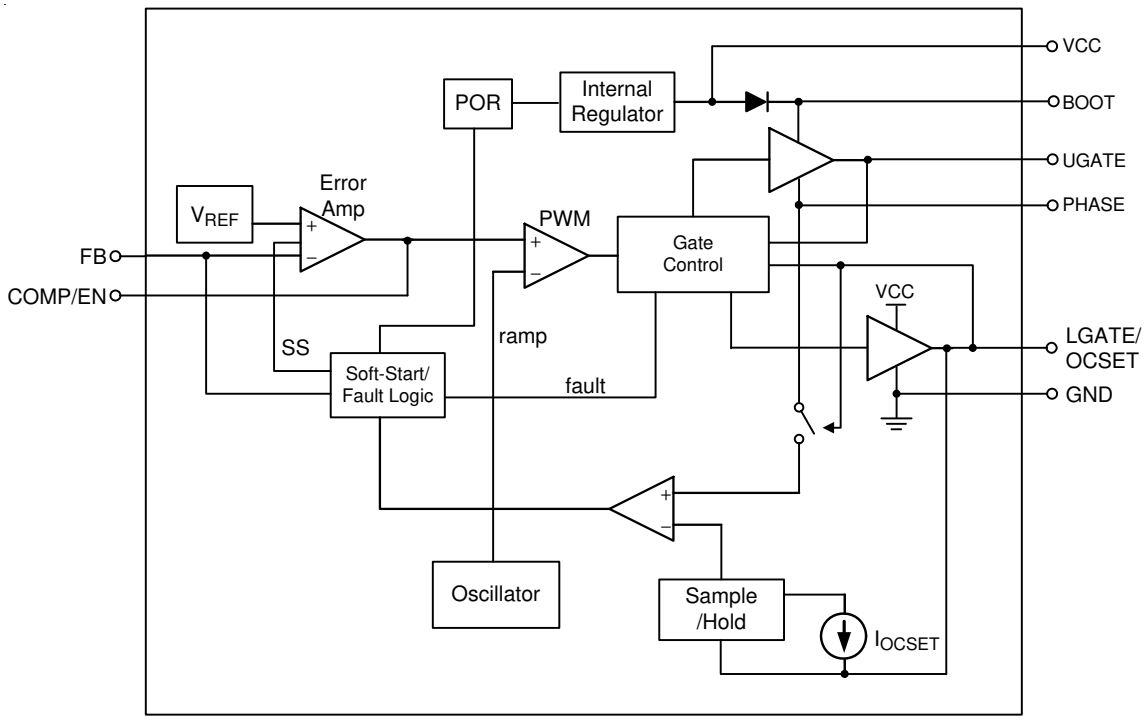


RT8120xZSP : Product Number
YMDNN : Date Code

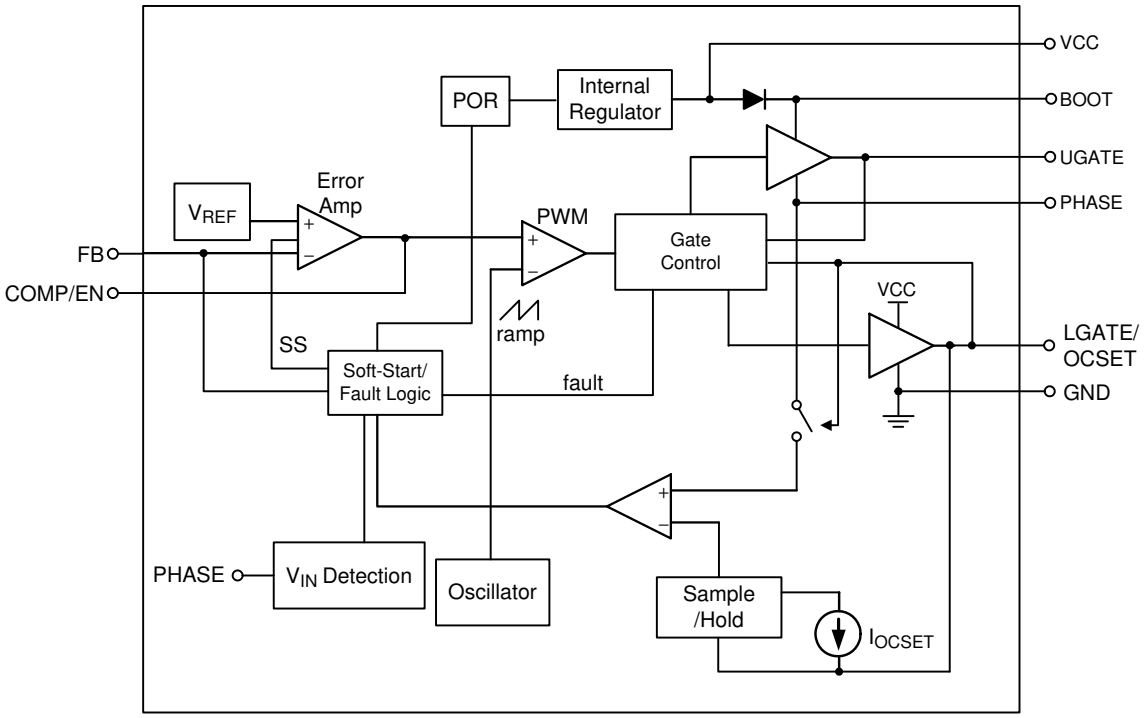
Typical Application Circuit



Functional Block Diagram



Figuer 1. RT8120A/B Function Block Diagram



Figuer 2. RT8120C/D Function Block Diagram

Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-8	SOP-8 (Exposed Pad)		
1	1	BOOT	Bootstrap Power Pin. This pin powers the upper gate driver. Connect a bootstrap capacitor between the BOOT pin and PHASE pin on the upper MOSFET.
2	2	UGATE	Upper-Gate Driver Output. Connect to gate of the high side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
3	3, 9 (Exposed Pad)	GND	Ground for the IC. All voltage levels are measured with respect to this pin. Connect this pin directly to the low side MOSFET source and ground plane with the lowest impedance. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	4	LGATE/OCSET	Lower-Gate Driver Output. Connect to the gate of the low side power N-MOSFET. It provides the PWM-controlled gate drive (from VCC). This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. During a short period of time following Power-On Reset (POR) or shutdown release, this pin is also used to determine the over-current threshold of the converter (LGOCS). Connect a resistor (R_{OCSET}) from this pin to GND. See the over current protection section for equations.
5	5	VCC	Supply Input Pin. Connect this pin to a well-decoupled 5V or 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.
6	6	FB	Feedback Input Pin. This pin is the inverting input of the error amplifier. FB senses the switch output through an external resistor divider network.
7	7	COMP/EN	Feedback Compensation. And could be used as EN pin, when COMP < 0.4V, to disable entire chip.
8	8	PHASE	Switch Node. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

Absolute Maximum Ratings (Note 1)

- VCC to GND, VCC ---------- 15V
- BOOT to PHASE, $V_{BOOT-PHASE}$ ---------- 15V
- PHASE to GND
  - DC ---------- –0.5V to 15V
  - < 20ns ---------- –8V to 25V
- UGATE to PHASE
  - DC ---------- –0.3V to ($V_{BOOT-PHASE}$ + 0.3V)
  - < 20ns ---------- –5V to ($V_{BOOT-PHASE}$ + 5V)
- LGATE to GND
  - DC ---------- –0.3V to (V_{CC} + 0.3V)
  - < 20ns ---------- –5V to (V_{CC} + 5V)
- Other Pins ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 ---------- 0.53W
  - SOP-8 (Exposed Pad) ---------- 3.26W
- Package Thermal Resistance (Note 2)
  - SOP-8, θ_{JA} ---------- 188°C/W
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 30.6°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 3.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 3V to 13.2V
- Control Input Voltage, VCC ---------- 4.5V to 13.2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	UGATE, LGATE Open, V_{CC} = 12V	--	1.5	--	mA
Shutdown Current	I_{SHDN}	UGATE, LGATE Open, V_{CC} = 12V	--	0.7	--	mA
Power On Reset Threshold	V_{CCR_TH}	V_{CC} Rising	3.9	4.1	4.3	V
Power On Reset Hysteresis	V_{CC_Hys}		0.26	0.45	0.64	V
Switching Frequency	f_{OSC}		270	300	330	kHz
Ramp Amplitude	ΔV_{OSC}		--	1.3	--	V_{P-P}
Minimum Duty Cycle			0	--	--	%
Maximum Duty Cycle	D_{MAX}		--	85	--	%
Reference Voltage	V_{REF}	RT8120A/C	0.591	0.6	0.609	V
		RT8120B/D	0.792	0.8	0.808	
Open Loop DC Gain	A_{DC}	Guaranteed by Design	--	70	--	dB
Gain Bandwidth	GBW	Guaranteed by Design	--	10	--	MHz
Slew Rate	SR	Guaranteed by Design, C_L = 10pF	--	6	--	V/μs
Transconductance	gm		500	700	--	μA/V
Output Source Current	I_{COMPSK}	V_{FB} < V_{REF}	80	120	--	μA
Output Sink Current	I_{COMPSC}	V_{FB} < V_{REF}	80	120	--	μA
Soft-Start Time	t_{SS}	RT8120A/C	--	1.5	--	ms
		RT8120B/D	--	2	--	
Upper Gate Sourcing Ability	I_{UG_SRC}	V_{BOOT} – V_{PHASE} = 12V, max source current	--	1.2	--	A
Upper Gate $R_{DS(ON)}$ Sinking	R_{UG_SNK}	V_{UGATE} – V_{PHASE} = 0.1V	--	3	--	Ω
Lower Gate Sourcing Ability	I_{LG_SRC}	V_{CC} = 12V, max source current	--	1.2	--	A
Lower Gate $R_{DS(ON)}$ Sinking	R_{LG_INK}	V_{LGATE} = 0.1V	--	1.8	--	Ω
Deadtime between UGATE Off to LGATE On		V_{UGATE} – V_{PHASE} = 1.2V to V_{LGATE} =1.2V	--	30	--	ns
Deadtime Between LGATE Off to UGATE On		V_{UGATE} – V_{PHASE} = 1.2V to V_{LGATE} = 1.2V	--	30	--	ns
Internal BOOT Switch						
Internal BOOT Switch On-Resistance	R_{BOOT}	VCC to BOOT, 10mA	--	--	80	Ω
Protection						
Under Voltage Protection	V_{UVP_FB}		65	75	80	%
Under Voltage Delay	V_{D_UVP}		--	6	--	μs
LGATE OC Setting Current	I_{OCSET}		9	10	11	μA
Over Current Threshold	V_{PHASE}	R_{OCSET} = Open	--	375	--	mV
Enable Threshold	V_{EN}		0.3	0.4	0.55	V

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

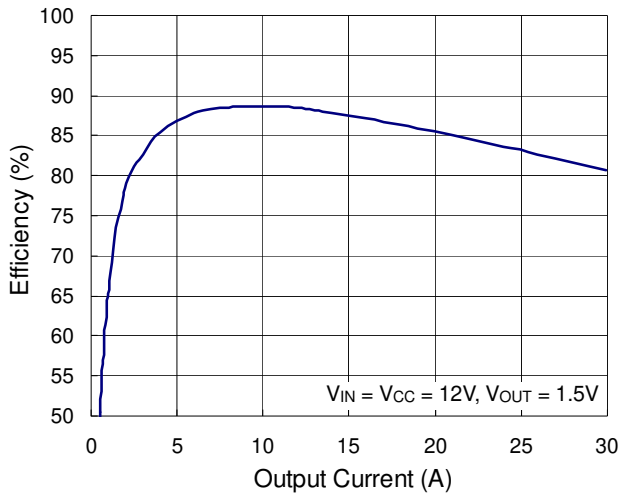
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

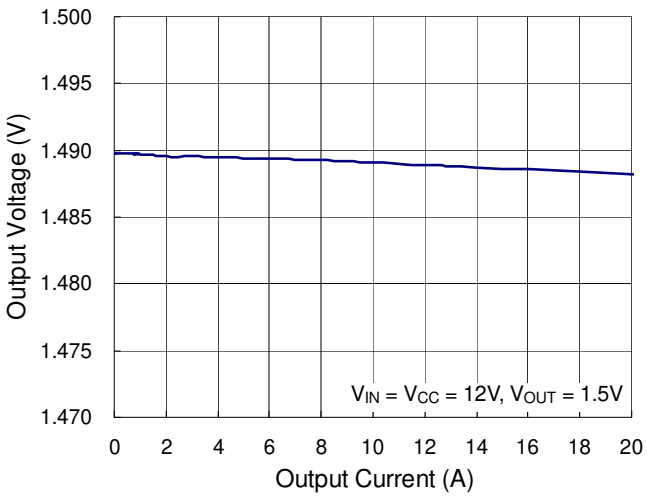
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

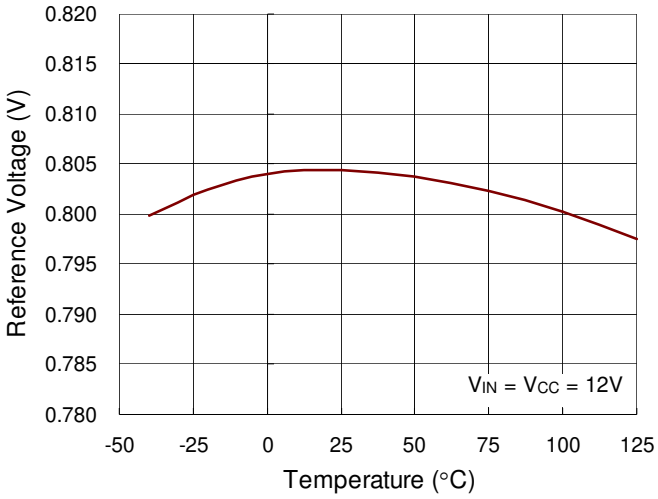
Efficiency vs. Output Current



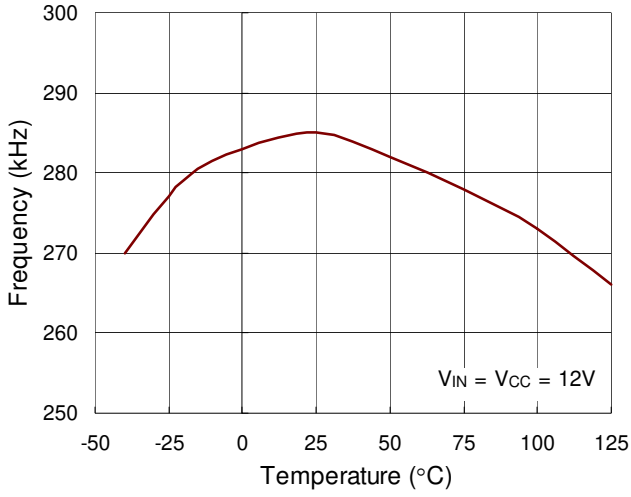
Output Voltage vs. Output Current



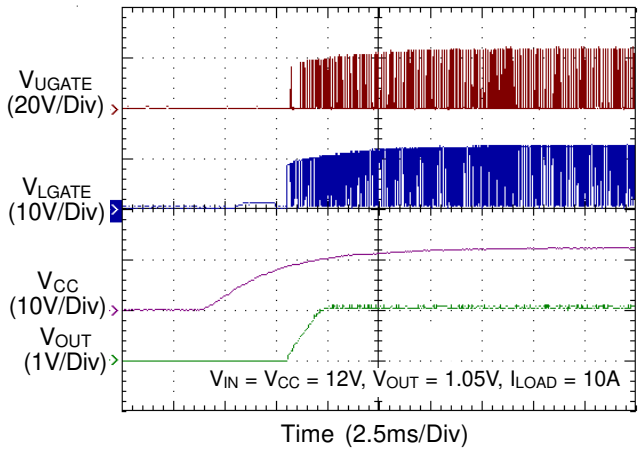
Reference Voltage vs. Temperature



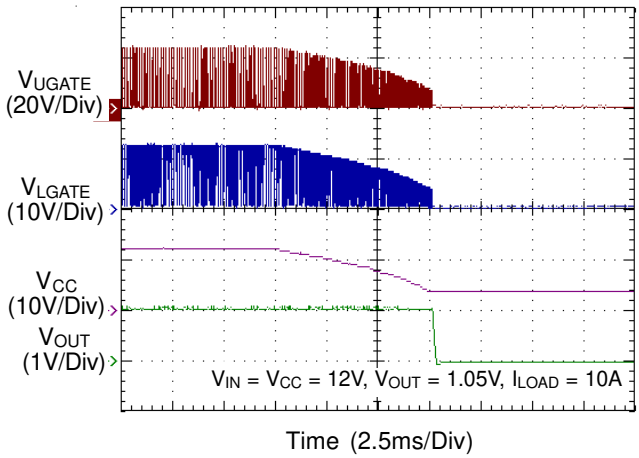
Frequency vs. Temperature



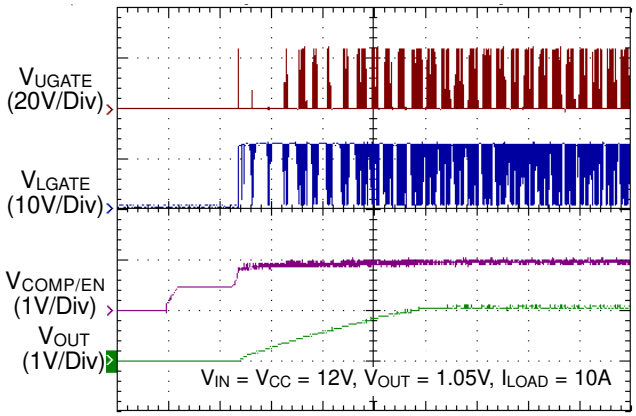
Power On



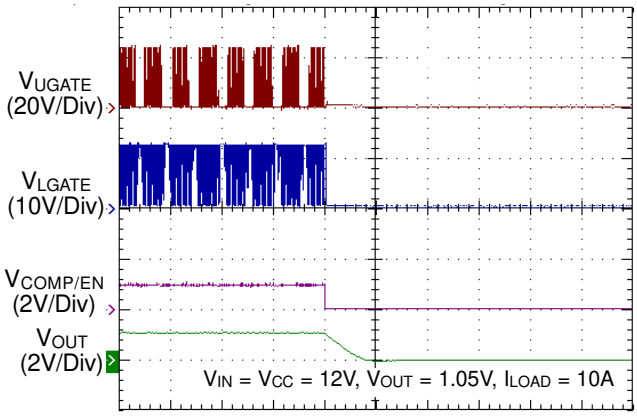
Power Off



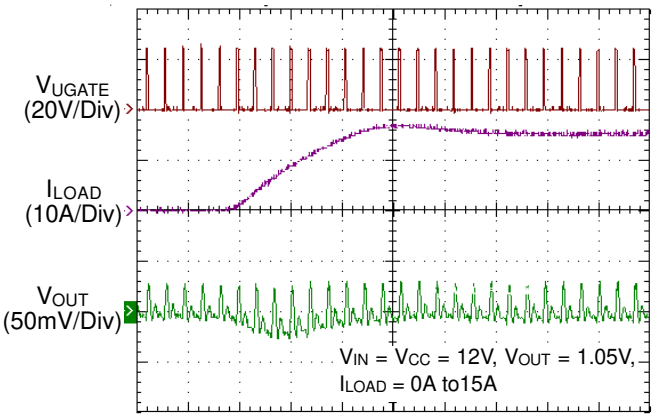
COMP/EN Power On



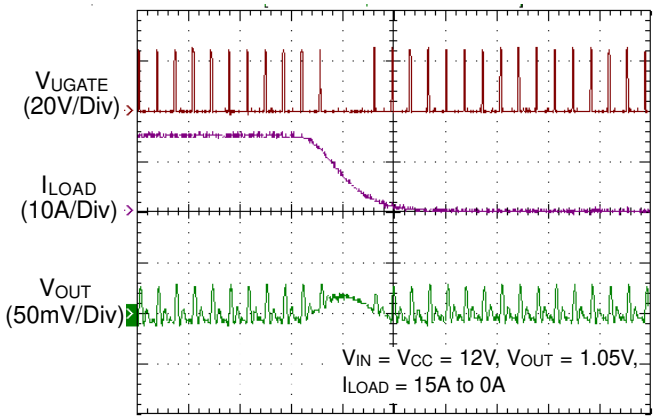
COMP/EN Power Off



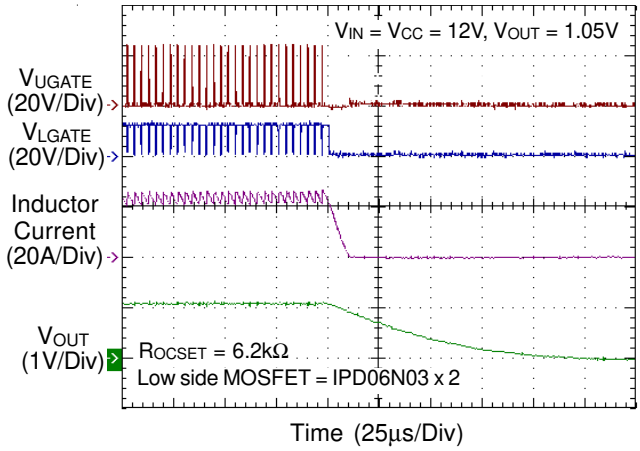
Load Transient Response



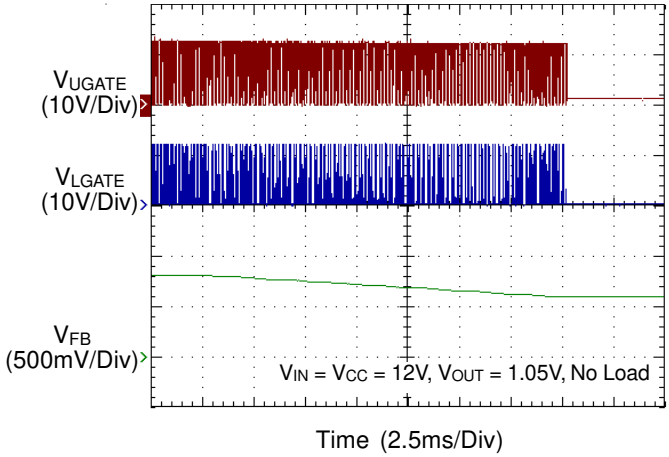
Load Transient Response



Over Current Protection



Under Voltage Protection



Application Information

Function Description

The RT8120 is a single-phase synchronous buck PWM controller with integrated N-MOSFET gate drivers. The RT8120 can be used in a broad variety of applications, with its wide input voltage range from 3V or 13.2V. It provides single feedback loop, voltage mode control with fast transient response. An internal 0.8V (option for 0.6V) reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed frequency (300kHz) oscillator is integrated to minimize external components. Protection features include programmable over current protection and Under Voltage Lockout (UVLO).

Supply Voltage and Power On Reset (POR)

The input voltage range for VCC is from 4.5 V to 13.2 V with respect to GND. An internal linear regulator regulates the supply voltage for internal control logic circuit. A minimum 0.1μF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC. VCC also supplies the integrated MOSFET drivers. A bootstrap diode is embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications.

The Power-On Reset (POR) circuit monitors the supply voltage at the VCC pin. If VCC exceeds the POR rising threshold voltage (typ. 4V), the controller resets and prepares the PWM for operation. If VCC falls below the POR falling threshold during normal operation, all MOSFETs stop switching. The POR rising and falling threshold has a hysteresis (typ.0.45V) to prevent unintentional noise based reset.

Chip Enable and Disable

The COMP/EN pin of the RT8120 is a multiplexed pin. During soft-start and normal converter operation, this pin represents the output of the error amplifier. When COMP/EN pin voltage falls or is pulled externally below the enable level V_{EN}, the chip shuts down. When the controller shuts down, UGATE and LGATE signals will go low. When the pull-down device is released and the COMP/EN pin rises above the V_{EN} trip point, the RT8120 will begin a new initialization and soft-start cycle. This allows flexible power sequence control for specified application. In practical applications, connect a small-signal MOSFET to the COMP/EN pin to implement the enable/disable function.

VIN Detection (RT8120C/D Only)

Once VCC exceeds its power on reset (POR) rising threshold voltage, UGATE will output continuous pulses (~60kHz, 200ns), and LGATE will be forced low for converter input voltage V_{IN} detection. If the voltage pulses at the PHASE pin exceed 1V when UGATE is turned on, V_{IN} is recognized as ready. Then, the controller will initiate soft-start operation.

Internal Soft-Start

The RT8120 provides an internal soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered-up. The soft-start function automatically begins once the chip is enabled. An internal current source charges the internal soft-start capacitor such that the internal soft-start voltage ramps up uniformly. The FB voltage will track the internal soft-start voltage during the soft-start interval. Therefore, the PWM pulse width increases gradually to limit the input current. After the internal soft-start voltage exceeds the reference voltage, the FB voltage no longer tracks the soft-start voltage but rather follows the reference voltage. Therefore, the duty cycle of the UGATE signal as well as the input current at power up are limited.

Over Current Protection (OCP)

The RT8120 provides lossless over current protection by detecting the voltage drop across the low side MOSFET when it is turned on. The over current trip threshold is set by an external resistor, R_{OCSET}, at LGATE. During the initial stage when LGATE is turned on, the RT8120 samples and holds the phase voltage. The sample-and-hold voltage represents the valley inductor current and is compared to the OCP threshold. If the sensed phase voltage is lower than the OCP threshold, OCP will be triggered. Both UGATE and LGATE will go low, and the controller will enter the hiccup mode until the OCP condition is released.

LGATE Over Current Setting (LGOCS)

Over current threshold is externally programmed by adding a resistor (R_{OCSET}) between LGATE and GND. Once VCC exceeds the POR threshold, an internal current source I_{OCSET} flows through R_{OCSET}. The voltage across R_{OCSET} is stored as the over current protection threshold V_{OCSET}. After that, the current source is switched off. R_{OCSET} can be determined using the following equation :

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

where I_{VALLEY} represents the desired inductor OCP trip current (valley inductor current).

If R_{OCSET} is not present, there is no current path for I_{OCSET} to build the OCP threshold. In this situation, the OCP threshold is internally preset to 375mV (typical).

Under Voltage Protection (UVP)

The voltage on the FB pin is monitored for under voltage protection. If the FB voltage is lower than the UVP threshold (typically 75% x V_{REF}) during normal operation, UVP will be triggered. When the UVP is triggered, both UGATE and LGATE go low. The controller enters hiccup mode until the UVP condition is removed.

Output Voltage Setting

The RT8120 allows the output voltage of the DC-DC converter to be adjusted from 0.8V (option for 0.6V) to 85% of V_{IN} via an external resistor divider. It will try to maintain the feedback pin at internal reference voltage (0.8V, with option for 0.6V).

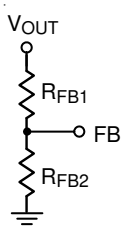


Figure 3. Output Voltage Setting

According to the resistor divider network above, the output voltage is set as :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

MOSFET Drivers

The RT8120 integrates high current gate drivers for the two N-MOSFETs to obtain high efficiency power conversion in synchronous buck topology. A dead time is used to prevent crossover conduction for the high side and low side MOSFETs. Because both gate signals are off during dead time, the inductor current freewheels through the body diode of the low side MOSFET. The freewheeling current and the forward voltage of the body diode contribute to power loss. The RT8120 employs constant dead time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, elaborate logic circuit is implemented to prevent cross conduction.

For high output current applications, two or more power MOSFETs are usually paralleled to reduce $R_{DS(ON)}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. Gate driver with lower source/ sink current capability result in longer rising/ falling time in gate signals, and therefore higher switching loss.

The RT8120 embeds high current gate drivers to obtain high efficiency power conversion. The embedded drivers contribute to the majority of the power dissipation of the controller. Therefore, SOP package is chosen for its power dissipation rating. If no gate resistor is used, the power dissipation of the controller can be approximately calculated using the following equation :

$$P_{DRIVER} = f_{SW} \times (Q_G \times V_{BOOT} + Q_{G\_LOW\ SIDE} \times V_{DRIVER\_LOW\ SIDE})$$

where V_{BOOT} represents the voltage across the bootstrap capacitor and f_{SW} is the switching frequency.

It is important to ensure the package can dissipate the switching loss and have enough room for safe operation.

Inductor Selection

The inductor plays an importance role in step-down converters because it stores the energy from the input power rail and then releases the energy to the load. From the viewpoint of efficiency, the dc resistance (DCR) of the inductor should be as small as possible to minimize the conduction loss. In addition, the inductor covers a significant proportion of the board space, so its size is also important. Low profile inductors can save board space

especially when the height has a limitation. However, low DCR and low profile inductors are usually cost ineffective.

Additionally, larger inductance results in lower ripple current, which translates into the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, inductance is chosen such that the ripple current ranges between 20% to 40% of the full load current. The inductance can be calculated using the following equation :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_RATED}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters when selecting an input capacitor. Conservatively speaking, an input capacitor should have a voltage rating 1.5 times greater than the maximum input voltage to be considered a safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for the RMS current rating. Using more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Placing the ceramic capacitor close to the drain of the high side MOSFET can also be helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output capacitor and the inductor form a low-pass filter in the buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in voltage ripple. The output voltage ripples contains two components, ΔV_{OUT_ESR} and ΔV_{OUT_C}.

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR$$

$$\Delta V_{OUT\_C} = \Delta I_L \times \frac{1}{8 \times C_{OUT} \times f_{SW}}$$

When load transient occurs, the output capacitor supplies the load current before controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage sag can be calculated using the following equation :

$$V_{OUT\_SAG} = ESR \times \Delta I_{OUT}$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore ESL contributes to part of the voltage sag. Using a capacitor with low ESL will obtain better transient performance. Generally, using several capacitors connected in parallel will also have better transient performance than just one single capacitor with the same total ESR.

Unlike electrolytic capacitors, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, it is suggested to use a mixed combination of electrolytic capacitor and ceramic capacitor for achieving better transient performance.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high side MOSFET is small. Therefore, the switching loss of the high side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application. However, the small duty cycle means the low side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state

resistance. However, this depends on the low side MOSFET driver capability and the budget.

It is recommended to bypass low side MOSFET with a snubber circuit (R = 1Ω, C = 3.3nF).

Compensation Network Design

The RT8120 is a voltage mode controller and requires external compensation to have an accurate output voltage regulation with fast transient response. The RT8120 uses a high gain operational transconductance amplifier (EOTA) as the error amplifier. As Figure 4 shows, the EOTA works as the voltage controlled current source. The calculation of the transconductance is shown below :

$$GM = \frac{\Delta I_{OUT}}{\Delta V_M}, \text{ where } \Delta V_M = (V_{IN+}) - (V_{IN-})$$

$$\text{and } \Delta V_{COMP} = \Delta I_{OUT} \times Z_{OUT}$$

Figure 5 shows a typical buck control loop using a Type II compensator. The control loop consists of the power stage, PWM comparator and a compensator. The PWM comparator compares V_{COMP} with the oscillator (OSC) sawtooth wave to provide a Pulse-Width Modulated (PWM) with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter L_{OUT} and C_{OUT}. The output voltage (V_{OUT}) is sensed and fed to the inverting input of the error amplifier.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP} (output voltage over the error amplifier output). This transfer function is dominated by a DC gain, a double pole, and an ESR zero as shown in Figure 6.

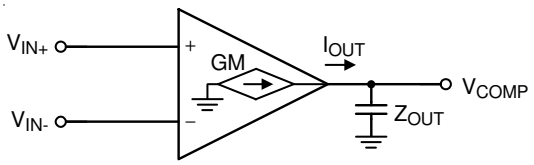


Figure 4. Operational Transconductance Amplifier, EOTA

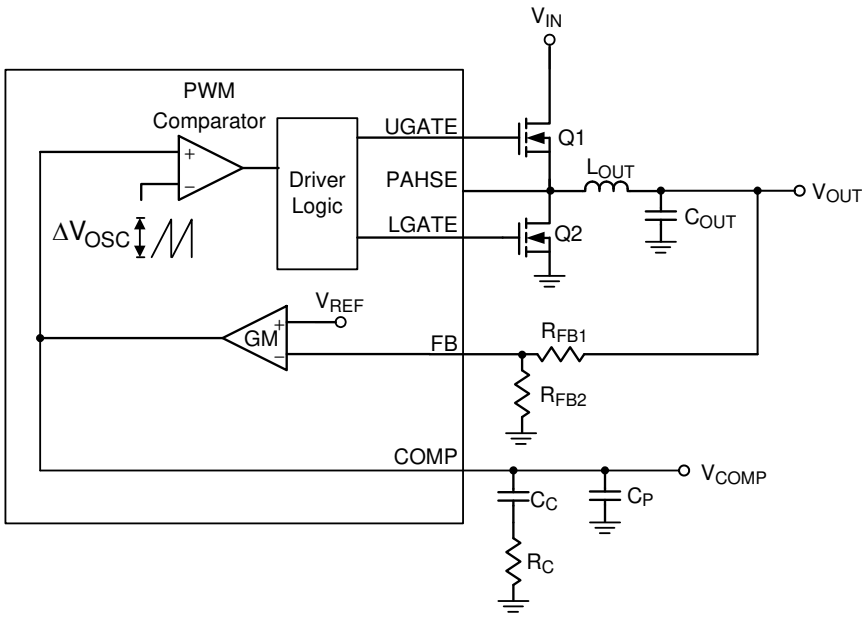


Figure 5. Typical Voltage Mode Buck Converter Control Loop

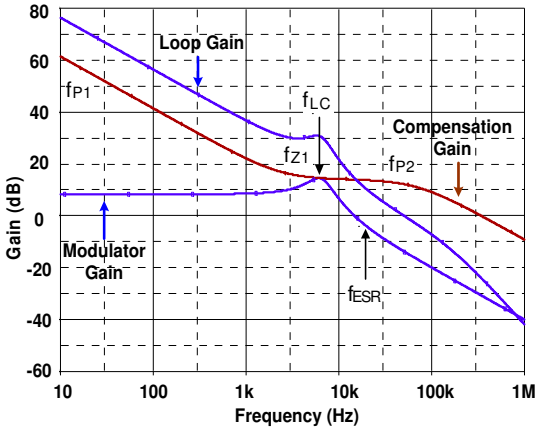


Figure 6. Typical Bode Plot of a Voltage Mode Buck Converter

The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage V_{OSC}.

$$Gain_{MODULATOR} = \frac{V_{IN}}{\Delta V_{OSC}}$$

The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter is expressed as :

$$f_{LC} = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as follows :

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

The goal of the compensation network is to provide adequate phase margin (usually greater than 45 degrees) and the highest bandwidth (0dB crossing frequency). It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of –20dB/dec. According to Figure 6, the compensation network frequency is as below :

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times R_C \times \left(\frac{C_C \times C_p}{C_C + C_P}\right)}$$

$$f_{Z1} = \frac{1}{2\pi \times R_C \times C_C}$$

To determine the 0dB crossing frequency (f_C, control loop bandwidth) is the first step of compensator design. Usually, the f_C is set to 0.1 to 0.3 times the switching frequency. The second step is to calculate the open loop modulator gain and find out the gain loss at f_C. The third step is to design a compensator gain that can compensate the modulator gain loss at f_C. The final step is to design f_{Z1} and f_{P2} to allow the loop sufficient phase margin. f_{Z1} is designed to cancel one of the double poles of modulator. Usually, place f_{Z1} before f_{LC}. f_{P2} is usually placed below the switching frequency (typically, 0.5 to 1 times the switching frequency) to cancel high frequency noise.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 package, the thermal resistance, θ_{JA}, is 188°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 30.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (188°C/W) = 0.53W for SOP-8 package

$P_{D(MAX)}$ = (125°C – 25°C) / (30.6°C/W) = 3.26W for SOP-8 (Exposed Pad) package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 7 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

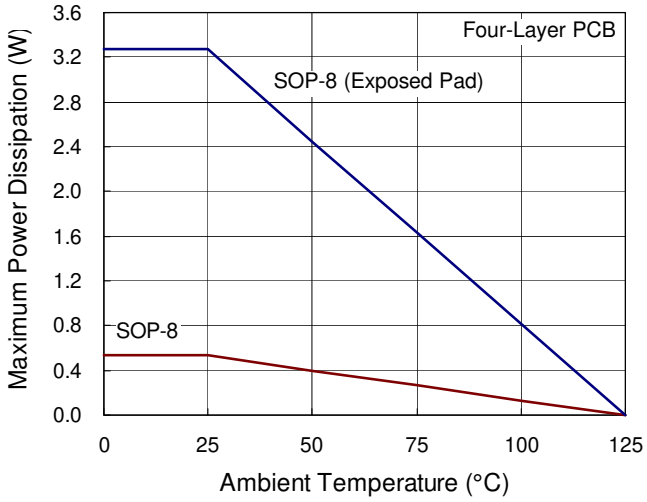


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Considerations

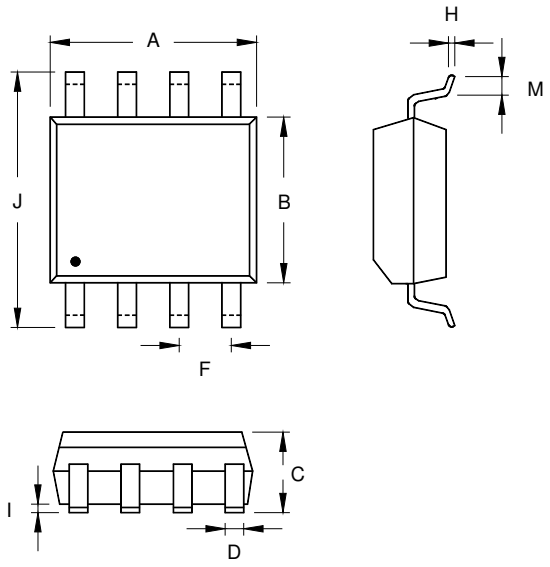
Layout planning plays a critical role in modern high-frequency switching converter design. Circuit boards with good layout can help the IC function properly and achieve low losses, low switching noise, and stable operation with improved performance. Without a good layout, the PCB could radiate excessive noise, causing noise-induced IC problems and converter instability. The following guidelines is suggested have better IC performance.

- The power components should be placed first. Keep the connection between power components as short as possible.
- Input bulk capacitors should be placed close to the drain of the high side MOSFET and the source of the low side MOSFET.
- Place the VCC bypass capacitor as close as possible to the RT8120.
- Minimize the trace length between the power MOSFETs and its drivers.

  Since the drivers use short, high current pulses to drive the power MOSFETs, the driving traces should be as short and wide as possible to reduce the trace inductance. This is especially true for the low side MOSFET, since this can reduce the possibility of the shoot through.
- Provide enough copper area around the power MOSFETs and the inductors to aid in heat sinking. Using thick copper PCB can also reduce the resistance and inductance to improve efficiency.
- The bank of the output capacitor should be placed physically close to the load. This can minimize the impedance seen by the load and then improve the transient response.
- Placing all the high frequency decoupling ceramic capacitors close to their decoupling targets.
- Small-signal components should be located as close as possible to the IC. The small signal components include the feedback components, current sensing components, compensation components, function setting components and any bypass capacitors.

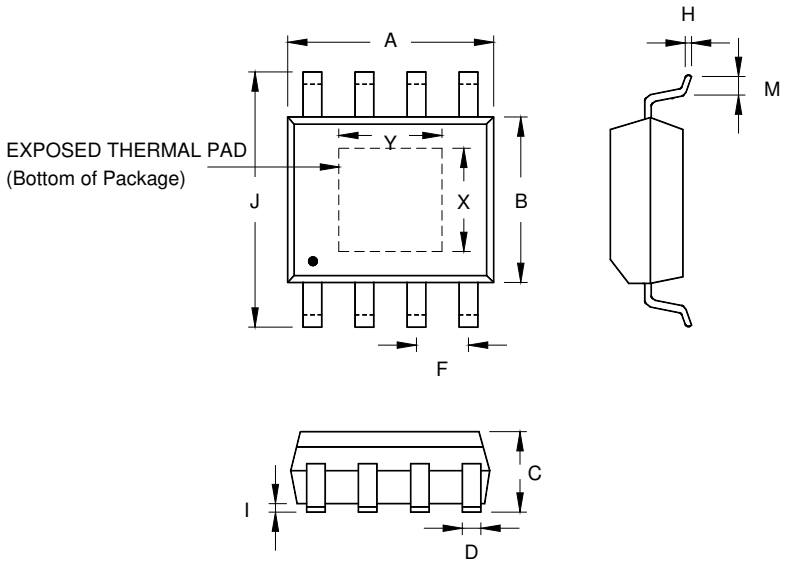
  These components belong to the high impedance circuit loop and are inherently sensitive to noise pick-up. Therefore, they must be located close to their respective controller pins and away from the noisy switching nodes.
- A multi-layer PCB design is recommended. Make use of one single layer as the power ground and have a separate control signal ground as the reference of all signals.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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