ADP3430

8−Bit, Programmable 2− to 3−Phase Synchronous Buck Controller

The ADP3430 is a highly efficient, multi−phase, synchronous buck switching regulator controller optimized for converting a 12 V main supply voltage into the core supply voltage of high performance Intel processors. It uses an internal 8−bit DAC to read a Voltage Identification (VID) code directly from the processor, to set the output voltage between 0.5 V and 1.6 V.

This device uses a multi−mode control architecture to drive the logic−level PWM outputs. The switching frequency can be programmed according to VR size and efficiency. The chip can provide 2− or 3−phase operation, allowing for the construction of up to four complementary buck switching stages.

The ADP3430 also includes programmable no load offset and load line slope setting function that adjusts the output voltage as a function of the load current, optimally positioning it for a system transient. The ADP3430 also provides accurate and reliable short−circuit protection, adjustable current limit, and a delayed power−good output that accommodates On−The−Fly (OTF) output voltage changes requested by the CPU.

Features

- Selectable 2− or 3−Phase Operation at Up to 1 MHz Per Phase
- ±8 mV Worst−Case Differential Sensing Error
- Logic−Level PWM Outputs for Interface to External High Power Drivers
- Fast−Enhanced PWM FlexMode™ for Excellent Load Transient Performance
- TRDET to Improve Load Release
- Active Current Balancing Between All Output Phases
- Built−In Power−Good/Crowbar Blanking Supports Dynamic VID Code Changes
- Digitally Programmable 0.5 V to 1.6 V Output Supports VR11.1 Specification
- Programmable Overcurrent Protection with Programmable Latchoff Delay
- This is a Pb−Free Device

Typical Applications

- Desktop PC Power Supplies for:
  - DDR Memory
  - VRM Modules

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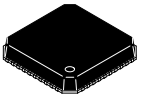
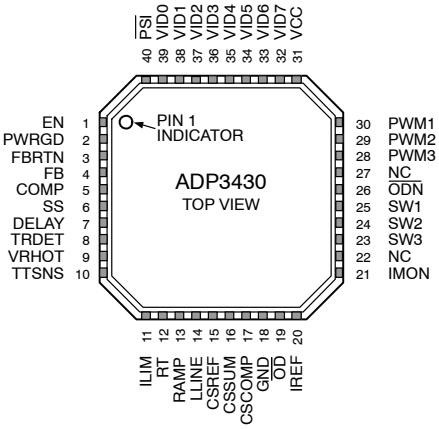
Package Name
LFCSP40
CASE Number
932AC



MARKING DIAGRAM

ADP3430	= Device Code
#	= Pb−Free Package
YY	= Date Code
ZZ	= Assembly Lot Number
CC	= Country of Origin

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
ADP3430JCPZ−RL	LFCSP40 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

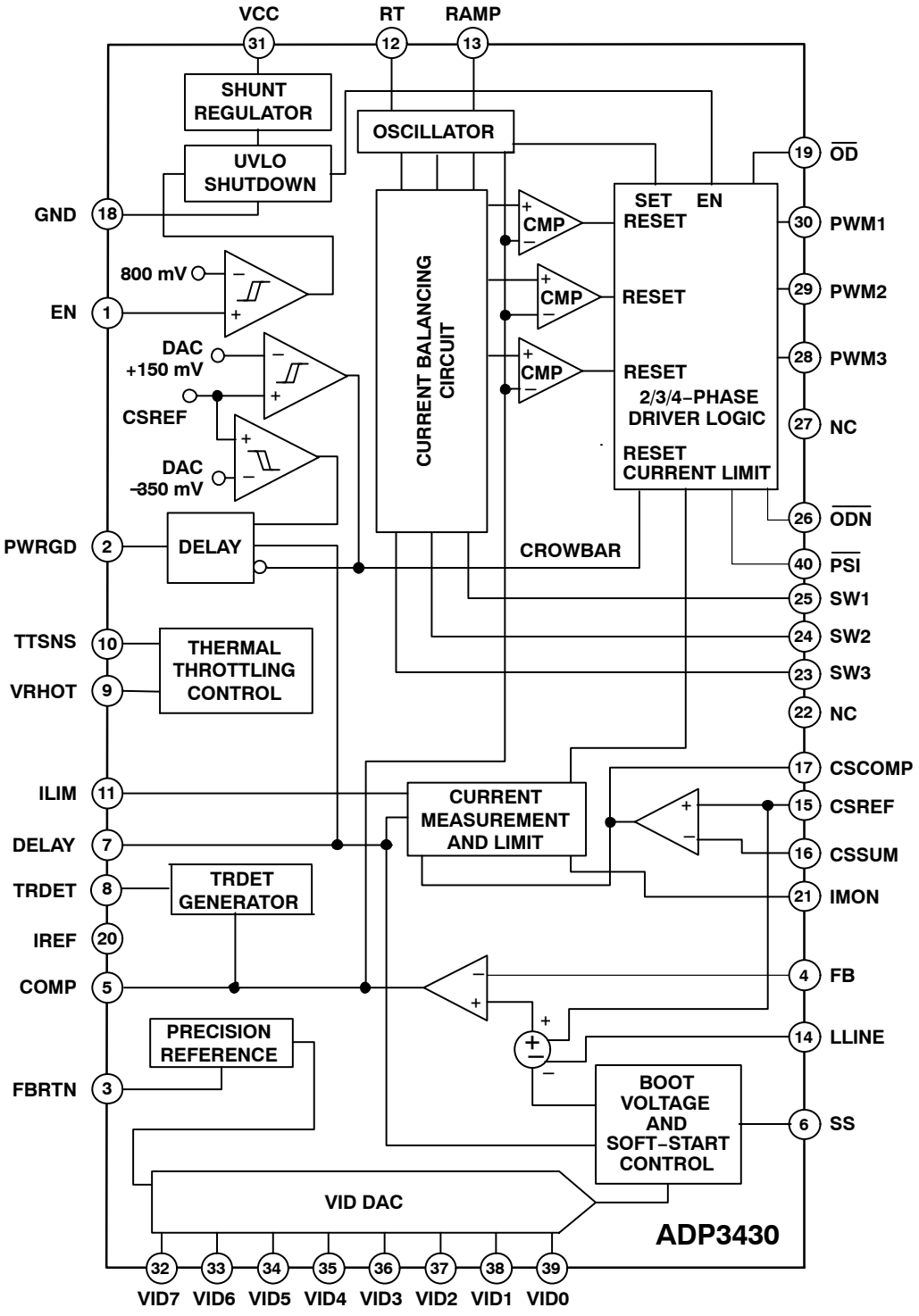


Figure 1. Simplified Block Diagram

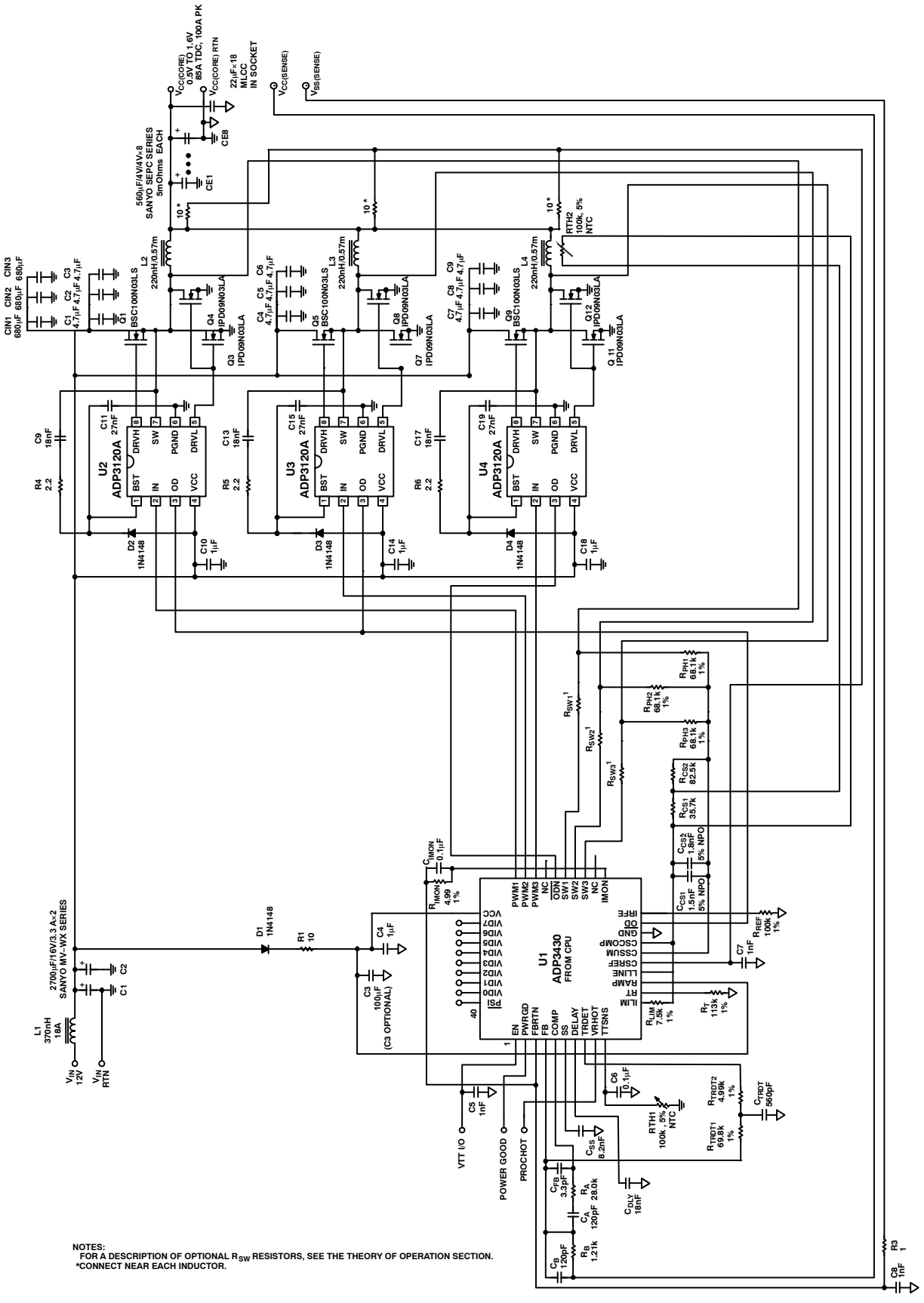


Figure 2. Application Schematic – 3–Phase Operation

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
2	PWRGD	Power−Good Output. Open−drain output that signals when the output voltage is outside of the proper operating range.
3	FBRTN	Feedback Return. VID DAC and error amplifier input for remote sensing of the output voltage.
4	FB	Feedback Input. Error amplifier reference for remote sensing of the output voltage.
5	COMP	Error Amplifier Output and Compensation Point.
6	SS	Soft−Start Delay Setting Input. An external capacitor connected between this pin and GND sets the soft−start ramp−up time.
7	DELAY	Delay Timer Setting Input. An external capacitor connected between this pin and GND sets the overcurrent latchoff delay time, boot voltage hold time, EN delay time, and PWRGD delay time.
8	TRDET	Transient Detection Output. This pin is pulled low when a load release transient is detected.
9	VRHOT	VR Hot Output. Active high open−drain output that signals when the temperature of the temperature sensor connected to TTSNS exceeds the programmed VRHOT temperature threshold.
10	TTSNS	VR Hot Thermal Throttling Sense Input. An NTC thermistor between this pin and GND is used to remotely sense the temperature at the desired thermal monitoring point.
11	ILIM	Current Sense and Limit Pin. Connecting a resistor from this pin to CSCOMP sets the internal current sensing signal for current limit and IMON.
12	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the PWM oscillator frequency. The switching frequency for each phase is up to 800 KHz.
13	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage to this pin sets the slope of the internal PWM ramp.
14	LLINE	Output Load Line Programming Input. This pin can be directly connected to CSCOMP, or it can be connected to the center point of a resistor divider between CSCOMP and CSREF. Connecting LLINE to CSREF disables positioning.
15	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power−good and crowbar functions. This pin should be connected to the common point of the output inductors.
16	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the inductor currents together to measure the total output current.
17	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time.
18	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
19	$\overline{OD}$	Output Disable Logic Output for phase 1. This pin is actively pulled low when the EN input is low or when V_{CC} is below its UVLO threshold to signal to the Driver IC that the driver high−side and low−side outputs should go low. This pin needs to connect to both 1st and 2nd phase gate drivers.
20	IREF	Current Reference Input. An external resistor from this pin to ground sets the internal reference current used to generate I_{FB}, I_{DELAY}, I_{SS}, I_{CL}, and I_{TTSNS}.
21	IMON	IMON Total Current Output Pin. A resistor/capacitor from this pin to FBRTN/VSS Sense sets the IMON signal.
22	NC	No Connection
23 to 25	SW3 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
26	$\overline{ODN}$	Output Disable Logic output for $\overline{PSI}$ Operation. This pin is pulled low when $\overline{PSI}$ is low, otherwise it functions the same as $\overline{OD}$. This pin needs to connect to the 3rd phase gate driver.
27	NC	No Connection
28 to 30	PWM3 to PMW1	Logic−Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3121. Connecting the PWM4, and/or PWM3 output to V_{CC} causes that phase to turn off, allowing the ADP3430 to operate as a 2− or 3−phase controller.
31	V_{CC}	Supply Voltage for the Device. A 340Ω resistor should be placed between the 12 V system supply and the V_{CC} pin. The internal shunt regulator maintains V_{CC} = 5.0 V.
32 to 39	VID7 to VID0	Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a Logic 0 if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.5 V to 1.6 V.
40	$\overline{PSI}$	Power State Indicator Input. Pulling this pin low places controller in lower power state operation. $\overline{PSI}$ = Low demands 2−phase operation, $\overline{PSI}$ = High for 3−phase. While $\overline{PSI}$ is an input signal which supports OTF change.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, FBRTN = GND, T_A = 0°C to 85°C unless otherwise noted) (Note 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference Current						
Reference Bias Voltage	V_{IREF}			1.5		V
Reference Bias Current	I_{IREF}	R_{IREF} = 100 kΩ	14.25	15	15.75	μA
Error Amplifier						
Output Voltage Range (Note 2)	V_{COMP}		0		4.4	V
Accuracy	V_{FB}	Relative to nominal DAC output, Referenced to FBRTN, LLINE = CSREF	–11.0		+11.0	mV
Load Line Positioning Accuracy	$V_{FB(BOOT)}$	In startup CSREF – LLINE = 80 mV, DAC = 1.51875 V	1.092 –82	1.1 –80	1.108 –78	V mV
Differential Non–linearity			–1.0		+1.0	LSB
FBRTN Current	I_{FBRTN}			125	200	μA
Output Current	I_{COMP}	FB forced to V_{OUT} – 3%		500		μA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		COMP = FB		25		V/μs
LLINE Input Voltage Range	V_{LLINE}	Relative to CSREF	–250		+250	mV
LLINE Input Bias Current	I_{LLINE}		–10		+10	nA
BOOT Voltage Hold Time	t_{BOOT}	C_{DELAY} = 10 nF		1.0		ms
VID Inputs						
Input Low Voltage	$V_{IL(VID)}$	VID(X)			0.3	V
Input High Voltage	$V_{IH(VID)}$	VID(X)	0.8			V
Input Current	$I_{IN(VID)}$			–1.0		μA
VID Transition Delay Time (Note 2)		VID code change to FB change	400			ns
No CPU Detection Turn–Off Delay Time (Note 2)		VID code change to PWM going low	5.0			μs
$\overline{\text{PSI}}$ Input						
Input Low Voltage	$V_{IL(\overline{PSI})}$				0.3	V
Input High Voltage	$V_{IH(\overline{PSI})}$		0.8			V
Input Current	$I_{IN(\overline{PSI})}$	$\overline{\text{PSI}}$ = HIGH		1.0		μA
Assertion Time	$t_{ast(\overline{PSI})}$	F_{SW} = 400 KHz, 3–phase		150		ns
De–assertion Time	$t_{deast(\overline{PSI})}$	F_{SW} = 400 KHz, 3–phase		260		ns
TRDET Output						
Low Voltage	$V_{IL(TRDET)}$	$I_{TRDET(sink)}$ = –4 mA		150	300	mV
Oscillator						
Frequency Range	f_{OSC}		0.25		4.0	MHz
Frequency Variation	f_{PHASE}	T_A = 25 °C, R_T = 87 kΩ, 3–phase T_A = 25 °C, R_T = 48 kΩ, 3–phase T_A = 25 °C, R_T = 23 kΩ, 3–phase	270	300 500 800	330	kHz
Output Voltage	V_{RT}	R_T = 87 kΩ to GND	1.9	2.0	2.1	V
RAMP Output Voltage	V_{RAMP}	RAMP – FB	–50		+50	mV
RAMP Input Current Range	I_{RAMP}		1.0		200	μA
Current Sense Amplifier						
Offset Voltage	$V_{OS(CSA)}$	CSSUM – CSREF, CSREF = 0.8V ~1.6V	–1.0		+1.0	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		–10		+10	nA
Gain Bandwidth Product	$GBW_{(CSA)}$	CSSUM = CSCOMP		10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/μs
Input Common–Mode Range		CSSUM and CSREF	0		3.5	V
Output Voltage Range			0.05		3.5	V

1. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
2. Guaranteed by design or bench characterization, not tested in production.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, FBRTN = GND, T_A = 0°C to 85°C unless otherwise noted) (Note 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Sense Amplifier cont.						
Output Current	I_{CSCOMP}			500		μA
Current Limit Latchoff Delay Time	$t_{OC(DELAY)}$	C_{DELAY} = 10 nF		8.0		ms
Current Balance Amplifier						
Common−Mode Range (Note 2)	$V_{SW(X)CM}$		−600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0 V	10	17	26	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0 V	8	12	20	μA
Input Current Matching	$\Delta I_{SW(X)}$	SW(X) = 0 V	−4.0		+4.0	%
IMON Output						
Clamp Voltage			1.0		1.15	V
Current Gain		$(IMON_{CURRENT})$ / $(ILIMIT_{CURRENT})$, R_{ILIM} = R_{IMON} = 8.0 kΩ, $\overline{PSI}$ = HIGH	9.0	10	11	
Output Current					800	μA
Offset		V_{CSREF} − V_{ILIMIT}		1.2		mV
Current Limit Comparator						
Current Limit Threshold Current	I_{CL}	4/3 x I_{IREF}	17.7	20	22.3	μA
Delay Timer						
Normal Mode Output Current	I_{DELAY}	I_{DELAY} = I_{IREF}	12	15	18	μA
Output Current in Current Limit	$I_{DELAY(CL)}$	$I_{DELAY(CL)}$ = 0.25 x I_{IREF}	3.0	3.75	4.5	μA
Threshold Voltage	$V_{DELAY(TH)}$		1.6	1.7	1.8	V
Soft−Start						
Output Current	I_{SS}	During startup	13.5	17.5	21.5	μA
Soft−Start slew rate	dv/dt	Css = 8.2 nF		2.0		mV/μs
Enable Input						
Input Low Voltage	$V_{IL(EN)}$				300	mV
Input High Voltage	$V_{IH(EN)}$		800			mV
Input Current	$I_{IN(EN)}$			−1.0		μA
Delay Time	$t_{DELAY(EN)}$	EN > 800 mV, C_{DELAY} = 10 nF		1.0		ms
$\overline{OD}$ and $\overline{ODN}$ Output						
Output Low Voltage	$V_{OL(\overline{OD})}$ $V_{OL(ODN)}$	$I_{\overline{OD}(SINK)}$ = −400 μA $I_{ODN(SINK)}$ = −400 μA		160	500	mV
Output High Voltage	$V_{OH(\overline{OD})}$ $V_{OH(ODN)}$	$I_{\overline{OD}(SOURCE)}$ = 400 μA, $I_{ODN\ (SOURCE)}$ = 400 μA	4.0	5.0		V
$\overline{OD}$ Pull−Down Resistor				60		kΩ
Thermal Throttling Control						
TTSNS Voltage Range		Internally limited	0		5.0	V
TTSNS Bias Current			−133	−123	−113	μA
TTSNS VRHOT Threshold Voltage			715	760	805	mV
TTSNS Hysteresis				50		mV
VRHOT Output Low Voltage	$V_{OL(VRHOT)}$	$I_{VRHOT(SINK)}$ = −4 mA, TTSNS = 5 V		150	300	mV
Power−Good Comparator						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal DAC output	−400	−350	−300	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to nominal DAC output	100	150	200	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = −4 mA		150	300	mV
Power−Good Delay Time During Soft−Start		C_{DELAY} = 10 nF		1.0		ms

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ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, FBRTN = GND, T_A = 0°C to 85°C unless otherwise noted) (Note 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power−Good Comparator cont.						
Crowbar Trip Point	$V_{CB(CSREF)}$	Relative to nominal DAC output	100	150	200	mV
Crowbar Reset Threshold		Relative to FBRTN	305	360	415	mV
PWM Outputs						
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = −400 μA		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400 μA	4.0	5.0		V
Supply						
V_{CC}	V_{CC}	V_{SYSTEM} = 12 V, R_{SHUNT} = 340 Ω	4.65	5.0	5.55	V
DC Supply Current	I_{VCC}	V_{SYSTEM} = 13.2 V, R_{SHUNT} = 340 Ω			25	mA
Shunt Turn−On Current				6.5		mA
Shunt Turn−On Threshold Voltage	V_{SYSTEM}	V_{SYSTEM} Rising		6.0		V
Shunt Turn−Off Voltage		V_{SYSTEM} Falling		4.1		V

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2. Guaranteed by design or bench characterization, not tested in production.

TYPICAL CHARACTERISTICS

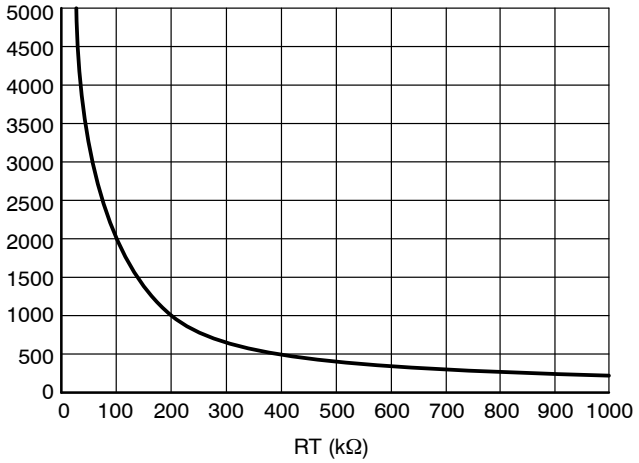


Figure 3. Oscillator Frequency vs. RT

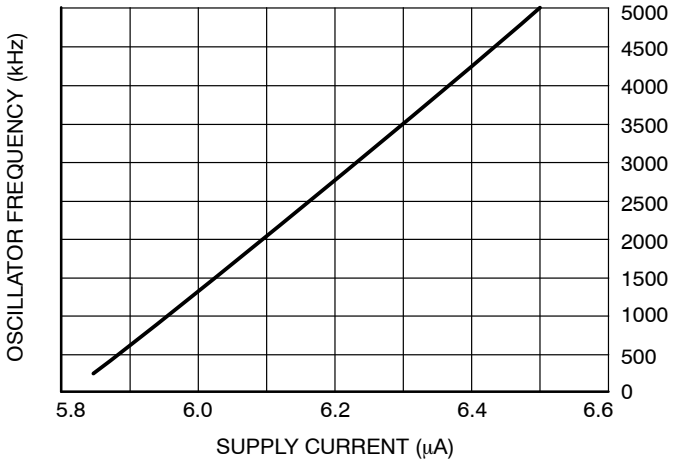


Figure 4. Oscillator Frequency vs. Supply Current

Theory of Operation

The ADP3430 combines a multi−mode, fixed frequency PWM control with multiphase logic outputs for use in 2− or 3−phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with Intel 8−bit VRD/VRM 11.1 and compatible CPUs. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single−phase converter places high thermal demands on the components in the system, such as the inductors and MOSFETs.

The multi−mode control of the ADP3430 ensures a stable, high performance topology for the following:

- Balancing currents and thermals between phases for both static and dynamic operation
- High speed response at the lowest possible switching frequency and output decoupling
- FEPWM and TRDET functions for improved load step and load release transient response
- Minimizing thermal switching losses by using lower frequency operation
- Functions of with and without tight load line regulation and accuracy
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

Startup Sequence

The ADP3430 follows the VR11.1 startup sequence shown in Figure 5. After both the EN and UVLO conditions are met, the DELAY pin goes through one cycle (TD1). After this cycle, the internal oscillator is enabled. The first four clock cycles are blanked from the PWM outputs and used for phase detection as explained in the Phase Detection Sequence section. Then, the soft−start ramp is enabled (TD2), and the output comes up to the boot voltage of 1.1 V. The boot hold time is determined by the DELAY pin as it goes through a third cycle (TD3). During TD3, the processor VID pins settle to the required VID code. When TD3 is over, the ADP3430 reads the VID inputs and soft−starts either up or down to the final VID voltage (TD4).When TD4 and the PWRGD masking time (equal to VID OTF masking) is completed, a third ramp on the DELAY pin sets the PWRGD blanking (TD5).

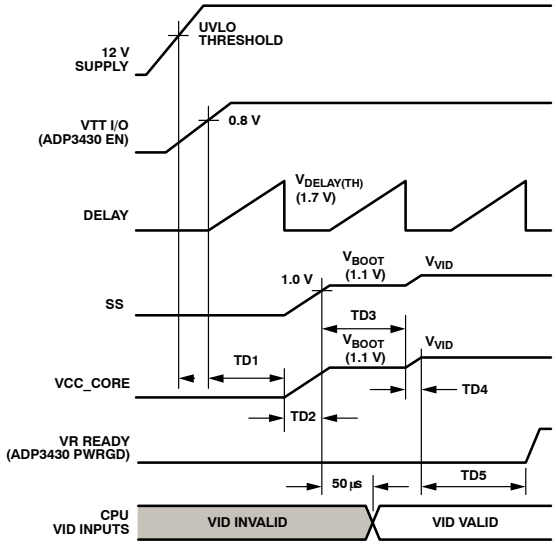


Figure 5. System Startup Sequence

Phase Number Configuration

The $\overline{\text{PSI}}$ pin is used as an input to determine the operating phase number (2− or 3−phase), depending on power state of the load. If this pin is set as low, the controller knows the load is in a low power state and it pulls the $\overline{\text{ODN}}$ signal low, which can be used to disable phase 3 (2−phase operation) for increased efficiency. When $\overline{\text{PSI}}$ pin is set as high, then it demands 3−phase operation. Please note that the $\overline{\text{PSI}}$ OTF change is also supported.

The PWM outputs are logic−level devices intended for driving fast response external gate drivers such as the ADP3121 and ADP3122. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one PWM output can be on at the same time to allow overlapping phases.

Master Clock Frequency

The clock frequency of the ADP3430 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. For both 2−Phase and 3−Phase operations, the frequency per phase is equal to 1/6 of the clock frequency.

Output Voltage Differential Sensing

The ADP3430 combines differential sensing with a high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst−case specification of ± 8.0 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB is connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN is connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 125 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

Output Current Sensing

The ADP3430 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning versus load current (when this function is required), for the I_{MON} output, and for current limit detection. Sensing the load current at the output gives the total real−time current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low−side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost.
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the average output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the input summing resistor.

An additional resistor divider connected between CSREF and CSCOMP (with the midpoint connected to LLINE) can be used to set the load line required by the microprocessor. The current information is then given as CSREF − LLINE. This difference signal is used internally to offset the VID DAC for voltage positioning. The difference between CSREF and CSCOMP is then used as a differential input for the current limit comparator. This allows the load line to be set independently of the current limit threshold. In the event that the current limit threshold and load line are not independent, the resistor divider between CSREF and CSCOMP can be removed and the CSCOMP pin can be directly connected to LLINE. To disable voltage positioning entirely (that is, no load line) connect LLINE to CSREF.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

Current Control Mode and Thermal Balance

The ADP3430 has individual inputs (SW1 to SW4) for each phase that are used for monitoring the current of each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning as described in the Load Line Setting section.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed−forward control for changes in the supply. A resistor connected from the power input voltage to the RAMP pin determines the slope of the internal PWM ramp.

External resistors can be placed in series with individual phases to create an intentional current imbalance if desired, such as when one phase has better cooling and can support higher currents. Resistor R_{SW1} through R_{SW4} can be used for adjusting thermal balance. It is best to have the ability to add these resistors during the initial design, therefore, ensure that placeholders are provided in the layout.

To increase the current in any given phase, enlarge R_{SW} for that phase (make $R_{SW} = 0$ for the hottest phase and do not change it during balancing). Increasing R_{SW} by 1 kΩ can make an increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

Voltage Control Mode

A high gain, bandwidth voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed.

The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps. The main loop compensation is incorporated into the feedback network between FB and COMP.

Fast Enhanced Transient Modes

The ADP3430 incorporates enhanced transient response for both load steps and load release. For load steps, it senses the error amp to determine if a load step has occurred and sequences the proper number of phases on to ramp up the output current.

For load release, it also senses the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the feedback for optimal positioning especially during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing stress on the components such as the input filter and MOSFETs.

Delay Timer

The delay times for the startup timing sequence are set with a capacitor from the DELAY pin to ground. In UVLO, or when EN is logic low, the DELAY pin is held at ground. After the UVLO and EN signals are asserted, the first delay time (TD1 in Figure 5) is initiated. A 15 μA current flows out of the DELAY pin to charge C_{DLY}. A comparator monitors the DELAY voltage with a threshold of 1.7 V. The delay time is therefore set by the 15 μA charging a capacitor from 0 V

to 1.7 V. This DELAY pin is used for multiple delay timings (TD1, TD3, and TD5) during the startup sequence. Also, DELAY is used for timing the current limit latchoff, as explained in the Current Limit, Short−Circuit, and Latchoff Protection section.

Soft−Start

The soft−start times for the output voltage are set with a capacitor from the SS pin to ground. After TD1 and the phase detection cycle have been completed, the SS time (TD2 in Figure 5) starts. The SS pin is disconnected from GND, and the capacitor is charged up to the 1.1 V boot voltage by the SS amplifier, which has a limited output current of 15 μA. The voltage at the FB pin follows the ramping voltage on the SS pin, limiting the inrush current during startup. The soft−start time depends on the value of the boot voltage and C_{SS}.

Once the SS voltage is within 100 mV of the boot voltage, the boot voltage delay time (TD3 in Figure 5) is started. The end of the boot voltage delay time signals the beginning of the second soft−start time (TD4 in Figure 5). The SS voltage now changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using the SS amplifier with the limited 15 μA output current. The voltage of the FB pin follows the ramping voltage of the SS pin, limiting the inrush current during the transition from the boot voltage to the final DAC voltage. The second soft−start time depends on the boot voltage, the programmed VID DAC voltage, and C_{SS}.

If EN is taken low or if V_{CC} drops below UVLO, DELAY and SS are reset to ground to be ready for another soft−start cycle. Figure 6 shows typical startup waveforms for the ADP3430.

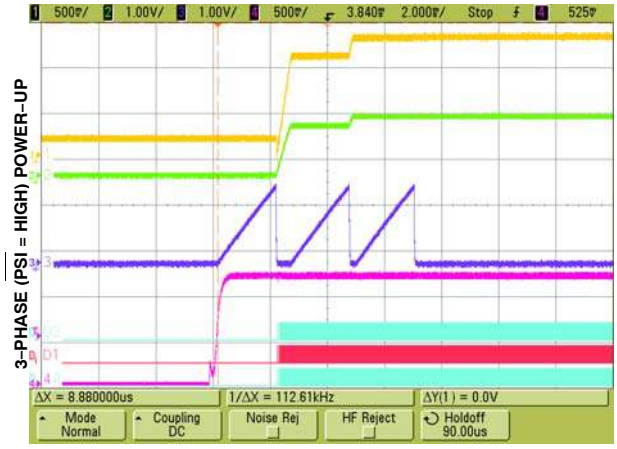


Figure 6. Typical Startup Waveform
1−Vo, 2−SS, 3−DELAY, 4−EN, D0−D3−PWM1~3

Current Limit, Short−Circuit, and Latchoff Protection

The ADP3430 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the I_{LIM} pin to CSCOMP. During operation, the voltage on I_{LIM} is equal to the voltage on CSREF. The current through the external resistor connected between I_{LIM} and CSCOMP is then compared to the internal current limit current I_{cl}. If the current generated through this register into the I_{LIM} pin(I_{LIM}) exceeds the internal current limit threshold current (I_{cl}), the internal current limit amplifier controls the internal COMP voltage to maintain the average output at the limit.

If the limit is reached and TD5 in Figure 5 has completed, a latchoff delay time starts, and the controller shuts down if the fault is not removed. The current limit delay time shares the DELAY pin timing capacitor with the startup sequence timing. However, during current limit, the DELAY pin current is reduced to 3.75 μA. A comparator monitors the DELAY voltage and shuts off the controller when the voltage reaches 1.7 V. Therefore, the current limit latchoff delay time is set by the current of 3.75 μA, charging the delay capacitor from 0 V to 1.7 V. This delay is four times longer than the delay time during the startup sequence.

The current limit delay time starts only after the TD5 is complete. If there is a current limit during startup, the ADP3430 goes through TD1 to TD5, and then starts the latchoff time. Because the controller continues to cycle the phases during the latchoff delay time, the controller returns to normal operation and the DELAY capacitor is reset to GND if the short is removed before the 1.7 V threshold is reached.

For the same R_t value, the current limit for 2−phase operation ($\overline{PSI}$ = Low) is 2/3 of that of 3−phase ($\overline{PSI}$ = High).

The latchoff function can be reset by either removing and reapplying the supply voltage to the ADP3430, or by toggling the EN pin low for a short time. To disable the short circuit latchoff function, an external resistor should be placed in parallel with C_{DLY}. This prevents the DELAY capacitor from charging up to the 1.7 V threshold. The addition of this resistor causes a slight increase in the delay times.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low−side MOSFETs through the current balance circuitry. An inherent per−phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage. Typical overcurrent latchoff waveforms are shown in Figure 6.

Output Current Monitor

The I_{MON} pin is used to output an analog voltage representing the total output current being delivered to the load. It outputs an accurate current that is directly proportional to the current set by the I_{LIM} resistor. This current is then run through a parallel RC connected from the I_{MON} pin to the FBRTN pin to generate an accurately scaled and filtered voltage per the VR11.1 specification. The size of the resistor is used to set the I_{MON} scaling.

If the I_{MON} and OCP are then desired to be changed based on the TDC of the CPU, the I_{LIM} resistor is the only component that needs to be changed. If the I_{MON} scaling is the only desired change, then just changing the I_{MON} resistor accomplishes this.

The I_{MON} pin also includes an active clamp to limit the I_{MON} voltage to 1.15 V MAX yet maintaining 1.0 V MIN full−scale accurate reporting.

Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output whose high level, when connected to a pullup resistor, indicates that the output voltage is within the nominal limits specified based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or if the EN pin is pulled low.

The PWRGD circuitry also incorporates an initial turn−on delay time (TD5), based on the DELAY timer. Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking−time finishing, the PWRGD pin is held low. Once the SS pin is within 100 mV of the programmed DAC voltage, the capacitor on the DELAY pin begins to charge. A comparator monitors the DELAY voltage and enables PWRGD when the voltage reaches 1.7 V. The PWRGD delay time is, therefore, set by a current of 15 μA, charging a capacitor from 0 V to 1.7 V.

High Frequency Current Balance

Randomization for phases is implemented, in order to prevent high frequency current/thermal imbalance due to load and voltage regulator synchronization.

Power State Indicator

The $\overline{\text{PSI}}$ pin is used as an input to determine the operating power state of the load. If this pin is pulled low, the controller knows the load is in a low power state and it takes the $\overline{\text{ODN}}$ signal low, which can be used to disable phases for increased efficiency. $\overline{\text{PSI}}$ supports OTF change.

One additional feature of the ADP3430 is the internal current limit threshold is changed when $\overline{\text{PSI}}$ is pulled low. The current limit threshold is reduced by 2/3 such that the same per phase average current limit is maintained to protect the components in the system.

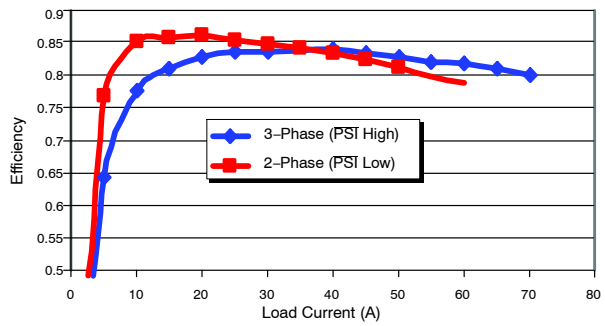


Figure 7. Efficiency Comparison ($\overline{\text{PSI}}$ High vs. Low) (Vin = 12 V, Vo = 1.51875 V, Fs = 375 kHz)

Output Crowbar

To protect the load and output components of the supply, the PWM outputs are driven low, which turns on the low−side MOSFETs when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 375 mV.

Turning on the low−side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high−side MOSFET, this action current limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

Output Enable and UVLO

For the ADP3430 to begin switching, the input supply current to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.8 V threshold. This initiates a system startup sequence. If either UVLO or EN is less than their respective thresholds, the ADP3430 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and the forces PWRGD and $\overline{\text{OD}}$ signals low.

In the application circuit, the $\overline{\text{OD}}$ pin should be connected to the $\overline{\text{OD}}$ input of the external driver for the phase that is always on (phase 1 and 2) while the $\overline{\text{ODN}}$ pin should be connected to the $\overline{\text{OD}}$ input on the external drivers of the phase 3. Grounding $\overline{\text{OD}}$ and $\overline{\text{ODN}}$ disable the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

Thermal Monitoring

The ADP3430 includes a thermal monitoring circuit to detect when a point on the VR has exceeded a user−defined temperature. The thermal monitoring circuit requires an NTC thermistor to be placed between TTSNS and GND.

A fixed current of 123 μA is sourced out of the TTSNS pin and into the thermistor. The current source is internally limited to 5.0 V. An internal circuit compares the TTSNS voltage to a 0.81 V threshold, and outputs an open−drain signal at the VRHOT output. Once the voltage on the TTSNS pin drops below its threshold, the open−drain output asserts high to signal the system that an overtemperature event has occurred. Because the TTSNS voltage changes slowly with respect to time, 55 mV of hysteresis is built into this comparator. The thermal monitoring circuitry does not depend on EN and is active when UVLO is above its threshold. When UVLO is below its threshold, VRHOT is forced low.

VR11.1 VID Codes

OUTPUT(V)	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
OFF	0	0	0	0	0	0	0	0
OFF	0	0	0	0	0	0	0	1
1.60000	0	0	0	0	0	0	1	0
1.59375	0	0	0	0	0	0	1	1
1.58750	0	0	0	0	0	1	0	0
1.58125	0	0	0	0	0	1	0	1
1.57500	0	0	0	0	0	1	1	0
1.56875	0	0	0	0	0	1	1	1
1.56250	0	0	0	0	1	0	0	0
1.55625	0	0	0	0	1	0	0	1
1.55000	0	0	0	0	1	0	1	0
1.54375	0	0	0	0	1	0	1	1
1.53750	0	0	0	0	1	1	0	0
1.53125	0	0	0	0	1	1	0	1
1.52500	0	0	0	0	1	1	1	0
1.51875	0	0	0	0	1	1	1	1
1.51250	0	0	0	1	0	0	0	0
1.50625	0	0	0	1	0	0	0	1
1.50000	0	0	0	1	0	0	1	0
1.49375	0	0	0	1	0	0	1	1
1.48750	0	0	0	1	0	1	0	0
1.48125	0	0	0	1	0	1	0	1
1.47500	0	0	0	1	0	1	1	0
1.46875	0	0	0	1	0	1	1	1
1.46250	0	0	0	1	1	0	0	0
1.45625	0	0	0	1	1	0	0	1
1.45000	0	0	0	1	1	0	1	0
1.44375	0	0	0	1	1	0	1	1
1.43750	0	0	0	1	1	1	0	0
1.43125	0	0	0	1	1	1	0	1
1.42500	0	0	0	1	1	1	1	0
1.41875	0	0	0	1	1	1	1	1
1.41250	0	0	1	0	0	0	0	0
1.40625	0	0	1	0	0	0	0	1
1.40000	0	0	1	0	0	0	1	0
1.39375	0	0	1	0	0	0	1	1
1.38750	0	0	1	0	0	1	0	0
1.38125	0	0	1	0	0	1	0	1
1.37500	0	0	1	0	0	1	1	0
1.36875	0	0	1	0	0	1	1	1
1.36250	0	0	1	0	1	0	0	0
1.35625	0	0	1	0	1	0	0	1
1.35000	0	0	1	0	1	0	1	0
1.34375	0	0	1	0	1	0	1	1
1.33750	0	0	1	0	1	1	0	0
1.33125	0	0	1	0	1	1	0	1
1.32500	0	0	1	0	1	1	1	0

VR11.1 VID Codes

OUTPUT(V)	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.31875	0	0	1	0	1	1	1	1
1.31250	0	0	1	1	0	0	0	0
1.30625	0	0	1	1	0	0	0	1
1.30000	0	0	1	1	0	0	1	0
1.29375	0	0	1	1	0	0	1	1
1.28750	0	0	1	1	0	1	0	0
1.28125	0	0	1	1	0	1	0	1
1.27500	0	0	1	1	0	1	1	0
1.26875	0	0	1	1	0	1	1	1
1.26250	0	0	1	1	1	0	0	0
1.25625	0	0	1	1	1	0	0	1
1.25000	0	0	1	1	1	0	1	0
1.24375	0	0	1	1	1	0	1	1
1.23750	0	0	1	1	1	1	0	0
1.23125	0	0	1	1	1	1	0	1
1.22500	0	0	1	1	1	1	1	0
1.21875	0	0	1	1	1	1	1	1
1.21250	0	1	0	0	0	0	0	0
1.20625	0	1	0	0	0	0	0	1
1.20000	0	1	0	0	0	0	1	0
1.19375	0	1	0	0	0	0	1	1
1.18750	0	1	0	0	0	1	0	0
1.18125	0	1	0	0	0	1	0	1
1.17500	0	1	0	0	0	1	1	0
1.16875	0	1	0	0	0	1	1	1
1.16250	0	1	0	0	1	0	0	0
1.15625	0	1	0	0	1	0	0	1
1.15000	0	1	0	0	1	0	1	0
1.14375	0	1	0	0	1	0	1	1
1.13750	0	1	0	0	1	1	0	0
1.13125	0	1	0	0	1	1	0	1
1.12500	0	1	0	0	1	1	1	0
1.11875	0	1	0	0	1	1	1	1
1.11250	0	1	0	1	0	0	0	0
1.10625	0	1	0	1	0	0	0	1
1.10000	0	1	0	1	0	0	1	0
1.09375	0	1	0	1	0	0	1	1
1.08750	0	1	0	1	0	1	0	0
1.08125	0	1	0	1	0	1	0	1
1.07500	0	1	0	1	0	1	1	0
1.06875	0	1	0	1	0	1	1	1
1.06250	0	1	0	1	1	0	0	0
1.05625	0	1	0	1	1	0	0	1
1.05000	0	1	0	1	1	0	1	0
1.04375	0	1	0	1	1	0	1	1
1.03750	0	1	0	1	1	1	0	0
1.03125	0	1	0	1	1	1	0	1

VR11.1 VID Codes

OUTPUT(V)	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.02500	0	1	0	1	1	1	1	0
1.01875	0	1	0	1	1	1	1	1
1.01250	0	1	1	0	0	0	0	0
1.00625	0	1	1	0	0	0	0	1
1.00000	0	1	1	0	0	0	1	0
0.99375	0	1	1	0	0	0	1	1
0.98750	0	1	1	0	0	1	0	0
0.98125	0	1	1	0	0	1	0	1
0.97500	0	1	1	0	0	1	1	0
0.96875	0	1	1	0	0	1	1	1
0.96250	0	1	1	0	1	0	0	0
0.95625	0	1	1	0	1	0	0	1
0.95000	0	1	1	0	1	0	1	0
0.94375	0	1	1	0	1	0	1	1
0.93750	0	1	1	0	1	1	0	0
0.93125	0	1	1	0	1	1	0	1
0.92500	0	1	1	0	1	1	1	0
0.91875	0	1	1	0	1	1	1	1
0.91250	0	1	1	1	0	0	0	0
0.90625	0	1	1	1	0	0	0	1
0.90000	0	1	1	1	0	0	1	0
0.89375	0	1	1	1	0	0	1	1
0.88750	0	1	1	1	0	1	0	0
0.88125	0	1	1	1	0	1	0	1
0.87500	0	1	1	1	0	1	1	0
0.86875	0	1	1	1	0	1	1	1
0.86250	0	1	1	1	1	0	0	0
0.85625	0	1	1	1	1	0	0	1
0.85000	0	1	1	1	1	0	1	0
0.84375	0	1	1	1	1	0	1	1
0.83750	0	1	1	1	1	1	0	0
0.83125	0	1	1	1	1	1	0	1
0.82500	0	1	1	1	1	1	1	0
0.81875	0	1	1	1	1	1	1	1
0.81250	1	0	0	0	0	0	0	0
0.80625	1	0	0	0	0	0	0	1
0.80000	1	0	0	0	0	0	1	0
0.79375	1	0	0	0	0	0	1	1
0.78750	1	0	0	0	0	1	0	0
0.78125	1	0	0	0	0	1	0	1
0.77500	1	0	0	0	0	1	1	0
0.76875	1	0	0	0	0	1	1	1
0.76250	1	0	0	0	1	0	0	0
0.75625	1	0	0	0	1	0	0	1
0.75000	1	0	0	0	1	0	1	0
0.74375	1	0	0	0	1	0	1	1
0.73750	1	0	0	0	1	1	0	0

VR11.1 VID Codes

OUTPUT(V)	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
0.73125	1	0	0	0	1	1	0	1
0.72500	1	0	0	0	1	1	1	0
0.71875	1	0	0	0	1	1	1	1
0.71250	1	0	0	1	0	0	0	0
0.70625	1	0	0	1	0	0	0	1
0.70000	1	0	0	1	0	0	1	0
0.69375	1	0	0	1	0	0	1	1
0.68750	1	0	0	1	0	1	0	0
0.68125	1	0	0	1	0	1	0	1
0.67500	1	0	0	1	0	1	1	0
0.66875	1	0	0	1	0	1	1	1
0.66250	1	0	0	1	1	0	0	0
0.65625	1	0	0	1	1	0	0	1
0.65000	1	0	0	1	1	0	1	0
0.64375	1	0	0	1	1	0	1	1
0.63750	1	0	0	1	1	1	0	0
0.63125	1	0	0	1	1	1	0	1
0.62500	1	0	0	1	1	1	1	0
0.61875	1	0	0	1	1	1	1	1
0.61250	1	0	1	0	0	0	0	0
0.60625	1	0	1	0	0	0	0	1
0.60000	1	0	1	0	0	0	1	0
0.59375	1	0	1	0	0	0	1	1
0.58750	1	0	1	0	0	1	0	0
0.58125	1	0	1	0	0	1	0	1
0.57500	1	0	1	0	0	1	1	0
0.56875	1	0	1	0	0	1	1	1
0.56250	1	0	1	0	1	0	0	0
0.55625	1	0	1	0	1	0	0	1
0.55000	1	0	1	0	1	0	1	0
0.54375	1	0	1	0	1	0	1	1
0.53750	1	0	1	0	1	1	0	0
0.53125	1	0	1	0	1	1	0	1
0.52500	1	0	1	0	1	1	1	0
0.51875	1	0	1	0	1	1	1	1
0.51250	1	0	1	1	0	0	0	0
0.50625	1	0	1	1	0	0	0	1
0.50000	1	0	1	1	0	0	1	0
OFF	1	1	1	1	1	1	1	0
OFF	1	1	1	1	1	1	1	1

Application Information

The design parameters for a typical Intel VRD 11.1 compliant CPU application are as follows:

- Input voltage (V_{IN}) = 12 V
- VID setting voltage (V_{VID}) = 1.51875 V
- Duty cycle (D) = 0.1266
- Nominal output voltage at no load (V_{ONL}) = 1.5 V
- Maximum output current (I_O) = 69 A
- Maximum output current step (ΔI_O) = 56 A
- Maximum output current slew rate (S_R) = 50 A/μs
- Number of phases (n) = 3
- Switching frequency per phase (f_{sw}) = 300 kHz

Setting the Clock Frequency

The ADP3430 uses a fixed frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency determines the switching frequency per phase, which relates directly to switching losses as well as the sizes of the inductors, the input capacitors, and output capacitors. A clock frequency of 1.8 MHz sets the switching frequency (f_{sw}) of each phase to 300 kHz, which represents a practical trade−off between the switching losses and the sizes of the output filter components. Figure 3 shows that to achieve a 1.8 MHz oscillator frequency, the correct value for R_T is 97 kΩ. Alternatively, the value for R_T can be calculated using:

$$R_T = \frac{1}{f_{osc} \times 5.3\ pF} + 4.4\ k\Omega$$
$$f_{sw} = \frac{f_{osc}}{6} \quad \text{(eq. 1)}$$

where 5.3 pF is the internal IC component values. For good initial accuracy and frequency stability, a 1% resistor is recommended.

Soft−Start Delay Time

The value of C_{SS} sets the soft−start time. The ramp is generated with a 15 μA internal current source. The value for C_{SS} can be found using:

$$C_{SS} = 15\ \mu A \times \frac{TD2}{V_{BOOT}} \quad \text{(eq. 2)}$$

where TD2 is the desired soft−start time, and V_{BOOT} is internally set to 1.0 V.

Assuming a desired TD2 time of 2.5 ms, C_{SS} is 37.5 nF. The closest standard value for C_{SS} is 39 nF. Although C_{SS} also controls the time delay for TD4 (determined by the final VID voltage), the minimum specification for TD4 is 0 ns. This means that as long as the TD2 time requirement is met, TD4 is within the specification.

Current Limit Latchoff Delay Times

The startup and current limit delay times are determined by the capacitor connected to the DELAY pin. The first step is to set C_{DLY} for the TD1, TD3, and TD5 delay times (see Figure 5). The DELAY ramp (I_{DELAY}) is generated using a 15 μA internal current source.

The value for C_{DLY} can be approximated using:

$$C_{DLY} = I_{DELAY} \times \frac{TD(x)}{V_{DELAY(TH)}} \quad \text{(eq. 3)}$$

where TD(x) is the desired delay time for TD1, TD3, and TD5. The DELAY threshold voltage ($V_{DELAY(TH)}$) is given as 1.7 V. In this example, 2 ms is chosen for all three delay times, which meets Intel specifications. Solving for C_{DLY} gives a value of 17.6 nF. The closest standard value for C_{DLY} is 18 nF.

When the ADP3430 enters current limit, the internal current source changes from 15 μA to 3.75 μA. This makes the latchoff delay time four times longer than the startup delay time. Longer latchoff delay times can be achieved by placing a resistor in parallel with C_{DLY}.

Inductor Selection

The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs. However, using smaller inductors allows the converter to meet a specified peak−to−peak transient deviation with less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but more output capacitance is required to meet the same peak−to−peak transient deviation.

In any multiphase converter, a practical value for the peak−to−peak inductor ripple current is less than 50% of the maximum dc current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak−to−peak ripple current in the inductor.

$$I_R = \frac{V_{VID} \times (1 - D)}{f_{SW} \times L} \quad \text{(eq. 4)}$$

As a typical design, the I_R should be no bigger than 45% of the DC current, thus it needs to satisfy:

$$\frac{V_{VID} \times (1 - D)}{f_{SW} \times L} \le 0.45 \times \frac{I_{max}}{n} \quad \text{(eq. 5)}$$

Solving Equation 5 for for above example, it has:

$$L \ge \frac{1.51875\ V \times (1 - 0.1266)}{300\ kHz \times 0.45 \times \frac{69\ A}{3}} = 430\ nH$$

For this example, choosing a 450 nH inductor is a good starting point and gives a calculated ripple current of 9.8 A. The inductor should not saturate at the peak current of 28 A and should be able to handle the sum of the power dissipation caused by the average current of 23 A in the winding and core loss.

Another important factor in the inductor design is the dc resistance (DCR), which is used for measuring the phase currents. A large DCR can cause excessive power losses, though too small a value can lead to increased measurement error for current limit and current monitoring. The typical DCR value is about 0.5 − of 0.8 mΩ.

Designing an Inductor

Once the inductance and DCR are known, the next step is to either design an inductor or to find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to control the accuracy of the system. Reasonable tolerances most manufacturers can meet are 15% inductance and 7% DCR at room temperature. The first decision in designing the inductor is choosing the core material. Several possibilities for providing low core loss at high frequencies include the powder cores (from Micrometals, Inc., for example, or Kool Mu® from Magnetics®) and the gapped soft ferrite cores (for example, 3F3 or 3F4 from Philips®). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

The best choice for a core geometry is a closed−loop type such as a potentiometer core (PQ, U, or E core) or toroid. A good compromise between price and performance is a core with a toroidal shape.

Many useful magnetics design references are available for quickly designing a power inductor, such as:

- Intusoft Magnetic Designer Software
- Designing Magnetic Components for High Frequency DC to DC Converters, by William T. McLyman, Kg Magnetics, Inc., ISBN 1883107008

Selecting a Standard Inductor

The following power inductor manufacturers can provide design consultation and deliver power inductors optimized for high power applications upon request.

- Coilcraft®
- Coiltronics®
- Sumida Corporation®

Current Sense Amplifier

The output current is measured by summing the voltage across each inductor and passing the signal through a low−pass filter. This summer filter is the CS amplifier configured with resistors $R_{PH(X)}$ (summers), and R_{CS} and C_{CS} (filter). The impedance gain of the regulator is set by the following equations, where R_L is the DCR of the output inductors:

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \qquad \text{(eq. 6)}$$

The user has the flexibility to choose either R_{CS} or $R_{PH(X)}$. However, it is best to select R_{CS} equal to 110 kΩ.

In this example, $R_{PH(X)}$ is selected as 61.9 kΩ, DCR = 0.57 mΩ, use Equation 6 to solve for C_{CS}.

$$C_{CS} = \frac{450\ \text{nH}}{0.57\ \text{m}\Omega \times 110\ \text{k}\Omega} = 7.2\ \text{nF} \qquad \text{(eq. 7)}$$

It is best to have a dual location for C_{CS} in the layout so that standard values can be used in parallel to get as close to the desired value. For best accuracy, C_{CS} should be a 5% or 10% NPO capacitor. This example uses a 5% combination for C_{CS} of one 3.3 nF capacitor and one 3.9 nF capacitor in parallel.

Inductor DCR Temperature Correction

When the inductor DCR is used as the sense element and copper wire is used as the source of the DCR, the user needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage change in resistance to that of the wire, it cancels the temperature variation of the inductor DCR. Due to the non−linear nature of NTC thermistors, Resistor R_{CS1} and Resistor R_{CS2} are needed. See Figure 8 to linearize the NTC and produce the desired temperature tracking.

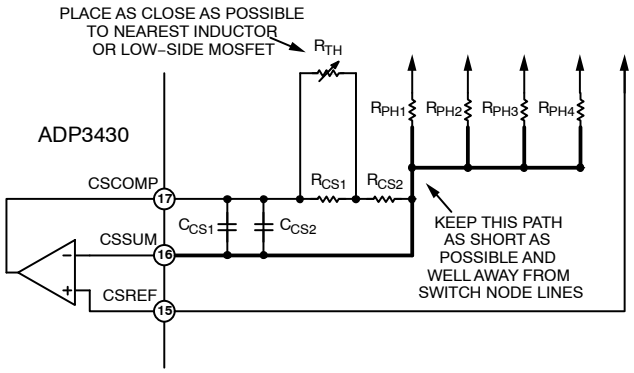


Figure 8. Temperature Compensation Circuit Values

The following procedure and equations yield values to use for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC based on type and value. Because the value is unknown, use a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.
2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. These resistance values are called A $(R_{TH(50°C)})/R_{TH(25°C)})$ and B $(R_{TH(90°C)})/R_{TH(25°C)})$. The relative value of the NTC is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage change needed, which in this example is initially 0.39%/°C. These temperatures are called r_1 $(1/(1 + TC \times (T_1 - 25°C)))$ and r_2 $(1/(1 + TC \times (T_2 - 25°C)))$, where TC = 0.0039 for copper, T_1 = 50°C, and T_2 = 90°C. From this, r_1 = 0.9112 and r_2 = 0.7978.

4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using:

$$r_{CS2} = \frac{(A - B) \times r_1 \times r_2 - A \times (1 - B) \times r_2 + B \times (1 - A) \times r_1}{A \times (1 - B) \times r_1 - B \times (1 - A) \times r_2 - (A - B)} \quad \text{(eq. 8)}$$

$$r_{CS1} = \frac{(1 - A)}{\frac{1}{1 - r_{CS2}} - \frac{A}{r_1 - r_{CS2}}} \quad \text{(eq. 9)}$$

$$r_{TH} = \frac{1}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_{CS1}}} \quad \text{(eq. 10)}$$

Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also, compute a scaling factor (k) based on the ratio of the actual thermistor value used relative to the computed one.

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad \text{(eq. 11)}$$

5. Calculate values for R_{CS1} and R_{CS2} using Equation 12 and 13.

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \quad \text{(eq. 12)}$$

$$R_{CS2} = R_{CS} \times \left((1 - k) + \left(k \times r_{CS2}\right)\right) \quad \text{(eq. 13)}$$

In this example, R_{CS} is calculated to be 114 kΩ. Look for an available 100 kΩ thermistor, 0603 size. One such thermistor is the Vishay NTHS0603N01N1003JR NTC thermistor with A = 0.3602 and B = 0.09174. From these values, r_{CS1} = 0.3795, r_{CS2} = 0.7195, and r_{TH} = 1.075.

Solving for R_{TH} yields 122.55 kΩ, so 100 kΩ is chosen, making k = 0.816. Next, find R_{CS1} and R_{CS2} to be 35.3 kΩ and 87.9 kΩ. Finally, choose the closest 1% resistor values, which yield a choice of 35.7 kΩ and 88.7 kΩ.

C_{OUT} Selection

The required output decoupling for the regulator is typically recommended by Intel for various processors and platforms. Use some simple design guidelines to determine the requirements. These guidelines are based on having both bulk capacitors and ceramic capacitors in the system.

First, select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramic capacitors is inside the socket, with 12 to 18, 1206 size being the physical limit. Other capacitors can be placed along the outer edge of the socket as well.

To determine the minimum amount of ceramic capacitance required, start with a worst−case load step occurring right after a switching cycle has stopped. The ceramic capacitance then delivers the charge to the load while the load is ramping up and until the VR has responded with the next switching cycle.

Equation 14 gives the designer a rough approximation for determining the minimum ceramic capacitance. Due to the complexity of the PCB parasitics and bulk capacitors, the actual amount of ceramic capacitance required can vary.

$$C_{Z(MIN)} \geq \frac{1}{\frac{\Delta V_{rl}}{\Delta I_O}} \times \left[\frac{1}{f_{SW}} \times \left(\frac{1}{n} - D\right) - \frac{\Delta I_O}{2 S_R}\right] \quad \text{(eq. 14)}$$

The typical ceramic capacitors consist of multiple 10 μF or 22 μF capacitors. For this example, Equation 14 yields 132 μF, so six, 22 μF ceramic capacitors suffice. A lower limit is based on meeting the capacitance for the load release for a given maximum load step (ΔI_O) and a maximum allowable overshoot.

$$C_{X(MIN)} \geq \left[\frac{\frac{1}{2} \times \frac{L}{n} \times \left(\Delta I_O\right)^2}{\Delta V_{rl} \times V_{VID}} - C_Z\right] \quad \text{(eq. 15)}$$

This example uses 6, 22 μF 1206 MLC capacitors (CZ = 132 μF), solving for the bulk capacitance yields.

$$C_{X(MIN)} \geq \left[\frac{\frac{1}{2} \times \frac{450\ nH}{3} \times (56\ A)^2}{50\ mV \times 1.51875\ V} - 132\ \mu F\right] = 2.96 mF$$

Using 7, 470 μF tantanium capacitors (KEMET) with a typical ESR of 5 mΩ each yields C_X = 3.29 μF with an RX = 0.7 mΩ.

One last check should be made to ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change.

This is tested using:

$$L_X \leq C_Z \times R_X{}^2 \times Q^2 \quad \text{(eq. 16)}$$

$$L_X \leq 132\ \mu F \times (0.7\ m\Omega)^2 \times \frac{4}{3} = 86.2\ pH$$

where Q^2 is limited to 4/3 to ensure a critically damped system.

In this example, L_X is approximately 70 pH for the 7, tantanium capacitors, which satisfies this limitation. If L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors needs to be increased, or lower ESL bulks need to be used if there is excessive undershoot during a load transition.

Power MOSFETs

For this example, the N−channel power MOSFETs have been selected for one high−side switch and two low−side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3120A dictates whether standard threshold or logic−level threshold MOSFETs must be used. With V_{GATE} ~10 V, logic−level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low−side (synchronous) MOSFETs. With the ADP3430, currents are balanced between phases, thus, the current in each low−side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, Equation 17 shows

the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O).

$$P_{SF} = (1 - D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{nI_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad \text{(eq. 17)}$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, the user can find the required $R_{DS(ON)}$ for the MOSFET. For D−PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for P_{SF} is 1 W to 1.5 W at 120°C junction temperature. Thus, for this example (69 A maximum), $R_{DS(SF)}$ (per MOSFET) < 3.2 mΩ. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C. As a result, users need to account for this when making this selection. This example uses one lower−side MOSFET at 4.4 mΩ, each at 120°C.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn−on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the non−overlap dead time of the MOSFET driver (40 ns typical for the ADP3120A). The output impedance of the driver is approximately 2 Ω, and the typical MOSFET input gate resistances are about 1 Ω to 2 Ω. Therefore, a total gate capacitance of less than 6000 pF should be adhered to. Because two MOSFETs are in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000 pF.

The high−side (main) MOSFET has to be able to handle two main power dissipation components: conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, Equation 18 provides an approximate value for the switching loss per main MOSFET, where n_{MF} is the total number of main MOSFETs.

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad \text{(eq. 18)}$$

where R_G is the total gate resistance (2 Ω for the ADP3120A and about 1 Ω for typical high speed switching MOSFETs, making R_G = 3 Ω), and C_{ISS} is the input capacitance of the main MOSFET. Adding more main MOSFETs (n_{MF}) does not help the switching loss per MOSFET because the additional gate capacitance slows switching. Use lower gate capacitance devices to reduce switching loss.

The conduction loss of the main MOSFET is given by the following, where $R_{DS(MF)}$ is the on resistance of the MOSFET:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad \text{(eq. 19)}$$

Typically, for main MOSFETs, the highest speed (low C_{ISS}) device is preferred, but these usually have higher on resistance. Select a device that meets the total power dissipation (about 1.5 W for a single D−PAK) when combining the switching and conduction losses.

For this example, an RJK0305DPB is selected as the main MOSFET (three total; n_{MF} = 3), with C_{ISS} = 1300 pF (maximum) and $R_{DS(MF)}$ = 10 mΩ (maximum at T_J = 125°C). An FDMS8670S is selected as the synchronous MOSFET (three total; n_{SF} = 8), with C_{ISS} = 4000 pF (maximum) and $R_{DS(SF)}$ = 4.4 mΩ (maximum at T_J = 125°C). The synchronous MOSFET C_{ISS} is less than 6000 pF, satisfying this requirement.

Solving for the power dissipation per MOSFET at I_O = 56 A and I_R = 9.8 A yields 1.37 W for each synchronous MOSFET and 0.975 W for each main MOSFET.

Finally, consider the power dissipation in the driver for each phase. This is best expressed as Q_G for the MOSFETs and is given by Equation 20, where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad \text{(eq. 20)}$$

Also shown is the standby dissipation factor ($I_{CC} \times V_{CC}$) of the driver. For the ADP3120A, the maximum dissipation should be less than 400 mW. In this example, with I_{CC} = 7 mA, Q_{GMF} = 15 nC, and Q_{GSF} = 73 nC, there is 242 mW in each driver, which is below the 400 mW dissipation limit. See the ADP3120A data sheet for more details.

Ramp Resistor Selection

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Equation 21 is used for determining the optimum value.

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad \text{(eq. 21)}$$

$$R_R = \frac{0.5 \times 450\ \text{nH}}{3 \times 5 \times 4\ \text{m}\Omega \times 5\ \text{pF}} = 750\ \text{k}\Omega$$

where:
A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low−side MOSFET on resistance.
C_R is the internal ramp capacitor value.

Another requirement also needs to be satisfied:
$I_{RAMP} < I_{CLAMP}$ (200 μA/3), thus:

$$R_R \geq \frac{A_R \times (V_{CC} - V_{VID})}{I_{CLAMP}} = \frac{0.5 \times (12 - 1.51875)\ V}{66.7\ \mu A} = 79\ k\Omega \quad \text{(eq. 22)}$$

Since above R_R value is bigger than 79 kΩ, it keeps the value of 750 KΩ.

The internal ramp voltage magnitude can be calculated by using:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad \text{(eq. 23)}$$

$$V_R = \frac{0.5 \times (1 - 0.1266) \times 1.51875\ V}{750\ k\Omega \times 5\ pF \times 300\ kHz} = 590\ mV$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and noise rejection improves, but transient degrades. Likewise, if the ramp is made smaller, transient response improves at the sacrifice of noise rejection and stability.

The factor of 3 in the denominator of Equation 21 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

Comp Pin Ramp

A ramp signal on the COMP pin is due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad \text{(eq. 24)}$$

In this example, the overall ramp signal is 0.862 V. If the ramp size is smaller than 0.5 V, increase the ramp size to be at least 0.5 V by decreasing the ramp resistor for noise immunity.

Current Limit Setpoint

To select the current limit setpoint, first find the resistor value for R_{LIM}. The current limit threshold for the ADP3430 is set with a constant current source ($I_{ILIM} = 4/3 * I_{REF}$) flowing out of the I_{LIM} pin, which sets up a voltage (V_{LIM}) across R_{LIM}. Thus, increasing R_{LIM} now increases the current limit. R_{LIM} can be found using:

$$R_{LIM} = \frac{V_{LIM}}{I_{ILIM}} = \frac{I_{LIM} \times R_{CS} \times DCR}{\frac{4}{3} \times V_{REF} \times R_{PH}} \times R_{REF} \quad \text{(eq. 25)}$$

Here, I_{LIM} is the peak average current limit for the supply output. The peak average current is the dc current limit plus the output ripple current. In this example, choose I_{LIM_DC} =82.8 A and having a ripple current of 10 A gives an I_{LIM} of 92.8 A. R_{CS} is selected as 110 kΩ in this example, R_{PH} is 61.9 kΩ, DCR is 0.57 mΩ (assuming). This results in an R_{LIM} = 4.7 kΩ, for which 4.53 kΩ is chosen as the nearest 1% value.

The per−phase initial duty cycle limit and peak current during a load step are determined by:

$$D_{MAX} = D \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_R} \quad \text{(eq. 26)}$$

$$I_{PHMAX} \cong \frac{D_{MAX}}{f_{SW}} \times \frac{(V_{IN} - V_{VID})}{L} \quad \text{(eq. 27)}$$

For the ADP3430, the maximum COMP voltage ($V_{COMP(MAX)}$) is 4.4 V and the COMP pin bias voltage (V_{BIAS}) is 1.2 V. In this example, the maximum duty cycle is 0.687 and the peak current is 53.3 A.

The limit of the peak per−phase current described earlier during the secondary current limit is determined by:

$$I_{PHLIM} \cong \frac{V_{COMP(CLAMPED)} - V_{BIAS}}{A_D \times R_{DS(MAX)}} \quad \text{(eq. 28)}$$

For the ADP3430, the current balancing amplifier gain (A_D) is 5 and the clamped COMP pin voltage is 3.3 V. Using an $R_{DS(MAX)}$ of 4.0 mΩ (low−side on resistance at 125°C) results in a per−phase peak current limit of 100 A. This current level can be reached only with an absolute short at the output, and the current limit latchoff function shuts down the regulator before overheating can occur.

I_{MON} Setpoint

According to the function definition, I_{MON} output voltage should represent the load condition within the whole load current range. The formula below will result R_{IMON} in need:

$$R_{IMON} = \frac{V_{IMON}}{I_{IMON}} = \frac{V_{IMON} \times R_{LIM}}{M \times R_{CS} \times \frac{DCR}{R_{PH}} \times I_L} \quad \text{(eq. 29)}$$

Here, I_L is the total load current, M =10 is the current gain for I_{MON}. Since I_{MON} output clamp voltage is around 1.1 V, V_{IMON} is selected as 0.8 V when $I_L = I_{MAX}$ (69 A). While R_{LIM} = 4.53 kΩ, R_{IMON} is calculated as 5.18 kΩ, for which 5.36 kΩ is chosen as the nearest 1% value.

There is a capacitor (C_{IMON}) in parallel with R_{IMON}, in order to filter output current ripple. The time constant of $R_{IMON} * C_{IMON}$ should be much bigger (> 10 x) than circuit switching period. In this example, C_{IMON} is selected as 2.2 μF.

Feedback Loop Compensation Design

Optimized compensation of the ADP3430 allows the best possible response of the regulator output to a load change. A type−three compensator on the voltage feedback is adequate for proper compensation of the output filter. Selecting R_{fb} = 1.24 kΩ, assuming $C_a >> C_{fb}$, compensator

DC gain = 120 dB, Equation 30 to Equation 33 are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning the ADP3430 section).

First, compute the time constants for all the poles and zeros in the system using Equation 30 to Equation 33.

$$C_a = \frac{1}{R_{fb} \times Gain} - C_{fb} = \frac{1}{R_{fb} \times Gain}$$

$$C_a = \frac{1}{1.24\ k\Omega \times 10^{\frac{120}{20}}} = 806\ pF \quad \text{(eq. 30)}$$

$$R_a = \frac{1}{0.5 \times \omega_{c\_target} \times C_a} = \frac{1}{0.5 \times \left(\frac{1}{6} \times 2\pi \times 300\ kHz\right) \times 806\ pF} = 7.9\ k\Omega \quad \text{(eq. 31)}$$

$$C_{fb} = \frac{1}{1.5 \times \omega_S \times R_a} = \frac{1}{1.5 \times (2\pi \times 300\ kHz) \times 7.9\ k\Omega} = 44\ pF \quad \text{(eq. 32)}$$

$$C_b = \frac{1}{2 \times \omega_{c\_target} \times R_{fb}} = \frac{1}{2 \times \left(\frac{1}{6} \times 2\pi \times 300\ kHz\right) \times 1.24\ k\Omega} = 1.28\ nF \quad \text{(eq. 33)}$$

Figure 9 and Figure 10 show the typical transient response using these compensation values.

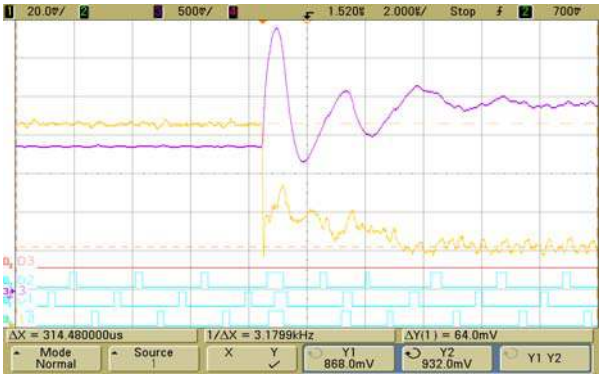


Figure 9. Typical Transient Response for Design Example Load Step

Figure 10. Typical Transient Response for Design Example Load Release
1−Vo, 3−COMP, 4−TRDET, D0~D2−PWM1~3

CIN Selection and Input Current di/dt Reduction

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to $n \times V_{OUT}/V_{IN}$ and an amplitude of one−nth the maximum output current. To prevent large voltage transients, a low ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by:

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{N \times D} - 1} \quad \text{(eq. 34)}$$

$$I_{CRMS} = 0.1266 \times 56\ A \times \sqrt{\frac{1}{3 \times 0.1266} - 1} = 9.1\ A$$

The capacitor manufacturer's ripple−current ratings are often based on only 2000 hours of life. As a result, it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors can be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 680 μF, 16 V aluminum electrolytic capacitors and twelve 4.7 μF ceramic capacitors.

To reduce the input current di/dt to a level below the recommended maximum of 0.1 A/μs, an additional small inductor (L > 370 nH at 18 A) should be inserted between the converter and the supply bus. This inductor also acts as a filter between the converter and the primary power source.

Thermal Monitor Design

The thermistor is used on the TTSENSE input of the ADP3430 for monitoring the temperature of the VR. A constant current of 123 μA is sourced out of this pin and runs through a thermistor network such as the one shown in Figure 11.

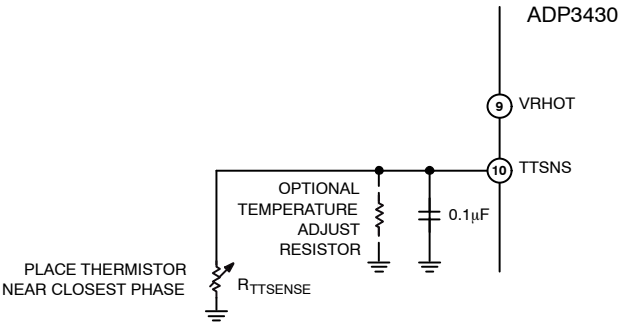


Figure 11. VR Thermal Monitor Circuit

A voltage is generated from this current through the thermistor and sensed inside the IC. When the voltage reaches 0.81 V, the VRHOT gets set. This corresponds to $R_{TTSENSE}$ values of 6.58 kΩ for VRHOT.

These values correspond to a thermistor temperature of ~100°C and ~110°C when using the same type of 100 kΩ NTC thermistor used in the current sense amplifier.

An additional fixed resistor in parallel with the thermistor allows tuning of the trip point temperatures to match the hottest temperature in the VR, when the thermistor itself is directly sensing a proportionately lower temperature. Setting this resistor value is best accomplished with a variable resistor during thermal validation and then fixing this value for the final design.

Additionally, a 0.1 μF capacitor should be used for filtering noise.

Shunt Resistor Design

The ADP3430 uses a shunt to generate 5.0 V from the 12 V supply range. A trade off can be made between the power dissipated in the shunt resistor and the UVLO threshold. Figure 12 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages.

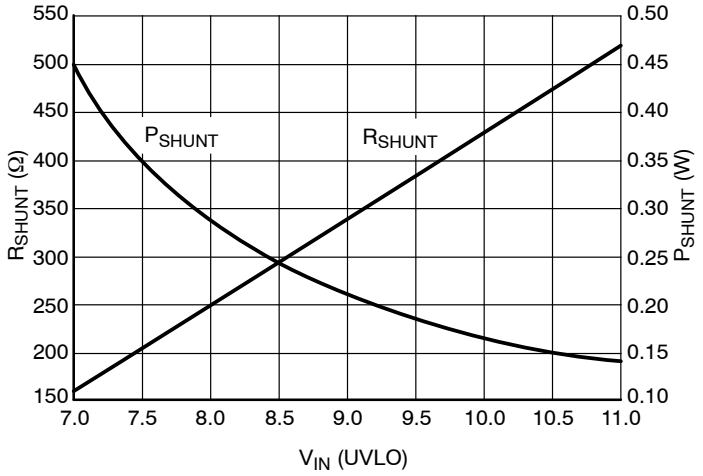


Figure 12. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltage

The maximum power dissipated is calculated using Equation 35.

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \quad \text{(eq. 35)}$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply (if the 12 V input supply is 12 V ± 5%, $V_{IN(MAX)}$ = 12.6 V; if the 12 V input supply is 12 V ± 10%, $V_{IN(MAX)}$ = 13.2 V). $V_{CC(MIN)}$ is the minimum V_{CC} voltage of the ADP3430. This is specified as 4.75 V. R_{SHUNT} is the shunt resistor value.

The CECC standard specification for power rating in surface mount resistors is: 0603 = 0.1 W, 0805 = 0.125 W, 1206 = 0.25 W.

Tuning the ADP3430

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Hook up the dc load to the circuit, turn it on, and verify its operation. Also, check for jitter at no load and full load.

DC Load Line Setting

3. Measure the output voltage at no load (V_{NL}). Verify that it is within tolerance.
4. Measure the output voltage at full load cold (V_{FLCOLD}). Let the board sit for ~10 minutes at full load, and then measure the output (V_{FLHOT}). If there is a change of more than a few mV, adjust R_{CS1} and R_{CS2} using Equation 36 and Equation 38.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad \text{(eq. 36)}$$

5. Repeat Step 4 until the cold and hot voltage measurements remain the same.
6. Measure the output voltage from no load to full load using 5 A steps. Compute the load line slope for each change, and then average to get the overall load line slope (R_{OMEAS}).
7. If R_{OMEAS} is off from R_O by more than 0.05 mΩ, use Equation 37 to adjust the R_{PH} values.

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad \text{(eq. 37)}$$

8. Repeat Step 6 and Step 7 to check the load line. Repeat adjustments if necessary.
9. When the dc load line adjustment is complete, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the remainder of the procedure.
10. Measure the output ripple at no load and full load with a scope, and make sure it is within specifications.

$$R_{CS1(NEW)} = \frac{1}{\frac{R_{CS1(OLD)} + R_{TH(25^oC)}}{R_{CS1(OLD)} \times R_{TH(25^oC)} + \left(R_{CS1(OLD)} - R_{CS2(NEW)}\right) \times \left(R_{CS1(OLD)} - R_{TH(25^oC)}\right)} - \frac{1}{R_{TH(25^oC)}}} \quad \text{(eq. 38)}$$

AC Load Line Setting

11. Remove the dc load from the circuit and hook up the dynamic load.
12. Hook up the scope to the output voltage and set it to dc coupling with the time scale at 100 μs/div.
13. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
14. Measure the output waveform (use dc offset on scope to see the waveform). Try to use a vertical scale of 100 mV/div or finer. This waveform should look similar to Figure 13.

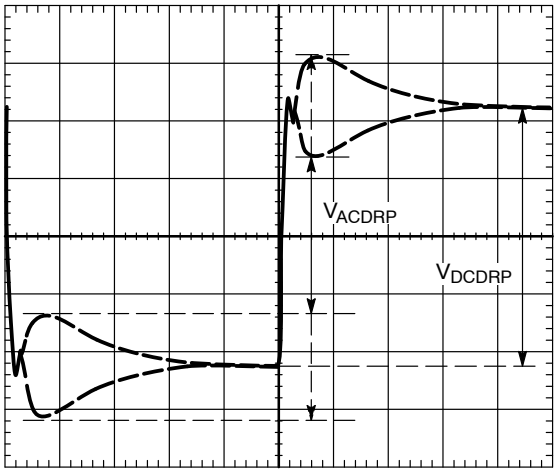


Figure 13. AC Load Line Waveform

15. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP} as shown in Figure 13. Do not measure the undershoot or overshoot that happens immediately after this step.
16. If V_{ACDRP} and V_{DCDRP} are different by more than a few millivolts, use Equation 38 to adjust C_{CS}. Users may need to parallel different values to get the right one because limited standard capacitor values are available. It is a good idea to have locations for two capacitors in the layout for this.

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad \text{(eq. 39)}$$

17. Repeat Step 11 to Step 13 and repeat the adjustments, if necessary. Once complete, do not change C_{CS} for the remainder of the procedure. Set the dynamic load step to maximum step size. Do not use a step size larger than needed. Verify that the output waveform is square, which means that V_{ACDRP} and V_{DCDRP} are equal.

Initial Transient Setting

18. With the dynamic load still set at the maximum step size, expand the scope time scale to either 2 μs/div or 5 μs/div. The waveform can have two overshoots and one minor undershoot (see Figure 14). Here, V_{DROOP} is the final desired value.

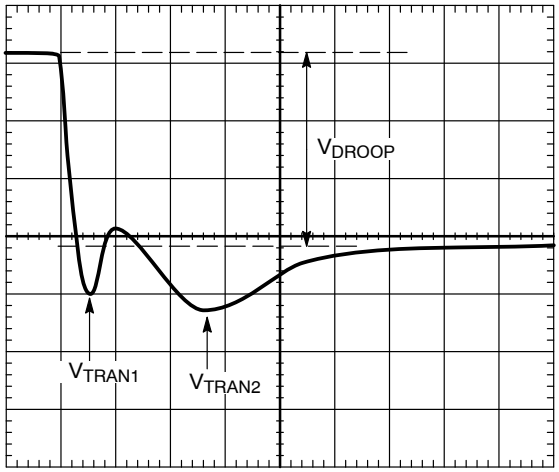


Figure 14. Transient Setting Waveform

19. If both overshoots are larger than desired, try making the adjustments using the following suggestions:
    - Make the ramp resistor larger by 25% (R_{RAMP})
    - For V_{TRAN1}, increase C_B or increase the switching frequency
    - For V_{TRAN2}, increase R_A and decrease C_A by 25%

    If these adjustments do not change the response, the design is limited by the output decoupling. Check

the output response every time a change is made, and check the switching nodes to ensure that the response is still stable.

20. For load release (see Figure 15), if $V_{TRANREL}$ is larger than the allowed overshoot, there is not enough output capacitance. Either more capacitance is needed, or the inductor values need to be made smaller. When changing inductors, start the design again using a spreadsheet and this tuning procedure.

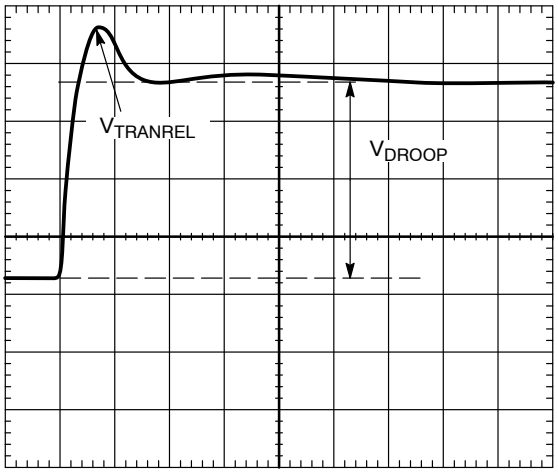


Figure 15. Transient Setting Waveform

Because the ADP3430 turns off all of the phases (switches inductors to ground), no ripple voltage is present during load release. Therefore, the user does not have to add headroom for ripple. This allows load release $V_{TRANREL}$ to be larger than V_{TRAN1} by the amount of ripple, and still meet specifications.

If V_{TRAN1} and $V_{TRANREL}$ are less than the desired final droop, this implies that capacitors can be removed. When removing capacitors, also check the output ripple voltage to make sure it is still within specifications.

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Requirements

For good results, a PCB with at least four layers is recommended. This provides the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, use vias liberally to create several parallel current paths, so the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3430) must cross through power circuitry, it is best to interpose a signal ground plane between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3430 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing into it.

The components around the ADP3430 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB pin and CSSUM pin. The output capacitors should be connected as close as possible to the load (or connector), for example, a microprocessor core, that receives the power. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop described in the Power Circuitry Recommendations sections.

Power Circuitry Recommendations

The switching power path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system and noise−related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing; and it accommodates the high current demand with minimal voltage loss.

When a power dissipating component, for example, a power MOSFET, is soldered to a PCB, it is recommended to liberally use the vias, both directly on the mounting pad and immediately surrounding it. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heat−sink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation in the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the

current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

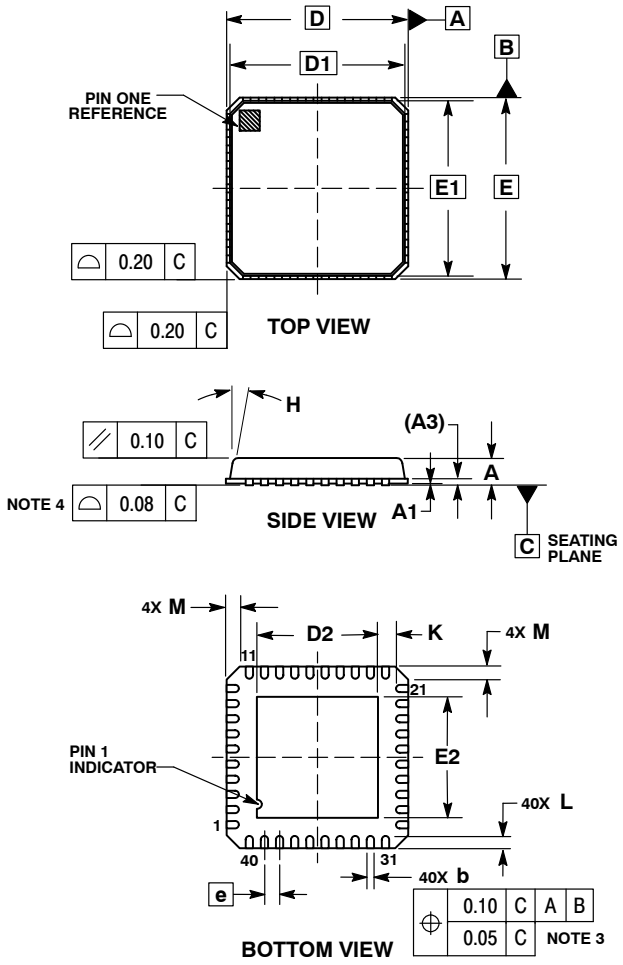
Signal Circuitry Recommendations

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB trace and FBRTN trace should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

PACKAGE DIMENSIONS

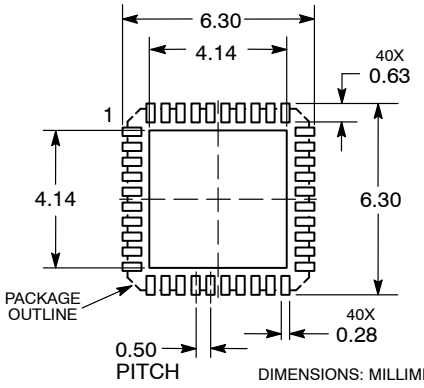
LFCSP40 6x6, 0.5P
CASE 932AC−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D1	5.75 BSC	
D2	3.95	4.25
E	6.00 BSC	
E1	5.75 BSC	
E2	3.95	4.25
e	0.50 BSC	
H	−−−	12°
K	0.20	−−−
L	0.30	0.50
M	−−−	0.60

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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