National Semiconductor

MICROCIRCUIT DATA SHEET

MN54F194-X REV 1B0

Original Creation Date: 03/29/96
Last Update Date: 06/21/02
Last Major Revision Date: 03/29/96

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

General Description

The F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The F194 is similar in operation to the F195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

Industry Part Number

54F194

NS Part Numbers

54F194DM-MLS
54F194DMQB.
54F194LMQB.

Prime Die

M194

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Typical Shift Frequency of 150 MHZ
- Asynchronous Master Reset
- Hold (do Nothing) Mode
- Fully Synchronous Serial or Parallel Data Transfers

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0 C to +70 C
Military	-55 C to +125 C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, -55 C to 125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V, VINH=5.5V, VINL=0.0V	1, 3	INPUTS		20	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=7.0V, VINH=5.5V, VINL=0.0V	1, 3	INPUTS		100	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.5V, VINL=0.0V, VINH=5.5V	1, 3	INPUTS		-0.6	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIL=0.8V, VIH=2.0V, IOL=20mA, VINH=5.5V, VINL=0.0V	1, 3	OUTPUTS		0.5	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, VIL=0.8V, VINH=5.5V, VIH=2.0V, IOH=-1.0mA, VINL=0.0V	1, 3	OUTPUTS	2.5		V	1, 2, 3
IOS	Short-Circuit Current	VCC=5.5V, VINH=5.5V, VINL=0.0V, VM=0.0V	1, 3	OUTPUTS	-60	-150	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=5.5V, VINH=4.5V	1, 3	INPUTS		-1.2	V	1, 2, 3
ICC	Supply Current	VCC=5.5V, VINL=0.0V, VINH=5.5V	1, 3	VCC		46	mA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VINL=0.0V, VINH=5.5V, VM=5.5V	1, 3	OUTPUTS		250	uA	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS

tpLH	Propagation Delay	VCC=5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	CP to Q	3.5	7.0	ns	9
			2, 4	CP to Q	3.0	8.5	ns	10, 11
tpHL (1)	Propagation Delay	VCC=5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	CP to Q	3.5	7.0	ns	9
			2, 4	CP to Q	3.0	8.5	ns	10, 11
tpHL (2)	Propagation Delay	VCC=5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	$\overline{MR}$ to Q	4.5	12.0	ns	9
			2, 4	$\overline{MR}$ to Q	4.5	14.5	ns	10, 11
th(H)	Hold Time (High)	VCC= 5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	5	P,DSR or DSL to CP	1.0		ns	9
			5	P,DSR or DSL to CP	1.5		ns	10, 11
th(L)	Hold Time (Low)	VCC= 5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	5	P,DSR or DSL to CP	0		ns	9
			5	P,DSR or DSL to CP	1.0		ns	10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ts(H)	Setup Time (High)	VCC= 5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	5	P,DSR or DSL to CP	4.5		ns	9
			5	P,DSR or DSL to CP	6.0		ns	10, 11
		VCC=5.5V @25C VCC=4.5V & 5.5V @ -55/125C	5	S to CP	9.0		ns	9
			5	S to CP	10.5		ns	10, 11
ts(L)	Setup Time (Low)	VCC= 5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	5	P,DSR or DSL to CP	4.0		ns	9, 10, 11
		VCC=5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	5	S to CP	8.0		ns	9, 10, 11
th(H/L)	Setup Time (High or Low)	VCC=5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	5	S to CP	0		ns	9, 10, 11
tw (L)	Pulse Width (Low)	VCC=5.5V @25C, VCC=4.5V & 5.5V @ -55/125C TR/TF=1.0ns	5	CP	5.0		ns	9
			5	CP	5.5		ns	10, 11
		VCC= 5.5V @25C, VCC=4.5V & 5.5V @ -55/125C TR/TF=1.0ns	5	$\overline{MR}$	5.0		ns	9, 10, 11
tREC	Recovery Time	VCC= 5.5V @25C, VCC=4.5V & 5.5V @ -55/125C	5	$\overline{MR}$ to CP	7.0		ns	9
			5	$\overline{MR}$ to CP	9.0		ns	10, 11
fMAX	Maximum Clock Frequency	VCC= 5.5V @25C, VCC=4.5V & 5.5V @ -55/125C TR/TF=1.0ns	5	CP	105		MHZ	9
			5	CP	90		MHZ	10, 11

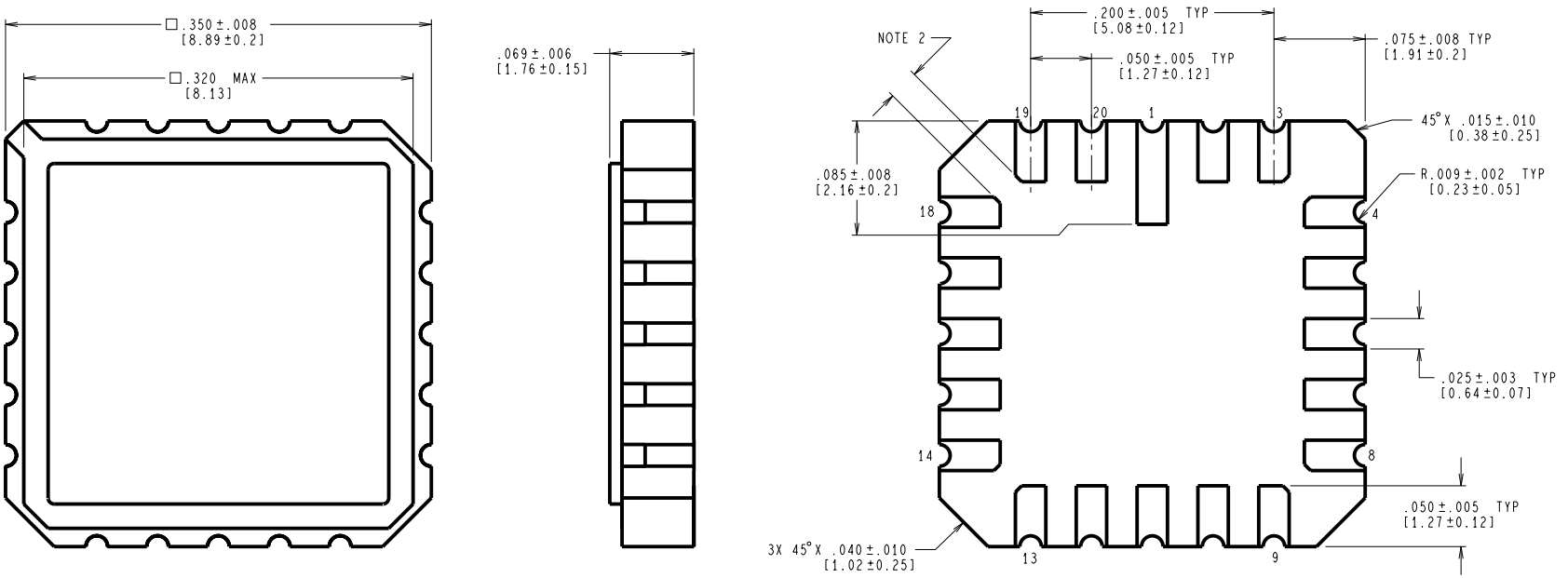
Note 1: Screen tested 100% on each device at -55 C, +25 C & +125 C temperature, Subgroups A1, 2, 3, 7 & 8.
Note 2: Screen tested 100% on each device at +25 C temperature only, Subgroup A9.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., Subgroups A1, 2, 3, 7 & 8.
Note 4: Sample Tested (Method 5005, Table 1) on each MFG. lot at +25 C Subgroup A9, & periodically at +125 C & -55 C temp., Subgroups 10 & 11.
Note 5: Guaranteed but not tested. (DESIGN CHARACTERIZATION DATA)

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH [MM]

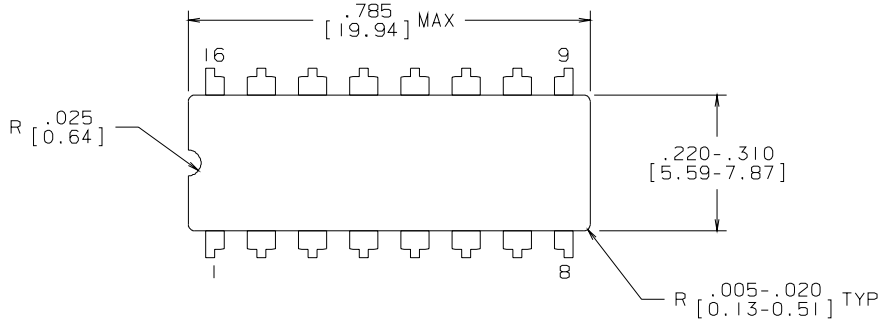
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

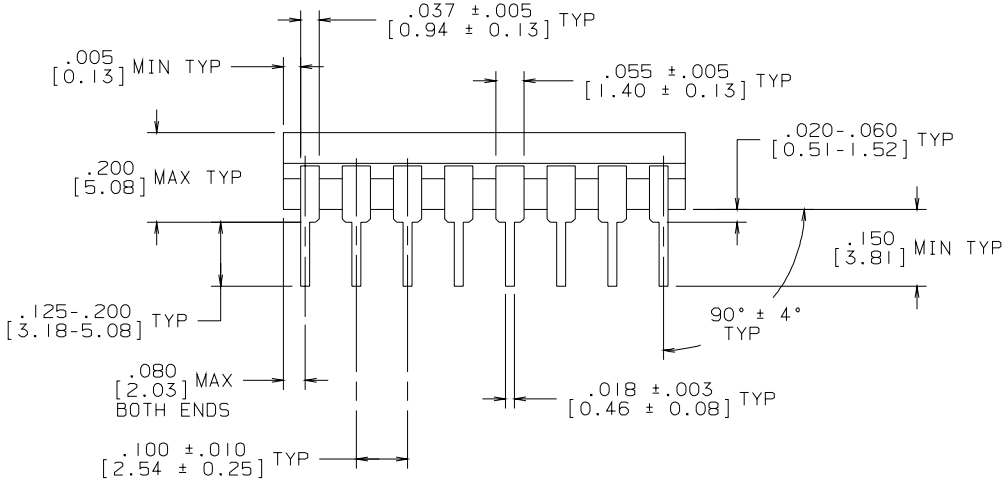
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

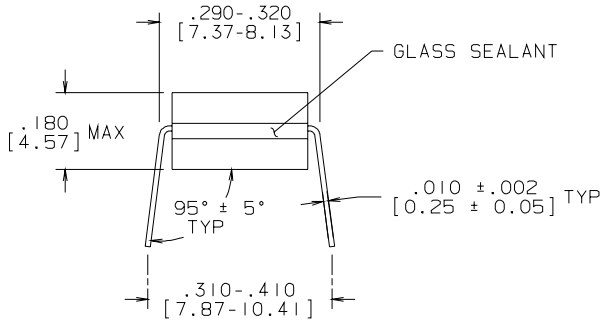
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1B0	M0004027	06/21/02	Rose Malone	Update MDS: MN54F194-X, Rev. 1A0 to MN54F194-X, Rev. 1B0. Updated NS Part Numbers on Main Table, Added Mkt Dwg.'s to Graphics Section.