# TPS1H000-Q1 40-V, 1-Ω, Single-Channel Smart High-Side Switch

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Single-Channel 1000-mΩ Smart High-Side Switch
- Wide Operating Voltage: 3.4 V to 40 V
- Low Standby Current: <500 nA
- Adjustable Current Limit With External Resistor
  - ±15% When ≥150 mA
  - ±10% When ≥300 mA
- Configurable Behavior After Current Limit
  - Holding Mode
  - Latch-Off Mode With Adjustable Delay Time
  - Auto-Retry Mode
- Supports Standalone Operation Without an MCU
- Protection:
  - Short-to-GND and Overload
  - Thermal Shutdown and Thermal Swing
  - Negative Voltage Clamp for Inductive Loads
  - Loss-of-GND and Loss-of-Battery
- Diagnostics:
  - Overload and Short-to-GND Detection
  - Open-Load and Short-to-Battery Detection in ON or OFF State
  - Thermal Shutdown and Thermal Swing

## 2 Applications

- Single-Channel LED Driver
- Single-Channel High-Side Relay Driver
- Body Lighting
- Advanced Driver Assistance Systems (ADAS) Sensors
- General Resistive, Inductive and Capacitive Loads

## 3 Description

The TPS1H000-Q1 device is a fully protected single-channel high-side power switch with an integrated 1000-mΩ NMOS power FET.

An adjustable current limit improves system reliability by limiting the inrush or overload current. The high accuracy of the current limit improves overload protection, simplifying the front-stage power design. Configurable features besides current limit provide design flexibility in the areas of functionality, cost, and thermal dissipation.

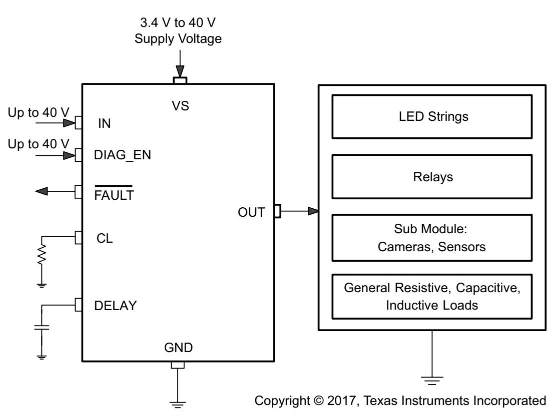
The device supports full diagnostics with the digital status output. Open-load detection is available in both the ON- and OFF-states. The device supports operation with or without an MCU. Standalone mode allows use of the device in isolated systems.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS1H000-Q1 | HVSSOP (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Block Diagram**




**Current-Limit Protection in Auto-Retry Mode**

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## 4 Revision History

**Changes from Revision B (March 2018) to Revision C** — **Page**

- Changed IN is high and DIAG_EN is high to IN is low and DIAG_EN is low in the *Standby Mode* section .... 21

**Changes from Revision A (August 2017) to Revision B** — **Page**

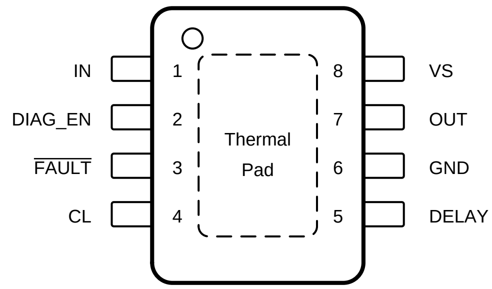
- Added Footnote 2 to the *Electrical Characteristics* table .... 6
- Added reverse current protection information to the *Reverse-Current Protection* section .... 19

**Changes from Original (August 2017) to Revision A** — **Page**

- Changed numerous locations in the *Features*, *Applications*, and *Description* sections .... 1
- Added typical characteristic graphs .... 8
- Changed text in the second paragraph of the Overview section .... 10
- Changed the links for references to Table 2 and Table 3. .... 14
- Added a row to Table 3 .... 15
- Changed text references to Figure 24 and Figure 25 .... 17
- Added application curves and explanatory text .... 23
- Changed "ground pad" to "thermal pad" in Layout Guidelines .... 24

# 5 Pin Configuration and Functions

**DGN PowerPAD™ Package**
**8-Pin HVSSOP With Exposed Thermal Pad**
**Top View**




Not to scale

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CL | 4 | O | Adjustable current limit. Connect to device GND if external current limit is not used. |
| DELAY | 5 | I/O | Function configuration when in current limit; internal pullup |
| DIAG_EN | 2 | I | Enable the diagnostic function |
| $\overline{\text{FAULT}}$ | 3 | O | Open-drain diagnostic status output. Leave floating if not used |
| GND | 6 | — | Ground pin |
| IN | 1 | I | Input control for output activation; internal pulldown |
| OUT | 7 | O | Output, source of the high-side switch, connected to the load |
| VS | 8 | I | Power supply, drain for the high-side switch. |
| Thermal pad | — | — | Thermal pad. Connect to device GND or leave floating. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage VS pin | t < 400 ms | — | 42 | V |
| Reverse polarity voltage (3) | t < 1 minute | –36 | — | V |
| Current on GND | t < 2 minutes | –100 | 250 | mA |
| Voltage on IN and DIAG_EN pins | | –0.3 | VS | V |
| Current on IN and DIAG_EN pins | | –10 | — | mA |
| Voltage on DELAY pin | | –0.3 | 7 | V |
| Current on DELAY pin | | –60 | — | mA |
| Voltage on $\overline{FAULT}$ pin | | –0.3 | 7 | V |
| Current on $\overline{FAULT}$ pin | | –30 | 10 | mA |
| Voltage on CL pin | | –0.3 | 7 | V |
| Current on CL pin | | — | 6 | mA |
| Voltage on OUT pin | | — | 42 | V |
| Inductive load switch-off energy dissipation single pulse(4) | | — | 40 | mJ |
| Operating junction temperature | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.
(3) Reverse polarity condition: $V_{IN}$ = 0 V, reverse current < $I_{R(2)}$, GND pin 1-kΩ resistor in parallel with diode.
(4) Test condition: $V_{VS}$ = 13.5 V, L = 300 mH, $T_J$ = 150°C. FR4 2s2p board, 2 × 70-µm Cu, 2 × 35-µm Cu. 600 mm$^2$ thermal pad copper area.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | All pins except VS, OUT, and GND | ±2000 | V |
| | | | Pins VS, OUT, and GND | ±3000 | |
| | | Charged-device model (CDM), per AEC Q100-011 | | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Operating voltage | 4 | | 40 | V |
| | Voltage on IN and DIAG_EN pins | 0 | | 40 | V |
| | Voltage on $\overline{FAULT}$ pin | 0 | | 5 | V |
| $I_{o,nom}$ | Nominal dc load current | 0 | | 1 | A |
| $T_J$ | Operating junction temperature | –40 | | 150 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS1H000-Q1 DGN (HVSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 49.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 50.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 21.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 21.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 7.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

## 6.5 Electrical Characteristics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING VOLTAGE** | | | | | | |
| $V_{VS(nom)}$ | Nominal operating voltage | | 4 | | 40 | V |
| $V_{VS(uvr)}$ | Undervoltage restart | $V_{VS}$ rising | 3.5 | 3.7 | 4 | V |
| $V_{VS(uvf)}$ | Undervoltage shutdown | $V_{VS}$ falling | 3 | 3.2 | 3.4 | V |
| $V_{(uv,hys)}$ | Undervoltage shutdown, hysteresis | | | 0.5 | | V |
| **OPERATING CURRENT** | | | | | | |
| $I_{(op)}$ | Nominal operating current | $V_{VS}$ = 13.5 V, $V_{IN}$ = 5 V, $V_{DIAG\_EN}$ = 0 V, $I_{OUT}$ = 0.1 A, $I_{CL}$ = 0.5 A. | | | 5 | mA |
| $I_{(off)}$ | Standby current | $V_{VS}$ = 13.5 V, $V_{IN}$ = $V_{DIAG\_EN}$ = $V_{CL}$ = $V_{OUT}$ = 0 V, $T_J$ = 25 °C | | | 0.5 | µA |
| | | $V_{VS}$ = 13.5 V, $V_{IN}$ = $V_{DIAG\_EN}$ = $V_{CL}$ = $V_{OUT}$ = 0 V, $T_J$ = 125 °C | | | 3 | |
| $I_{(off,diag)}$ | Standby current with diagnostics enabled | $V_{VS}$ = 13.5 V, $V_{IN}$ = 0 V, $V_{DIAG\_EN}$ = 5 V | | | 3 | mA |
| $t_{(off,deg)}$ | Standby-mode deglitch time[1] | IN from high to low, if deglitch time≥ $t_{(off,deg)}$, the device enters into standby mode. | | 12.5 | | ms |
| $I_{lkg(out)}$ | Output leakage current in off-state | $V_{VS}$ = 13.5 V, $V_{IN}$ = $V_{DIAG\_EN}$ = $V_{OUT}$ = 0 V | | | 3 | µA |
| **POWER STAGE** | | | | | | |
| $r_{DS(on)}$ | On-state resistance | $V_{VS}$ ≥ 3.5 V, $T_J$ = 25°C | | 1000 | | mΩ |
| | | $V_{VS}$ ≥ 3.5 V, $T_J$ = 150°C | | | 2000 | |
| $I_{CL(int)}$ | Internal current limit | CL pin connected to GND | 1 | | 1.8 | A |
| $I_{CL(TSD)}$ | Current-limit value percentage during thermal shutdown | | | 60% | | |
| $V_{DS(clamp)}$ | Drain−to−source voltage internally clamped | | 45 | | 65 | V |
| **OUTPUT DIODE CHARACTERISTICS** | | | | | | |
| $V_F$ | Drain−to-source diode voltage | IN = 0, $I_{OUT}$ = −0.15 A | 0.3 | 0.7 | 1 | V |
| $I_{R(1)}$ | Continuous reverse current from source to drain during a short-to-battery condition[1] | t < 60 s, $V_{IN}$= 0 V, $T_J$ = 25°C. | | | 1 | A |
| $I_{R(2)}$ | Continuous reverse current from source to drain during a reverse-polarity condition[1] | t < 60 s, $V_{IN}$= 0 V, $T_J$ = 25°C. GND pin 1-kΩ resistor in parallel with diode. | | | 1 | A |
| **LOGIC INPUT (IN, DIAG_EN)** | | | | | | |
| $V_{IH}$ | Logic high-level voltage | | 2 | | | V |

(1) Value specified by design, not subject to production test

## Electrical Characteristics (continued)

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Logic low-level voltage | | | | 0.8 | V |
| $R_{pd,in}$ | Logic-pin pulldown resistor | IN. $V_{IN}$ = 5 V | 150 | | 400 | kΩ |
| | | DIAG_EN. $V_{VS}$ = $V_{DIAG\_EN}$ = 5 V | 350 | | 850 | |
| **DIAGNOSTICS** | | | | | | |
| $I_{lkg(loss,GND)}$ | Loss of ground output leakage current | | | | 100 | µA |
| $t_{d(ol,on)}$ | Open-load deglitch time in on-state | $V_{IN}$ = 5 V, $V_{DIAG\_EN}$ = 5 V, when $I_{OUT}$ < $I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$, open load is detected. | 200 | 300 | 450 | µs |
| $I_{(ol,on)}$ | Open-load detection threshold in on-state | $V_{IN}$ = 5 V, $V_{DIAG\_EN}$ = 5 V, when $I_{OUT}$ < $I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$, open load is detected. | 1 | 5 | 8 | mA |
| $V_{(ol,off)}$ | Open-load detection threshold in off-state | $V_{IN}$ = 0 V, $V_{DIAG\_EN}$ = 5 V, when $V_{VS}$ – $V_{OUT}$ < $V_{(ol,off)}$, duration longer than $t_{d(ol,off)}$, open load is detected. | 1.4 | | 2.6 | V |
| $t_{d(ol,off)}$ | Open-load deglitch time in off-state | $V_{IN}$ = 0 V, $V_{DIAG\_EN}$ = 5 V, when $V_{VS}$ – $V_{OUT}$ < $V_{(ol,off)}$, duration longer than $t_{d(ol,off)}$, open load is detected. | 200 | 300 | 450 | µs |
| $I_{(ol,off)}$ | Off-state output sink current | $V_{IN}$ = 0 V, $V_{DIAG\_EN}$ = 5 V, $V_{VS}$ = $V_{OUT}$ = 13.5 V | –70 | | | µA |
| $V_{\overline{FAULT}}$ | $\overline{FAULT}$ low output voltage | $I_{\overline{FAULT}}$ = 2 mA | | | 0.2 | V |
| $t_{\overline{FAULT}}$ | $\overline{FAULT}$ signal holding time (1) | | | 8.5 | | ms |
| $T_{(SD)}$ | Thermal shutdown threshold (1) | | | 175 | | °C |
| $T_{(SD,rst)}$ | Thermal shutdown status reset (1) | | | 155 | | °C |
| $T_{(sw)}$ | Thermal swing shutdown threshold (1) | | | 60 | | °C |
| $T_{(hys)}$ | Hysterisis for resetting the thermal shutdown and swing (1) | | | 10 | | °C |
| **CURRENT LIMIT AND DELAY CONFIGURATION** | | | | | | |
| $K_{(CL)}$ | Current-limit current ratio (1) | | | 600 | | |
| $V_{CL(th)}$ | Current-limit internal threshold voltage (1) | | | 0.8 | | V |
| $dK_{(CL)}/K_{(CL)}$ | External current limit accuracy (2) ($I_{OUT}$ – $I_{CL}$ × $K_{(CL)}$) × 100 / ($I_{CL}$ × $K_{(CL)}$) | $I_{limit}$ ≥ 0.05 A , $V_{VS}$ – $V_{OUT}$ ≥ 2.5V | –20% | | 20% | |
| | | $I_{limit}$ ≥ 0.15 A , $V_{VS}$ – $V_{OUT}$ ≥ 2.5V | –15% | | 15% | |
| | | $I_{limit}$ ≥ 0.3 A, $I_{limit}$ < 1 A , $V_{VS}$ – $V_{OUT}$ ≥ 2.5V | –10% | | 10% | |
| $I_{dl(chg)}$ | Delay pin charging current in latch-off mode (1) | | | 4.5 | | µA |
| $V_{dl(th)}$ | Pulling up threshold in auto-retry mode | | 2.7 | | | V |
| $V_{dl(ref)}$ | Internal reference voltage in latch-off mode | | | 1.45 | | V |
| $t_{dl1}$ | Internal fixed delay time (1) | | 300 | 400 | 500 | µs |
| $t_{dl2}$ | Adjustable delay time by external capacitor on DELAY pin (1) | Connect with 3.3 uF capacitor as the maximum value. | | | 1000 | ms |
| $t_{CL(deg)}$ | Deglitch time when current limit (1) | IN low to high, $V_{DIAG\_EN}$ = 5 V, the deglitch time from IN rising edge to FAULT reporting out. | 300 | | 500 | µs |
| | | IN keeps high, $V_{DIAG\_EN}$ = 5 V, the deglitch time from CL start-point to FAULT reporting out. | 80 | | 180 | |
| $t_{hic(on)}$ | On-time when in auto-retry mode (1) | | 35 | 40 | 45 | ms |
| $t_{hic(off)}$ | Off-time when in auto-retry mode (1) | | 0.8 | 1 | 1.2 | s |

(2) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting

## 6.6 Switching Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turnon delay time, IN rising edge to 10% of $V_{OUT}$ | $V_{VS}$ = 13.5 V, $V_{DIAG\_EN}$ = 5 V, $I_{OUT}$ = 0.1 A | 20 | 50 | 90 | µs |
| $t_{d(off)}$ | Turnoff delay time, IN falling edge to 90% of $V_{OUT}$ | $V_{VS}$ = 13.5 V, $V_{DIAG\_EN}$ = 5 V, $I_{OUT}$ = 0.1 A | 20 | 50 | 90 | µs |
| $dV/dt_{(on)}$ | Slew rate on, $V_{OUT}$ from 10% to 90% | $V_{VS}$ = 13.5 V, $V_{DIAG\_EN}$ = 5 V, $I_{OUT}$ = 0.1 A | 0.1 | | 0.6 | V/µs |
| $dV/dt_{(off)}$ | Slew rate off, $V_{OUT}$from 90% to 10% | $V_{VS}$ = 13.5 V, $V_{DIAG\_EN}$ = 5 V, $I_{OUT}$ = 0.1 A | 0.3 | | 0.9 | V/µs |

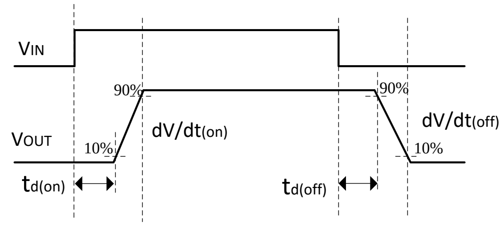



**Figure 1. Output Delay Characteristics**

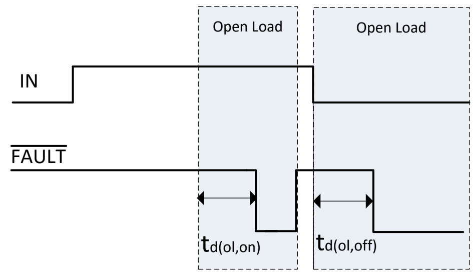



**Figure 2. Open-Load Blanking-Time Characteristic**

## 6.7 Typical Characteristics

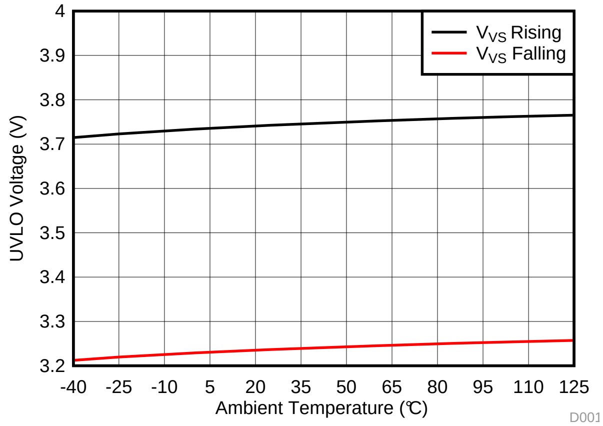



**Figure 3. UVLO Voltage Threshold**

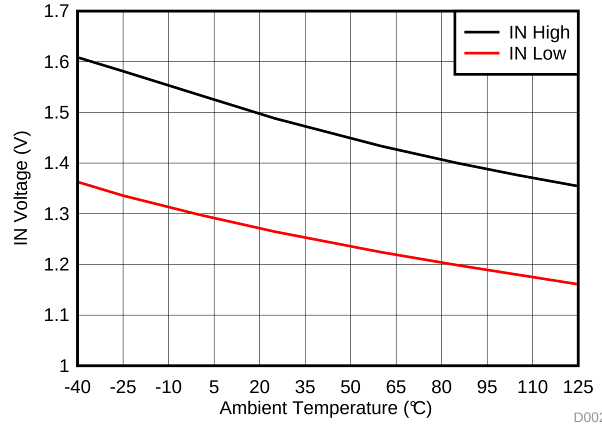



**Figure 4. IN Voltage Threshold**

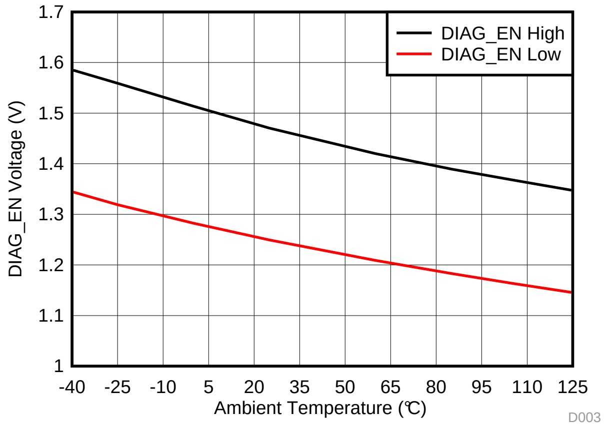



**Figure 5. DIAG_EN Voltage Threshold**

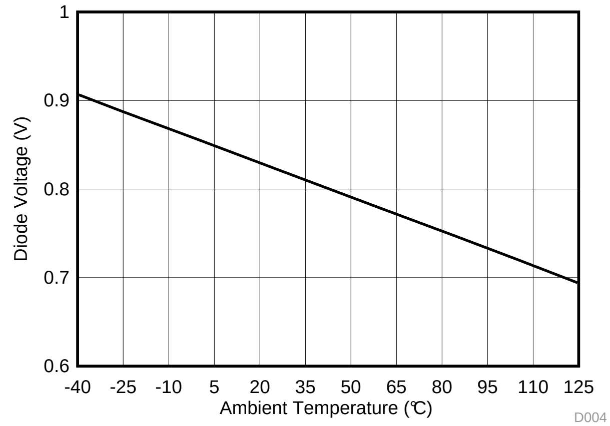



**Figure 6. Body-Diode Forward Voltage**

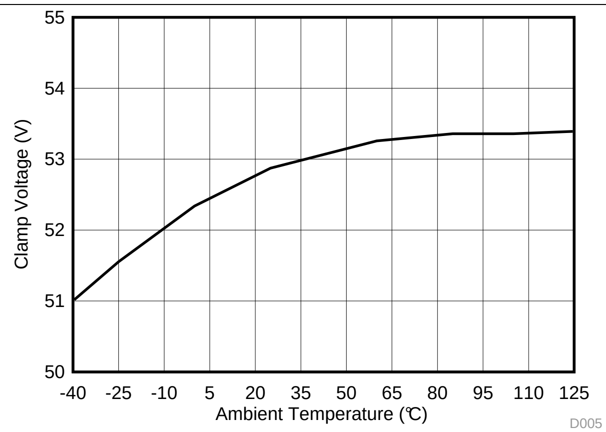



**Figure 7. Drain-to-Source Clamp Voltage**

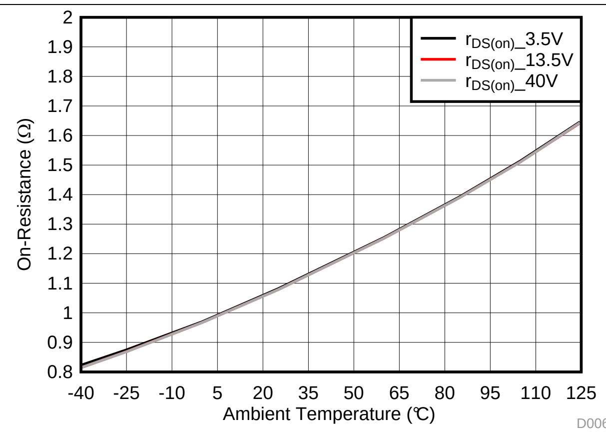
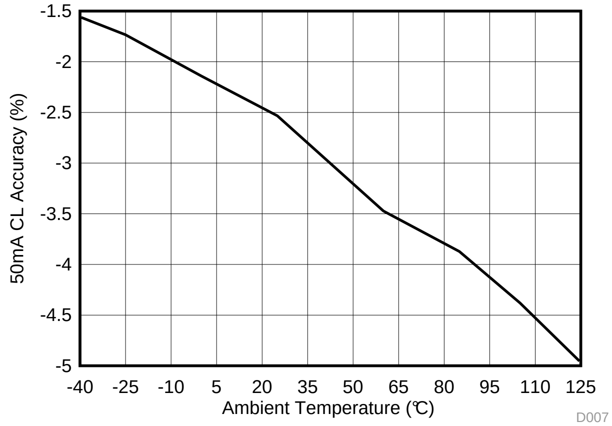


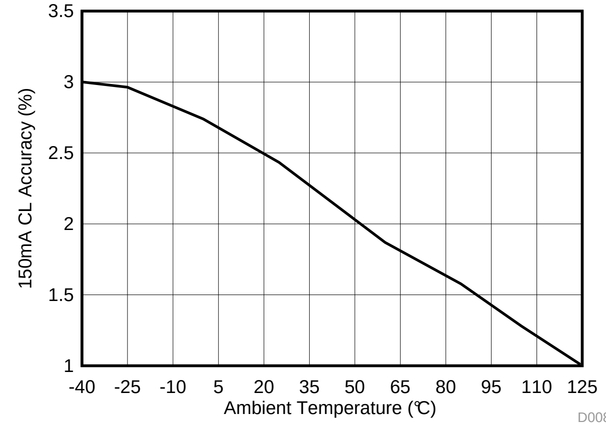

**Figure 8. FET On-Resistance**

## Typical Characteristics (continued)



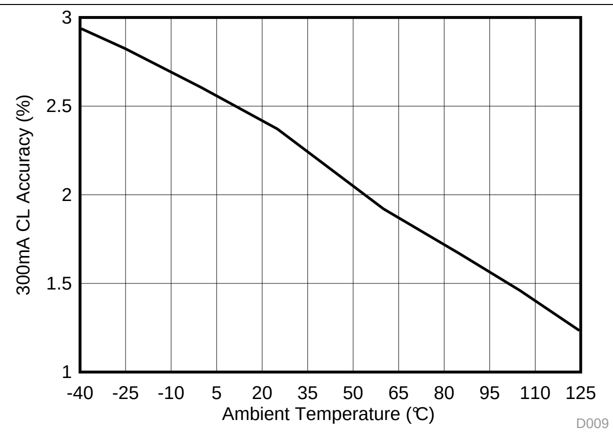

$I_{OUT}$ = 50 mA

**Figure 9. Current-Limit Accuracy at 50 mA**



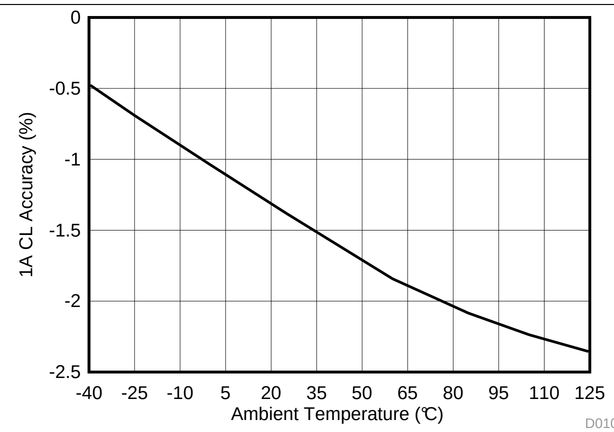

$I_{OUT}$ = 150 mA

**Figure 10. Current-Limit Accuracy at 150 mA**




$I_{OUT}$ = 300 mA

**Figure 11. Current-Limit Accuracy at 300 mA**




$I_{OUT}$ = 1 A

**Figure 12. Current-Limit Accuracy at 1 A**

# 7 Detailed Description

## 7.1 Overview

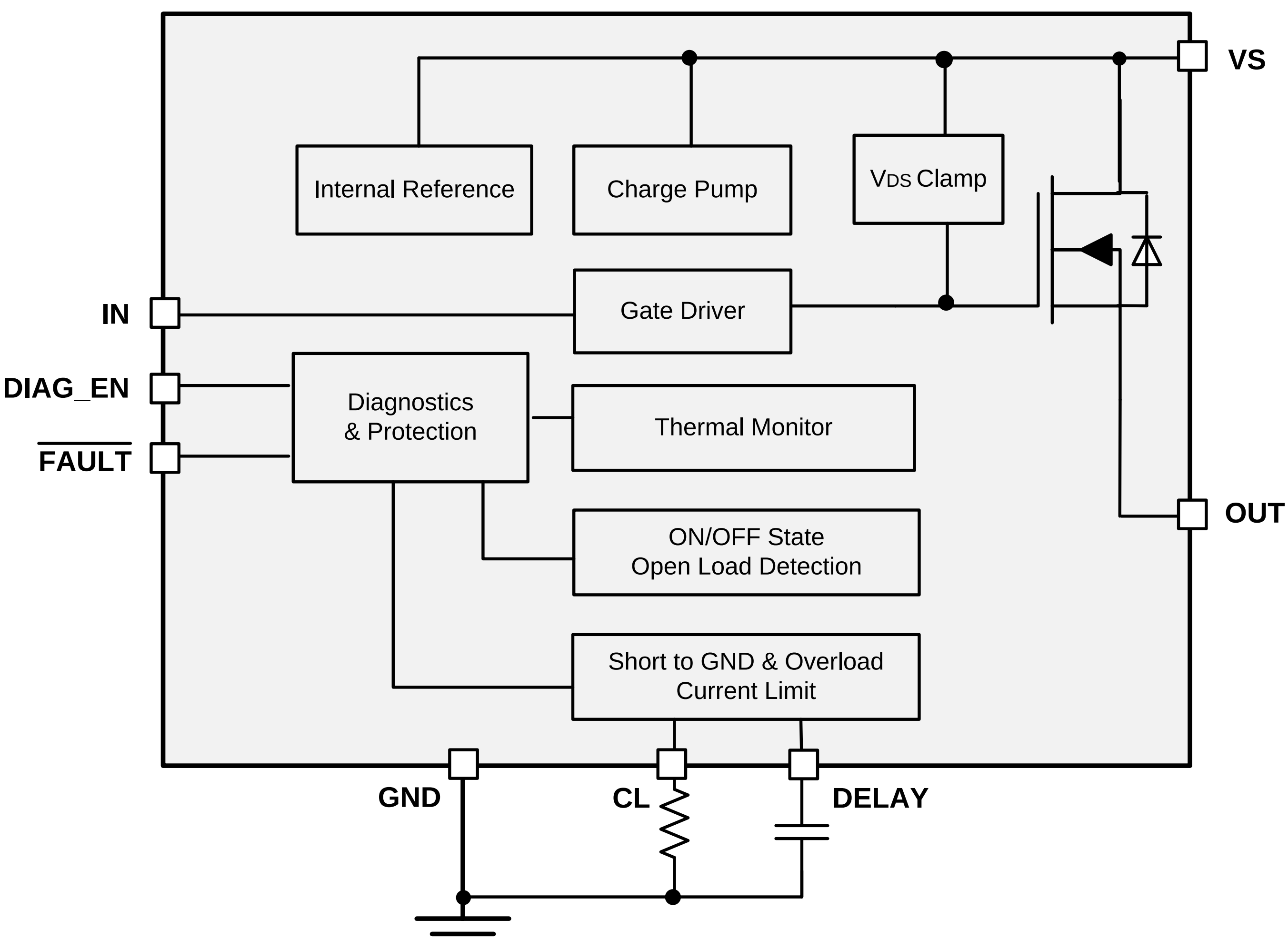
The TPS1H000-Q1 device is a smart high-side switch, with an internal charge pump and single-channel integrated NMOS power FET. The adjustable current-limit function greatly improves the reliability of the whole system. Full diagnostic features enable intelligent control of the load.

The external high-accuracy current limit allows setting the current-limit value for the application. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The TPS1H000-Q1 device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. The TPS1H000-Q1 device allows three modes when a current limit occurs. Through the configuration on the DELAY pin, users can set the output to any of three modes: hold the current consistently, latch off immediately, or retry automatically. The configurable behaviors during current limit provide design flexibility that considers functionality, cost, and thermal dissipation.

The TPS1H000-Q1 device supports full diagnostics with the digital status output. High-accuracy and low-threshold open-load detection enables real-time on-state monitoring. The TPS1H000-Q1 device also supports operation without an MCU, the standalone mode, which allows the system to implement the full functionality locally.

The TPS1H000-Q1 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and sub-modules.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is reached, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET.

The device has two current-limit thresholds.

- Internal current limit – The internal current limit is fixed at $I_{CL(int)}$. Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit – An external resistor is used to set the current-limit threshold. Use Equation 1 to calculate $R_{(CL)}$. $V_{CL(th)}$ is the internal band-gap voltage. $K_{(CL)}$ is the ratio of the output current and the current-limit set value. $K_{(CL)}$ is constant across temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current-limit value by application.

$$R_{CL} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} \quad (1)$$

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected to the device GND.

For better protection from a hard short-to-GND condition (when the IN pin is enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the output before the current-limit closed loop is set up. The fast-trip response time is less than 1 µs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

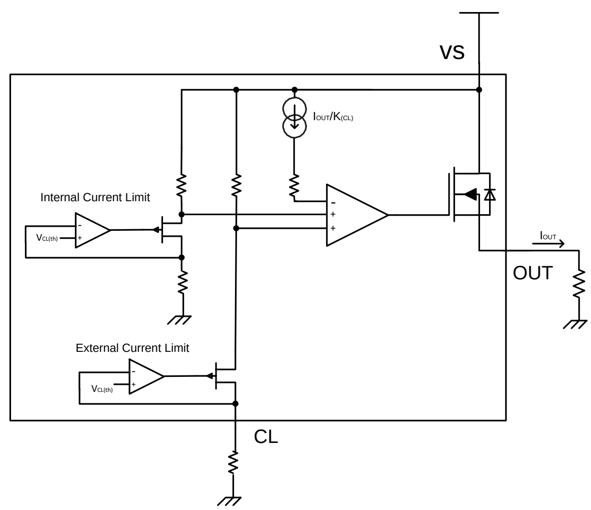



**Figure 13. Current Limit**

## Feature Description (continued)

### 7.3.2 DELAY Pin Configuration

When a current limit occurs, the TPS1H000-Q1 device supports three different behaviors of the output.

**Table 1. Current Limit Configurations**

| MODE | DELAY CONFIGURATION | OUTPUT CURRENT BEHAVIOR | $\overline{FAULT}$ RECOVERY |
|---|---|---|---|
| Holding | Connect to GND directly | When hitting a current limit, the output current holds at the setting current. The device enters into thermal shutdown mode when $T_J > T_{(SD)}$. | $\overline{FAULT}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$ OR when the current limit is removed when IN is high. |
| Latch-off | Connect to GND through a capacitor | When hitting a current limit, the output current holds at the setting current, but latches off after a preset DELAY time ($t_{dl1}$+ $t_{dl2}$). $t_{dl1}$ is the default delay time; $t_{dl2}$ is a capacitor-configurable delay time.<br>The output stays latched off regardless of whether the current limit is removed. The output recovers only when IN is toggling. | $\overline{FAULT}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$. |
| Auto-retry | External pullup | When hitting a current limit, the output current holds at the setting current, but periodically comes on for $t_{hic(on)}$ and turns off for $t_{hic(off)}$. | $\overline{FAULT}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$ OR when the current limit is removed for $t_{hic(on)}$ |

#### *7.3.2.1 Holding Mode*

Holding mode is active when the DELAY pin connects to GND directly. When hitting a current limit, the output current holds at the setting current. The device enters into thermal shutdown mode when $T_J > T_{(SD)}$.

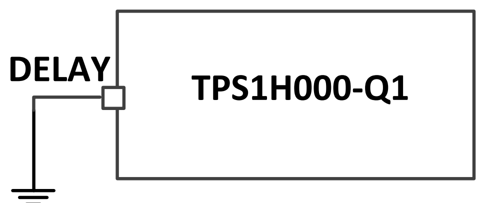



**Figure 14. Holding Mode Connection**

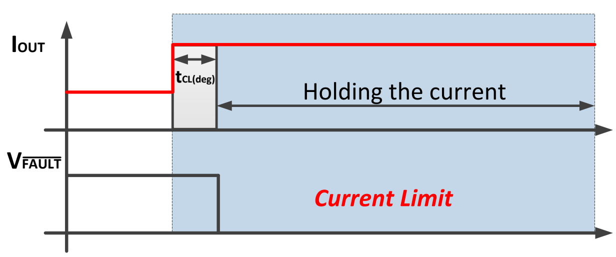



**Figure 15. Holding Mode Example**

#### *7.3.2.2 Latch-Off Mode*

Latch-off mode is active when the DELAY pin connects to GND through a capacitor. When hitting a current limit, the output current holds at the setting current, but latches off after a preset DELAY time ($t_{dl1}$+ $t_{dl2}$). $t_{dl1}$ is the default delay time, $t_{dl2}$ is a configurable delay time set by a capacitor. The output stays latched off regardless of whether the current limit is removed. The output recovers only when IN is toggling.

$t_{dl2}$ can be calculated by Equation 2. The $I_{dl(chg)}$is the device charging current in latch-off mode, $V_{dl(ref)}$ is the internal reference voltage in latch off mode, $t_{dl2}$ is the user-setting delay time, and $C_{DELAY}$ is the capacitor connected on the DELAY pin.

$$C_{DELAY} = \frac{I_{dl(chg)} \times t_{dl2}}{V_{dl(ref)}} \quad (2)$$

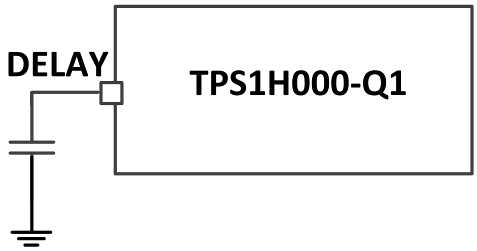



**Figure 16. Latch-Off-Mode Connection**

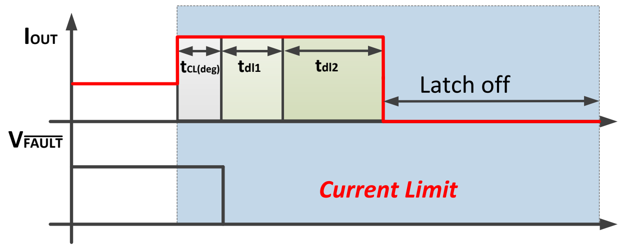



**Figure 17. Latch-Off-Mode Example**

#### 7.3.2.3 Auto-Retry Mode

Auto-retry mode is active when the DELAY pin is externally pulled up. The pullup voltage must be higher than $V_{dl(th)}$. When hitting the current limit, the output current holds at the setting current, but periodically comes on for $t_{hic(on)}$ and turns off for $t_{hic(off)}$.

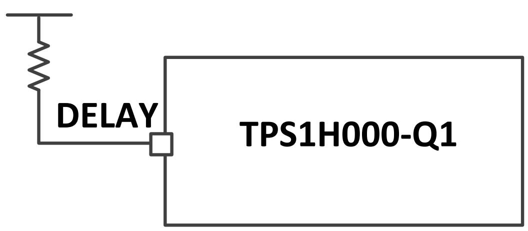



**Figure 18. Auto-Retry-Mode Connection**

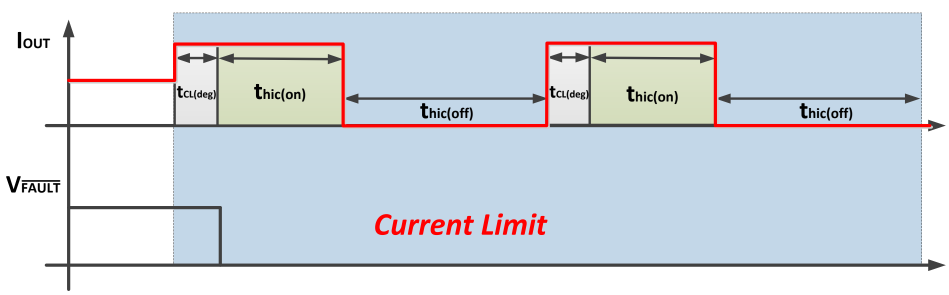



**Figure 19. Auto-Retry-Mode Example**

### 7.3.3 Standalone Operation

In a typical application, the TPS1H000-Q1 device is controlled by a microcontroller. The device also supports standalone operation. IN and DIAG_EN have a 40-V maximum dc rating, and can be connected to the VS pin directly. In auto-retry mode, the DELAY pin can also be connected to the VS pin through a 100-kΩ resistor.

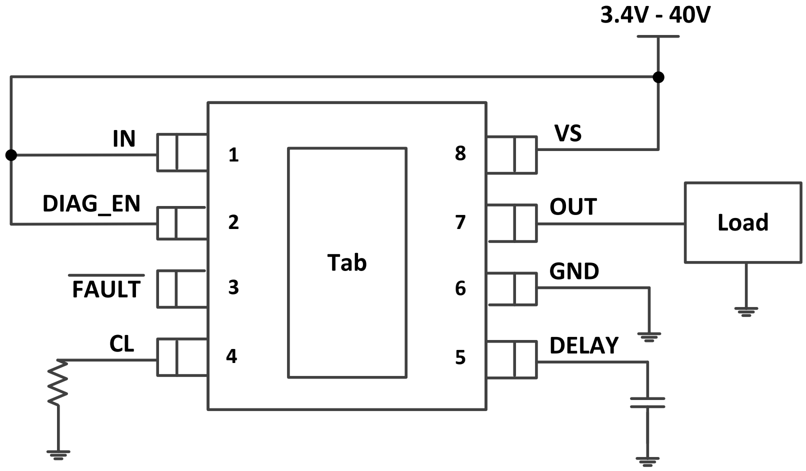



**Figure 20. Standalone Operation in Latch-Off Mode**

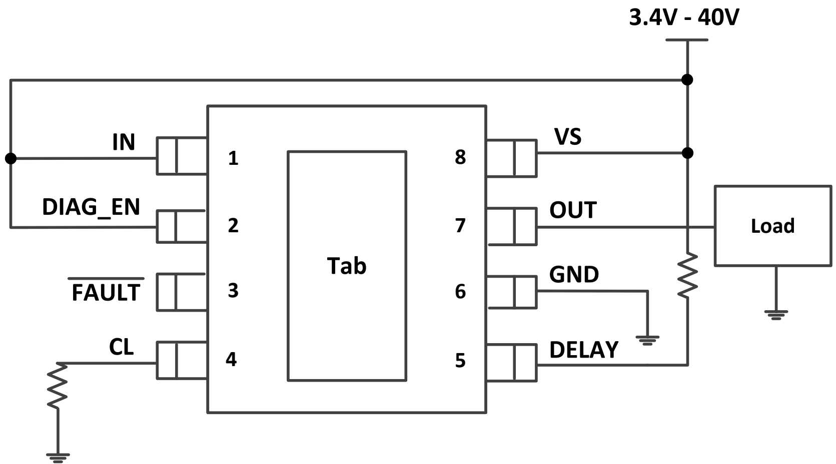



**Figure 21. Standalone Operation in Auto-Retry Mode**

### 7.3.4 Fault Truth Table

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the microcontroller can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and IN low.

Table 2 applies when the DIAG_EN pin is enabled. Table 3 applies when the DIAG_EN pin is disabled.

**Table 2. Fault Truth Table**

| CONDITION | IN | OUT | CRITERION | $\overline{FAULT}$ | FAULT RECOVERY |
|---|---|---|---|---|---|
| Normal | L | L | — | H | — |
| | H | H | — | H | |
| Overload or short to GND | H | L | Current limit triggered. | L | See Table 1. |
| Open load or short to battery | H | H | $I_{OUT} < I_{(ol,on)}$ | L | $\overline{FAULT}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$. OR $\overline{FAULT}$ clears when the open load is removed. |
| | L (1) | H | $V_{VS} - V_{OUT} < V_{(ol,off)}$ | L | $\overline{FAULT}$ clears when IN is toggling OR $\overline{FAULT}$ clears when the open load is removed. |
| Thermal shutdown | H | — | Thermal shutdown triggered | L | $\overline{FAULT}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$. OR $\overline{FAULT}$ clears when thermal shutdown quits. |
| Thermal swing | H | — | Thermal swing triggered | L | $\overline{FAULT}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$. OR $\overline{FAULT}$ clears when thermal swing quits. |

(1) An external pullup is required for open-load detection.

**Table 3. DIAG_EN Disabled Condition**

| DIAG_EN | IN | PROTECTIONS AND DIAGNOSTICS |
|---|---|---|
| LOW | ON | Diagnostics disabled, full protections |
| | OFF | Diagnostics disabled, no protection |

### 7.3.5 Full Diagnostics

#### *7.3.5.1 Short-to-GND and Overload Detection*

When the output is on, a short to GND or an overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, a fault condition is reported out as $\overline{FAULT}$ pin = low.

#### *7.3.5.2 Open-Load Detection*

##### 7.3.5.2.1 Output On

When the output is on, if the current flowing through the output $I_{OUT} < I_{(ol,on)}$, the device recognizes an open-load fault. For open-load detection in output on, no external circuitry is required.

##### 7.3.5.2.2 Output Off

When the output is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{VS} - V_{OUT} < V_{(ol,off)}$), and the device recognizes an open-load fault.

There is always a leakage current $I_{(ol,off)}$ present on the output due to the internal logic control path or external humidity, corrosion, and so forth. So an external pullup resistor is recommended to offset the leakage current when an open load is detected. The recommended pullup resistance is 15 kΩ.

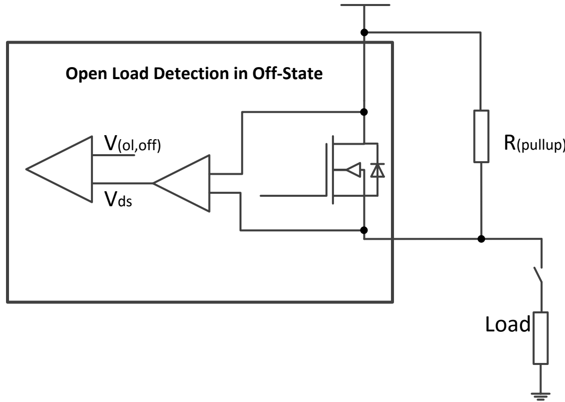



**Figure 22. Open-Load Detection in Output Off**

### *7.3.5.3 Short-to-Battery Detection*

Short-to-battery has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state.

### *7.3.5.4 Thermal Fault Detection*

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing).

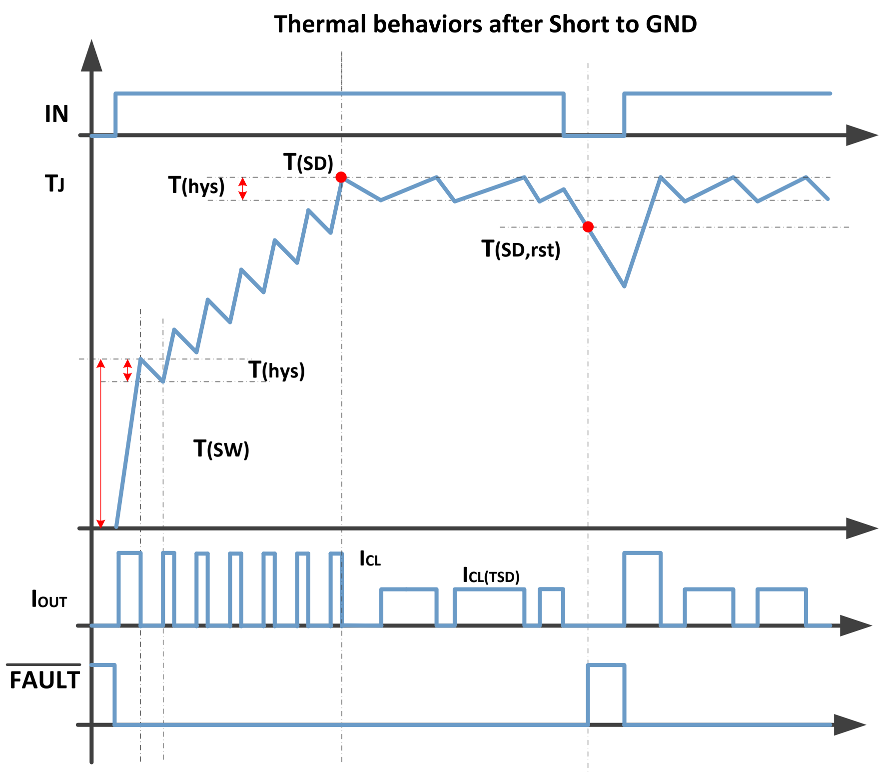



**Figure 23. Thermal Behavior Diagram**

#### 7.3.5.4.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thermal shutdown occurs, the output turns off.

#### 7.3.5.4.2 Thermal Swing

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$. The thermal swing function improves the device reliability when subjected to repetitive fast thermal variation.

#### 7.3.5.4.3 Fault Report Holding

When using PWM dimming, $\overline{FAULT}$ is easily cleared by the PWM falling edge. Even if the fault condition remains all the time, $\overline{FAULT}$ is discontinuous. To avoid this unexpected fault report behavior, the device implements fault-report holding time. Figure 24 shows a typical issue when PWM dimming, the $\overline{FAULT}$ is cleared unexpectedly even when the short-to-GND still exists. The TPS1H000-Q1 device with fault-report holding function allows the right behavior as shown in Figure 25.

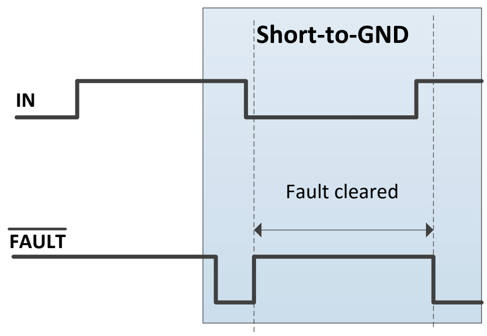



**Figure 24. Without Fault-Report Holding**

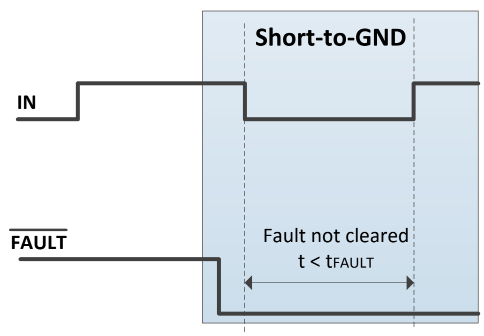



**Figure 25. With Fault-Report Holding**

### 7.3.6 Full Protections

#### *7.3.6.1 UVLO Protection*

The device monitors the supply voltage, $V_{VS}$, to prevent unpredicted behaviors when $V_{VS}$ is too low. When $V_{VS}$ falls down to $V_{VS(uvf)}$, the device shuts down. When $V_{VS}$ rises up to $V_{VS(uvr)}$, the device turns on.

#### *7.3.6.2 Inductive Load Switching Off Clamp*

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

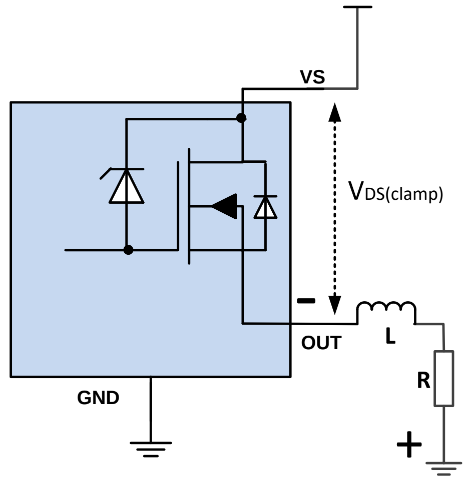



**Figure 26. Drain-to-Source Clamping Structure**

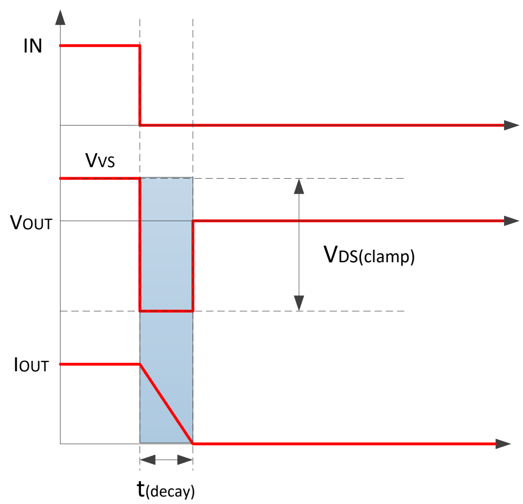



**Figure 27. Inductive-Load Switching-Off Diagram**

#### *7.3.6.3 Loss-of-GND Protection*

When loss of GND occurs, the output is shut down regardless of whether the IN pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

#### *7.3.6.4 Loss-of-Power-Supply Protection*

When loss of supply occurs, the output is shut down regardless of whether the IN pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the logic control pins to maintain the inductance current. To protect the system in this condition, TI recommends protection with an external free-wheeling diode.

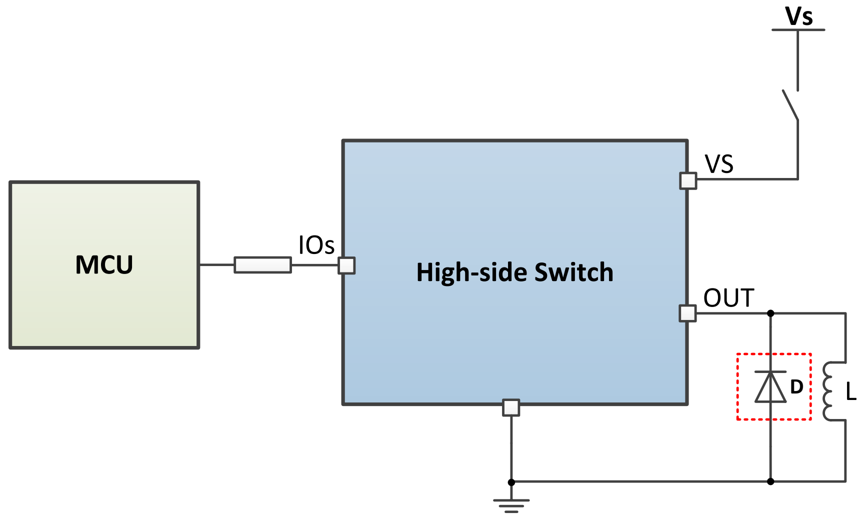



**Figure 28. Protection for Loss of Power Supply**

#### *7.3.6.5 Reverse-Current Protection*

Reverse current occurs in two conditions: short to supply and reverse polarity.

- When a short to the supply occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode (method 1). Both the device and load are protected when in reverse polarity.
- Adding a GND network (method 2). The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended configuration is a 1-kΩ resistor in parallel with a >100-mA diode. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.

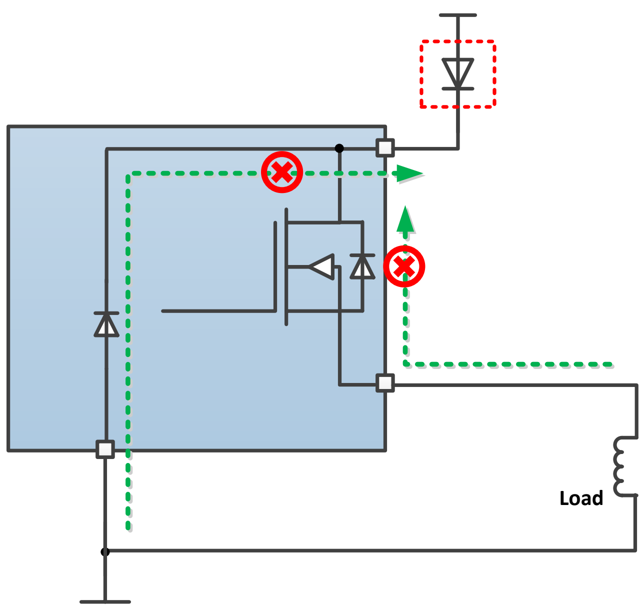



**Figure 29. Reverse-Current External Protection, Method 1**

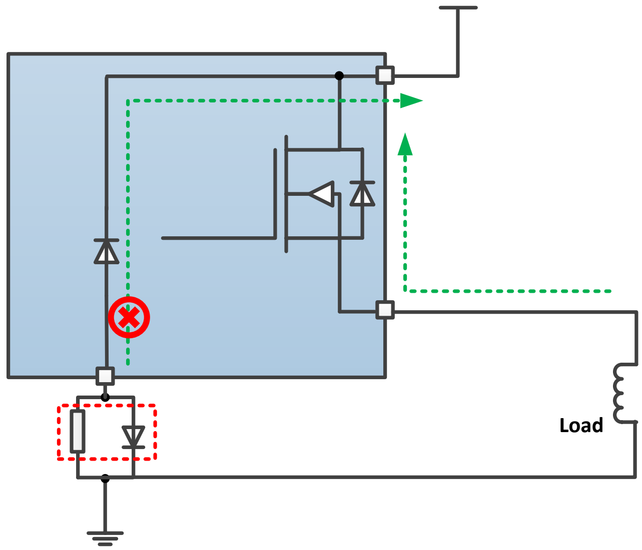



**Figure 30. Reverse-Current External Protection, Method 2**

#### *7.3.6.6 MCU I/O Protection*

TI recommends series resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.

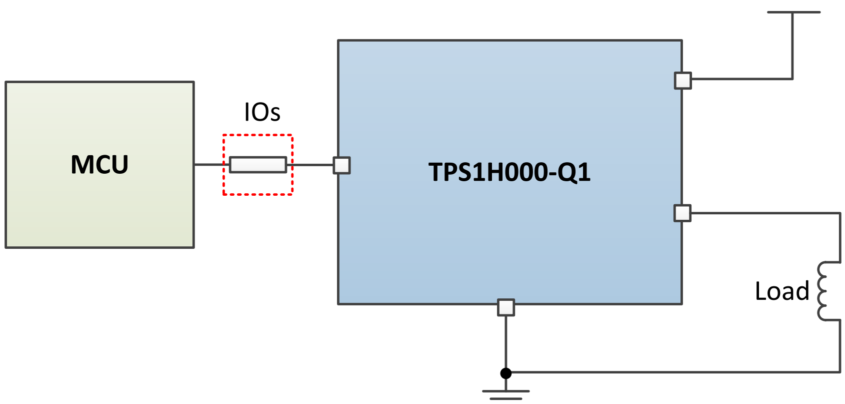



**Figure 31. MCU I/O External Protection**

## 7.4 Device Functional Modes

### 7.4.1 Working Modes

The device has three working modes, the normal mode, the standby mode, and the standby mode with diagnostics, as shown in Figure 32.

## Device Functional Modes (continued)

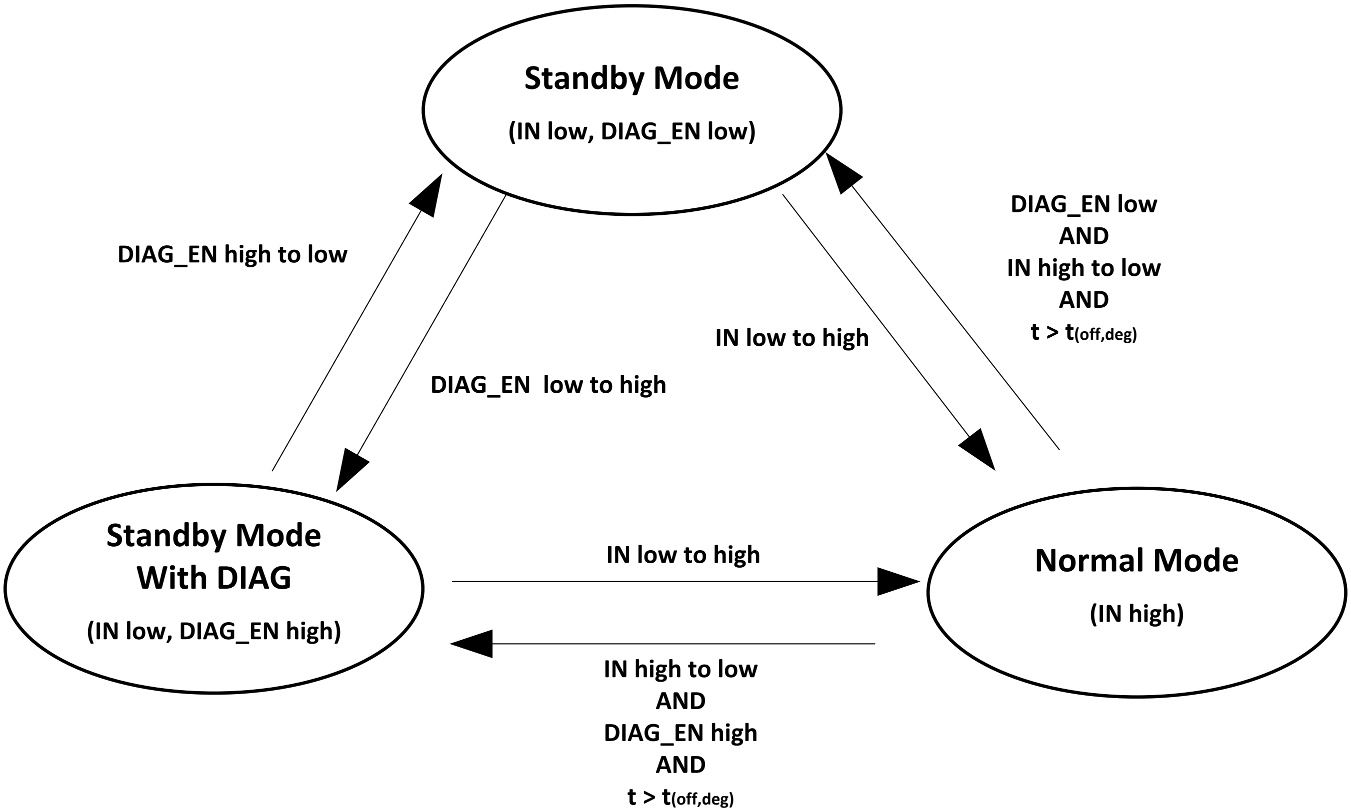



**Figure 32. Working Modes**

#### *7.4.1.1 Normal Mode*

When IN is high, the device enters normal mode.

#### *7.4.1.2 Standby Mode*

When IN is low and DIAG_EN is low, the device enters standby mode with ultralow power consumption.

#### *7.4.1.3 Standby Mode With Diagnostics*

When IN is low and DIAG_EN is high, the device enters standby mode with diagnostics. The device still supports open-load and short-to-battery detection even when IN is low.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS1H000-Q1 device is a smart high-side switch, with an internal charge pump and single-channel integrated NMOS power FET. The adjustable current-limit function greatly improves the reliability of the whole system. Full diagnostic features enable intelligent control of the load. The TPS1H000-Q1 device can be used for a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and sub-modules.

## 8.2 Typical Application

Figure 33 shows an example of how to design the external circuitry parameters.

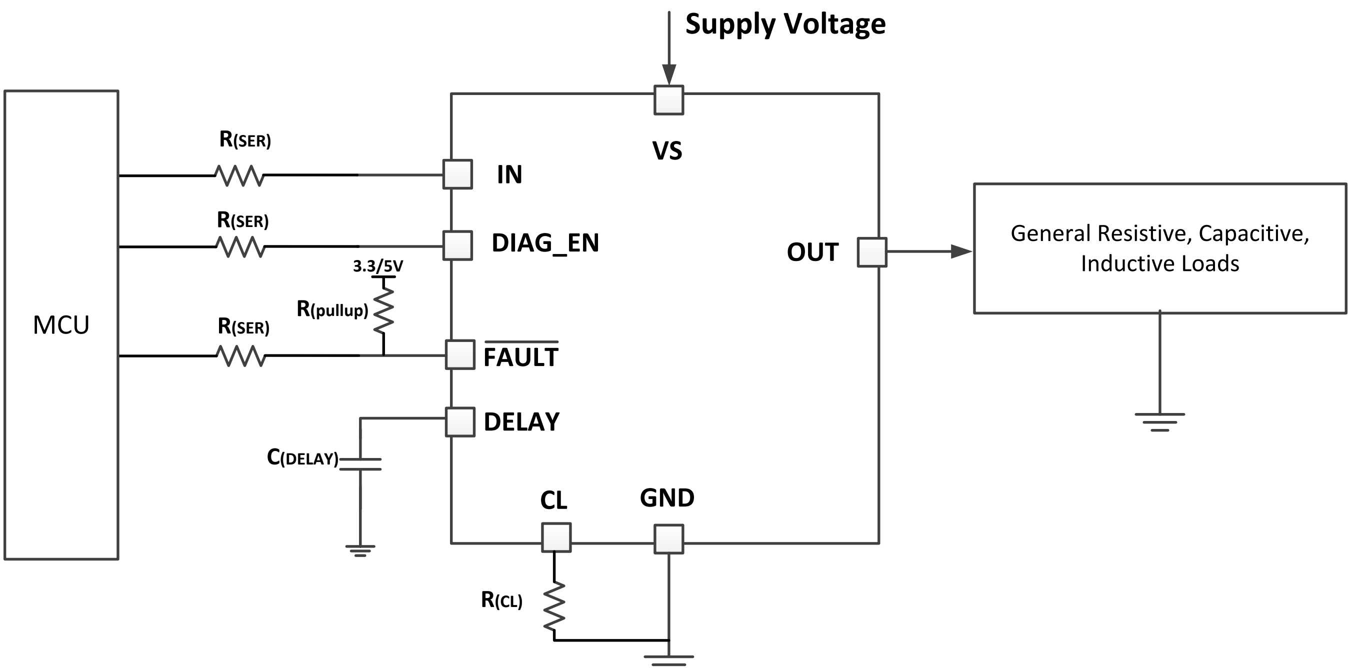



**Figure 33. Typical Application Circuitry**

### 8.2.1 Design Requirements

- $V_{VS}$ range from 6 V to 18 V
- Nominal current of 100 mA
- Expected current limit value of 500 mA
- Thermal sensitive system, when current limit occurs, the output latches off after 0.2 s. The 0.2 s is to ensure the safe start-up for a capacitive load, clamping the inrush current but without latch-off during start-up.
- Full diagnostics with 5-V MCU, including on-state open-load detection, short-to-GND or overcurrent detection, and thermal shutdown detection

### 8.2.2 Detailed Design Procedure

To set the adjustable current limit value at 500 mA, calculate $R_{(CL)}$ as follows:

## Typical Application (continued)

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 600}{0.5} = 960\ \Omega \tag{3}$$

To set the adjustable latch-off delay at 0.2 s, calculate $C_{(DELAY)}$ as follows:

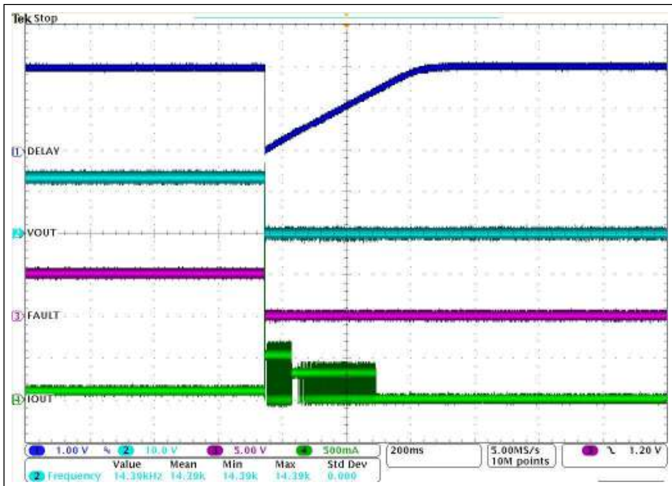
$$t_{dl} = t_{CL(deg)} + t_{dl1} + t_{dl2} = 0.2 \approx t_{dl2}$$

$$C_{DELAY} = \frac{I_{dl(chg)} \times t_{dl2}}{V_{dl(ref)}} = \frac{4.5 \times 0.2}{1.45} \times 10^{-6} = 0.62\ \mu F \tag{4}$$

TI recommends $R_{(SER)}$ = 10 kΩ for a 5-V MCU, and $R_{(pullup)}$ = 10 kΩ as the pullup resistor.

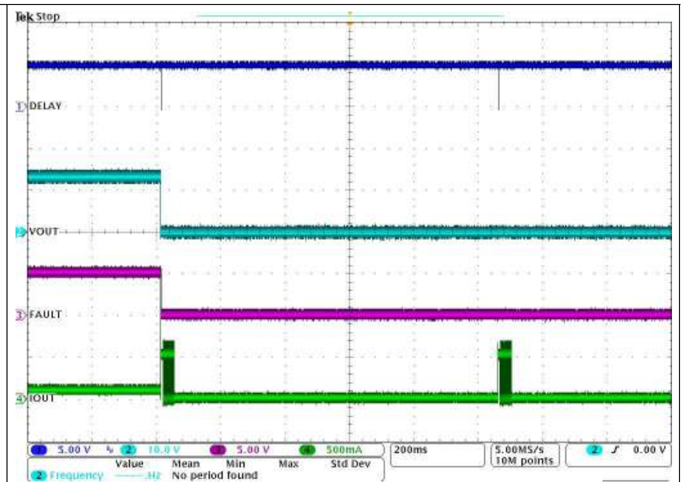
### 8.2.3 Application Curves

The following curves are test examples of hard short conditions. The load is 0.1 A and the current limit value is 0.5 A. Figure 34 shows a waveform of the latch-off mode. Figure 35 shows a waveform of the auto-retry mode.




Load = 0.1 A Current limit = 0.5 A

**Figure 34. Hard-Short Condition in Latch-Off Mode**




Load = 0.1 A Current limit = 0.5 A

**Figure 35. Hard-Short Condition in Auto-Retry Mode**

# 9 Power Supply Recommendations

The device can be used for both 12-V and 24-V applications. The normal power supply connection is a 12-V or 24-V system.

# 10 Layout

## 10.1 Layout Guidelines

To prevent thermal shutdown, $T_J$ must be less than 175°C. If the output current is very high, the power dissipation may be large. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package thermal pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

## 10.2 Layout Example

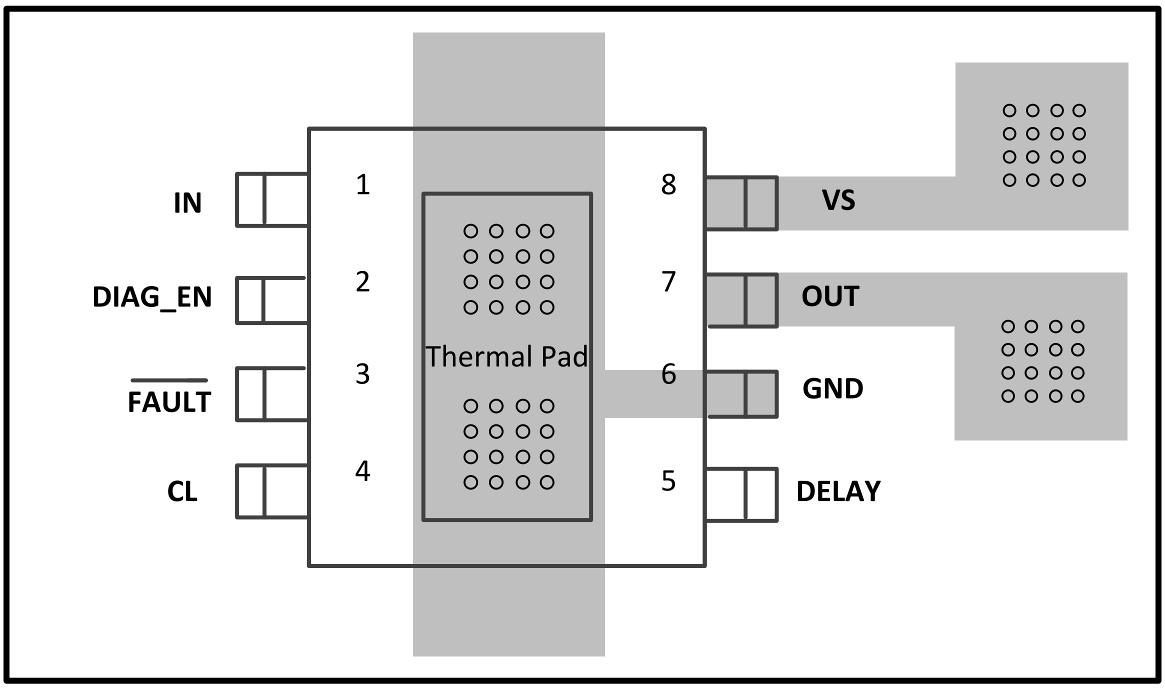



**Figure 36. Layout Example**

# 11 Device and Documentation Support

## 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS1H000AQDGNRQ1 | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 17SX | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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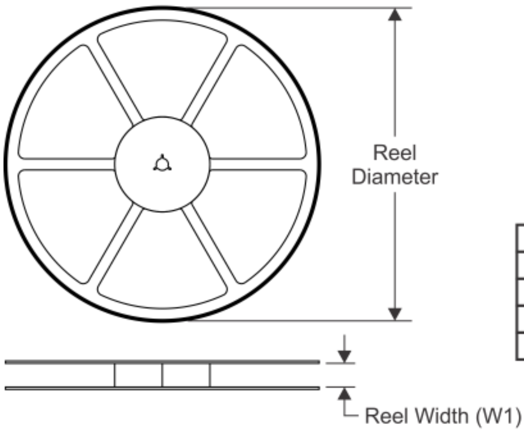
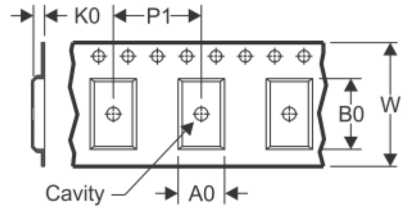
## TAPE AND REEL INFORMATION

REEL DIMENSIONS

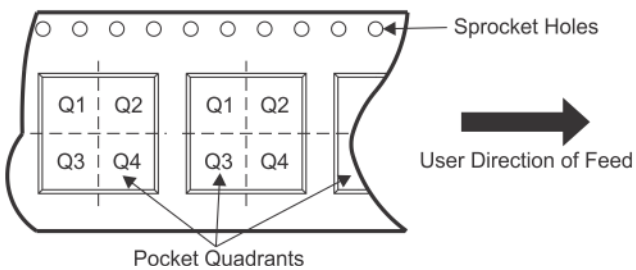



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

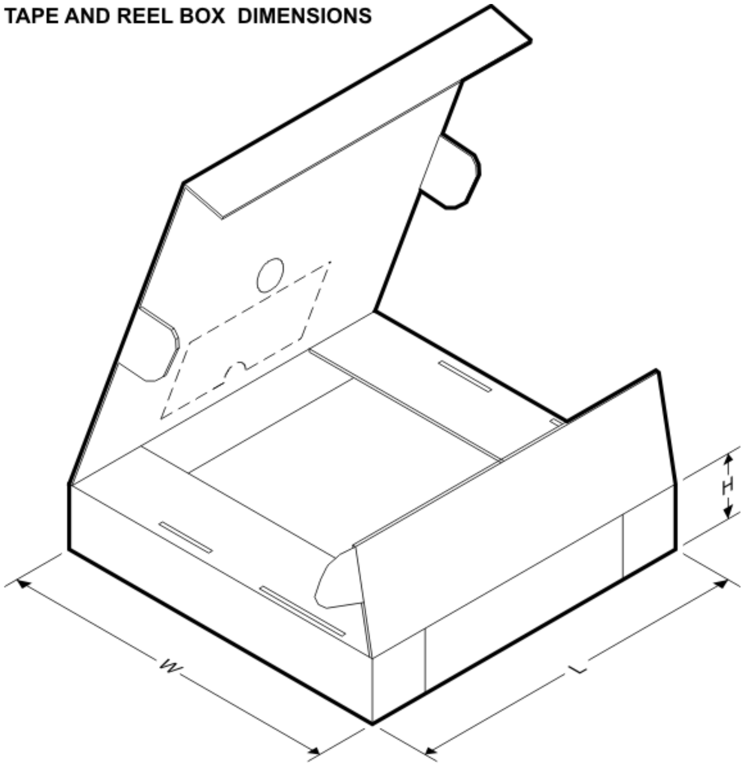
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS1H000AQDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

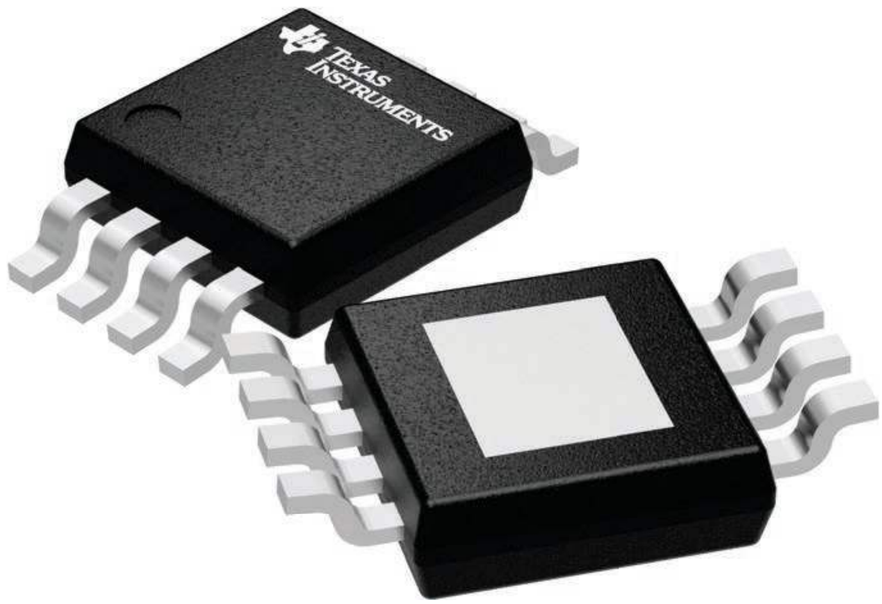
TAPE AND REEL BOX DIMENSIONS

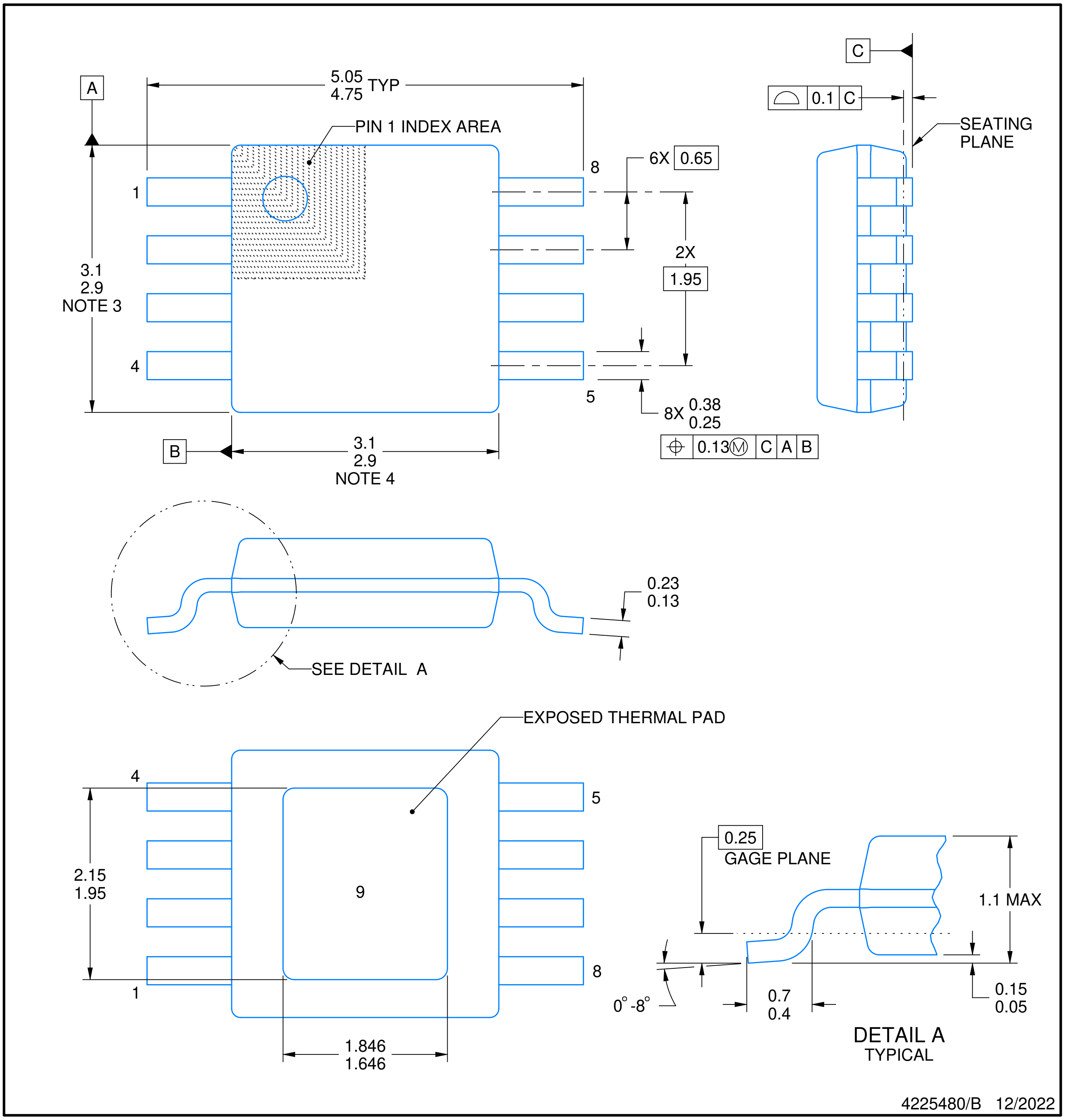



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS1H000AQDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 366.0 | 364.0 | 50.0 |

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

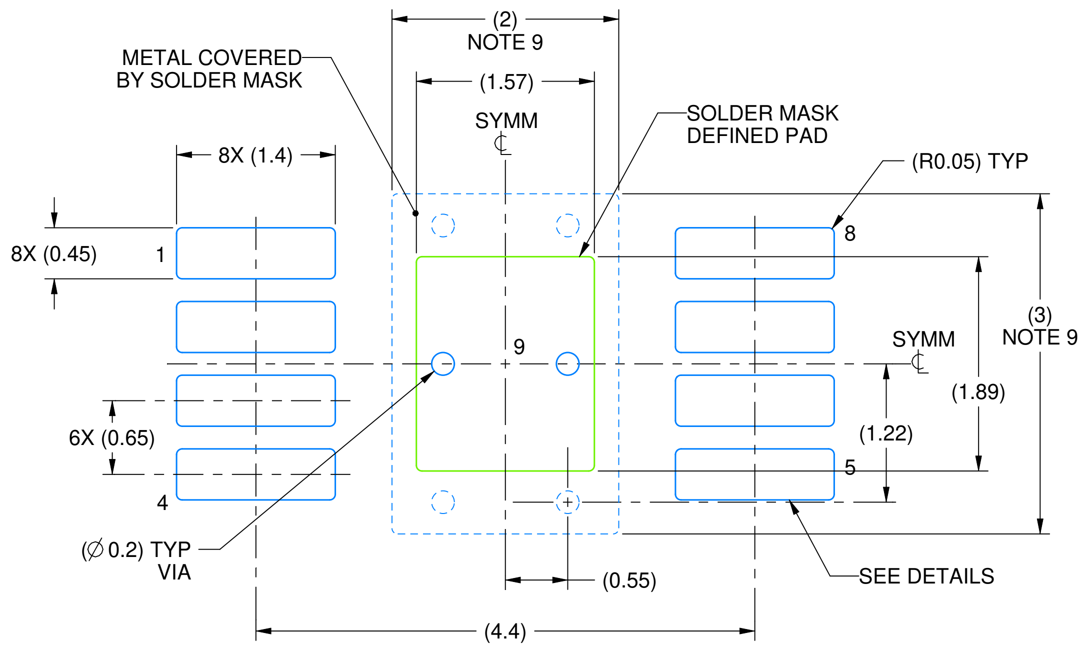




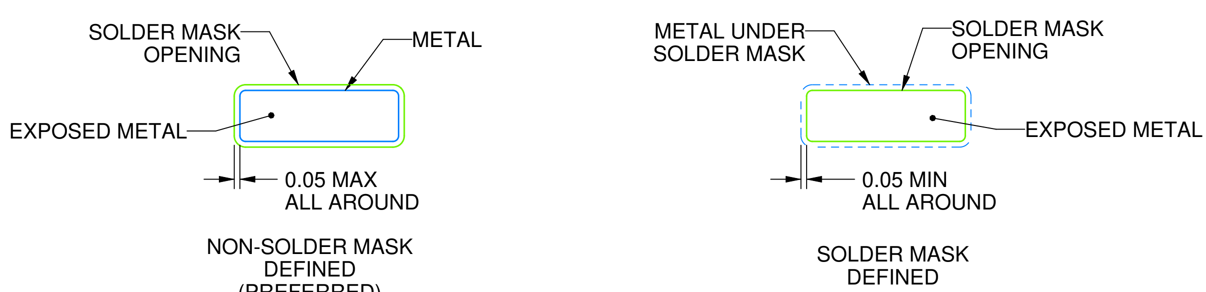

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

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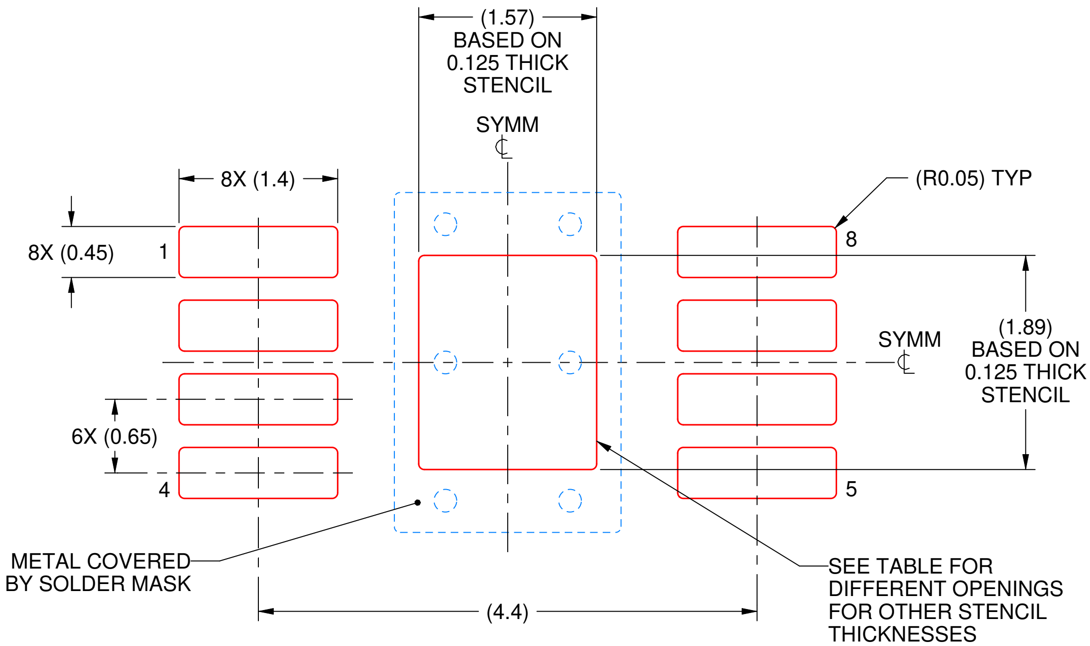
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 1.76 X 2.11 |
| 0.125 | 1.57 X 1.89 (SHOWN) |
| 0.15 | 1.43 X 1.73 |
| 0.175 | 1.33 X 1.60 |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.