Arria V GT FPGA Development Kit

User Guide

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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Contents

Chapter 1. About This Kit

Kit Features . . . 1–1
Hardware . . . 1–1
Software . . . 1–1
Quartus II Software . . . 1–1
Arria V GT FPGA Development Kit Installer . . . 1–2

Chapter 2. Getting Started

Before You Begin . . . 2–1
Inspect the Boards . . . 2–1
References . . . 2–2

Chapter 3. Software Installation

Installing the Quartus II Subscription Edition Software . . . 3–1
Licensing Considerations . . . 3–1
Installing the Development Kit . . . 3–3
Installing the USB-Blaster II Driver . . . 3–4

Chapter 4. Development Board Setup

Setting Up the Board . . . 4–1
Factory Default Switch and Jumper Settings . . . 4–2

Chapter 5. Board Update Portal

Connecting to the Board Update Portal Web Page . . . 5–1
Using the Board Update Portal to Update User Designs . . . 5–2

Chapter 6. Board Test System

Preparing the Board . . . 6–2
Running the Board Test System . . . 6–3
Using the Board Test System . . . 6–3
The Configure Menu . . . 6–3
The System Info Tab . . . 6–4
Board Information . . . 6–4
MAX II Registers . . . 6–4
JTAG Chain . . . 6–5
The GPIO FPGA 1 Tab . . . 6–6
Character LCD . . . 6–6
User DIP Switch . . . 6–7
User LEDs . . . 6–7
Push Button Switches . . . 6–7
The Flash Tab . . . 6–7
Read . . . 6–8
Write . . . 6–8
Random Test . . . 6–8
CFI Query . . . 6–8
Increment Test . . . 6–8
Reset . . . 6–8
Erase . . . 6–8

Flash Memory Map 6–8
The HSMA Tab 6–9
Status 6–9
Port (FPGA1) 6–10
PMA Setting 6–10
Data Type 6–10
Error Control 6–11
Start 6–11
Stop 6–11
Loopback 6–11
The SFP/SMA/C2C Tab 6–12
Status 6–12
Port (FPGA1) 6–13
PMA Setting 6–13
Data Type 6–13
Error Control 6–14
Loopback 6–14
Start 6–14
Stop 6–14
The HSMB/FMC Tab 6–15
Status 6–15
Port (FPGA2) 6–16
PMA Setting 6–16
Data Type 6–16
Error Control 6–17
Loopback 6–17
Start 6–17
Stop 6–17
The SDI/Bull's Eye Tab 6–18
Status 6–18
Port (FPGA2) 6–19
PMA Setting 6–19
Data Type 6–19
Error Control 6–20
Loopback 6–20
Start 6–20
Stop 6–20
The SMA Tab 6–21
Status 6–21
Port (FPGA2) 6–22
PMA Setting 6–22
Data Type 6–22
Error Control 6–23
Start 6–23
Stop 6–23
Loopback 6–23
The Power Monitor 6–23
General Information 6–24
Power Information 6–25
Power Graph 6–25
Graph Settings 6–25
Reset 6–25
Calculating Power 6–25
The Clock Control 6–26

Registers 6–27
Frequency (MHz) 6–27
Disable 6–27
Default 6–27
Set New Frequency 6–27
Configuring the FPGA Using the Quartus II Programmer 6–27
Samtec High-speed Bull's Eye Connector 6–28

Appendix A. Programming the Flash Memory Device

CFI Flash Memory Map A–1
Preparing Design Files for Flash Programming A–2
Creating Flash Files Using the Nios II EDS A–2
Programming Flash Memory Using the Board Update Portal A–2
Programming Flash Memory Using the Nios II EDS A–3
Restoring the Flash Device to the Factory Settings A–4
Restoring the MAX II CPLD to the Factory Settings A–5

Additional Information

Document Revision History Info–1
How to Contact Altera Info–1
Typographic Conventions Info–1

1. About This Kit

The Altera® Arria® V GT FPGA Development Kit is a complete design environment that includes both the hardware and software you need to develop Arria V GT FPGA designs.

Kit Features

This section briefly describes the Arria V GT FPGA Development Kit contents.

Hardware

The Arria V GT FPGA Development Kit includes the following hardware:

- Arria V GT FPGA development board—A development platform that allows you to develop and prototype hardware designs running on the Arria V GT 5AGTFD7K3F40N FPGA.

  For detailed information about the board components and interfaces, refer to the *Arria V GT FPGA Development Board Reference Manual*.

- HSMC loopback daughtercard
- HSMC debug daughtercard
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable
  - Samtec high-speed Bull’s Eye kit with 22-position connector, four SMA cables and tool

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

☞ After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software. For more information, refer to the Design Software page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

  ☞ The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor, which you can include in your Altera FPGA designs.

Arria V GT FPGA Development Kit Installer

The license-free Arria V GT FPGA Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to "Software Installation" on page 3–1.

2. Getting Started

The remaining chapters in this user guide lead you through the following Arria V GT FPGA development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the FPGA development board
- Configuring the Arria V GT FPGAs
- Running the Board Test System designs

For complete information about the FPGA development board, refer to the *Arria V GT FPGA Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the boards to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Boards

To inspect each board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components on the board appear in place and intact.

☞ In typical applications with the Arria V GT FPGA development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGAs that accommodate many different heat sinks, including the Dynatron CHR-152. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA power in real time, refer to "The Power Monitor" on page 6–23.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Arria V GT FPGA Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Arria V GT device documentation, refer to the Documentation: Arria V Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Arria V GT OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Arria V GT FPGA Development Kit
- USB-Blaster™ II driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools used for developing hardware and software for Altera devices. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Choosing an installation directory that is relative to the Quartus II software installation directory, follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing Manual*.

Licensing Considerations

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

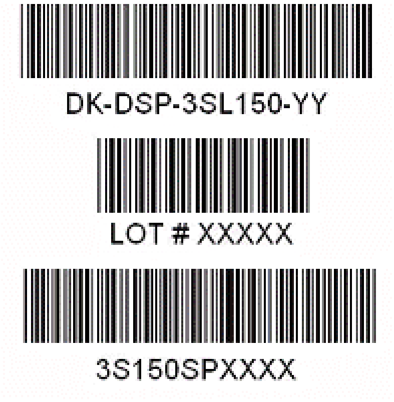
Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. Figure 3–1 shows *3S150SPXXXX* as an example serial number.

Figure 3–1. Locating Your Serial Number



2. Consult the Activate Products table, to determine how to proceed.
   a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
   b. If the administrator listed for your product is you, proceed to step 3.
   c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus_II software to enable the software.

For complete licensing details, refer to *Altera Software Installation and Licensing Manual*.

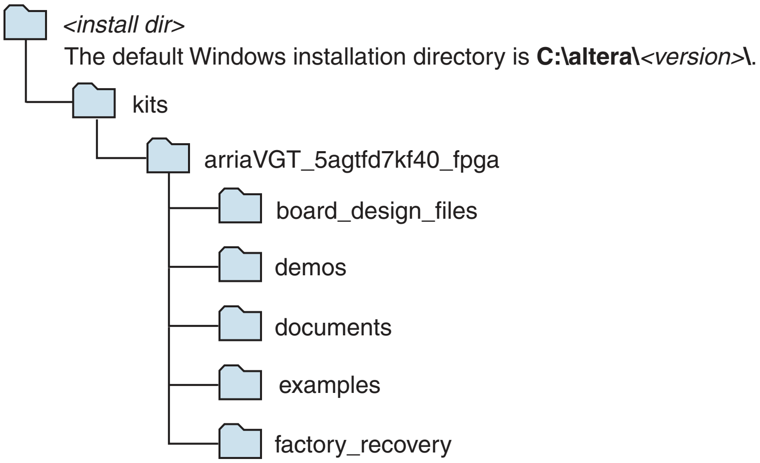
Installing the Development Kit

To install the Arria V GT FPGA Development Kit, perform the following steps:

1. Download the Arria V GT FPGA Development Kit installer from the Arria V GT FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Run the Arria V GT FPGA Development Kit installer.
3. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the Arria V GT FPGA Development Kit directory structure shown in Figure 3–2.

Figure 3–2. Arria V GT FPGA Development Kit Installed Directory Structure [(1)]


<install dir>
The default Windows installation directory is **C:\altera\**<*version*>\.
kits
arriaVGT_5agtfd7kf40_fpga
board_design_files
demos
documents
examples
factory_recovery

Note to Figure 3–2:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications, if present.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Arria V GT FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Arria V GT FPGA development board includes integrated On-Board USB-Blaster II circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster II driver on the host computer.

Installation instructions for the USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

4. Development Board Setup

The instructions in this chapter explain how to set up the Arria V GT FPGA development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Arria V GT FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch and Jumper Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The development board ships with design examples stored in the flash memory device. Verify the Load Selector (SW5.3) is in the on (factory) position to load the design stored in the factory portion of flash memory. Figure 4–1/Figure 4–2 shows the switch locations on the Arria V GT FPGA development board.
3. Connect the +19 V, 6.32 A to the DC Power Jack (J6) on the FPGA board and plug the cord into a power outlet.

   CAUTION Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage, and a lower-rated power supply may not be able to provide enough power for the board.

4. Set the POWER switch (SW1) to the on position. When power is supplied to the board, blue LED (D1) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The Load Selector (SW5.3) controls which design to load. When the switch is in the on (factory) position, the PFL loads the design from the factory portion of flash memory.

☞ The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\examples\max2** directory.

When configuration is complete, the Config Done LED (D16) illuminates, signaling that the Arria V GT device configured successfully.

For more information about the PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch and Jumper Settings

This section shows the factory switch and jumper settings for the Arria V GT FPGA development board. Figure 4–1 shows the switch and jumper locations and the default position of each switch and jumper on the top side of the board.

Figure 4–1. Switch Locations and Default Settings on the Board Top

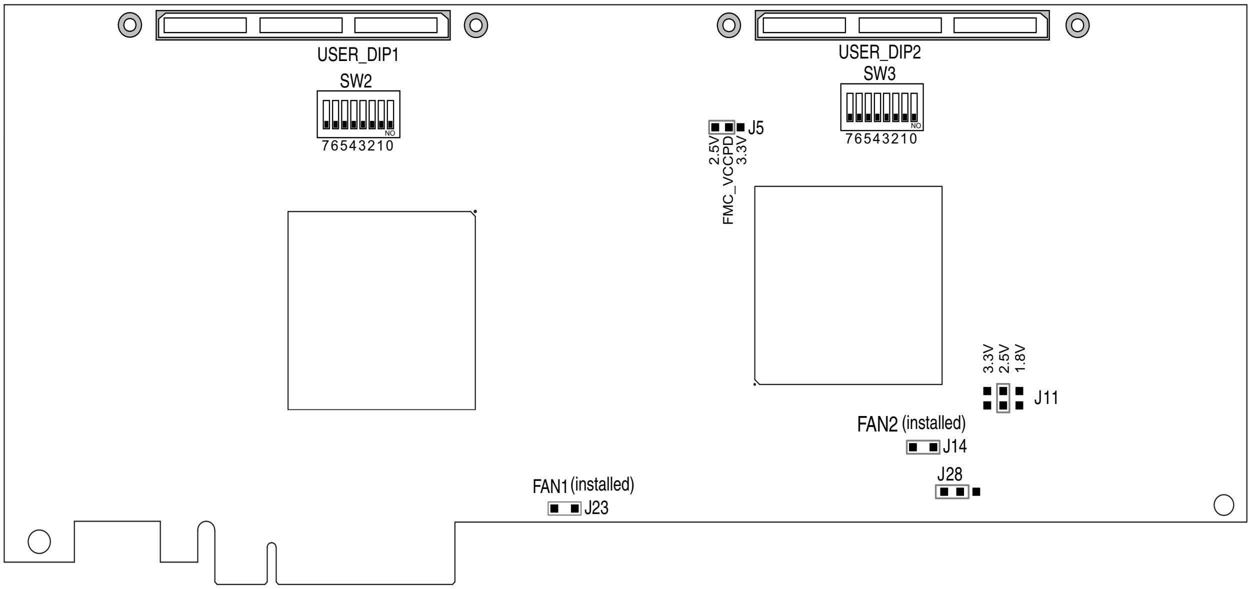
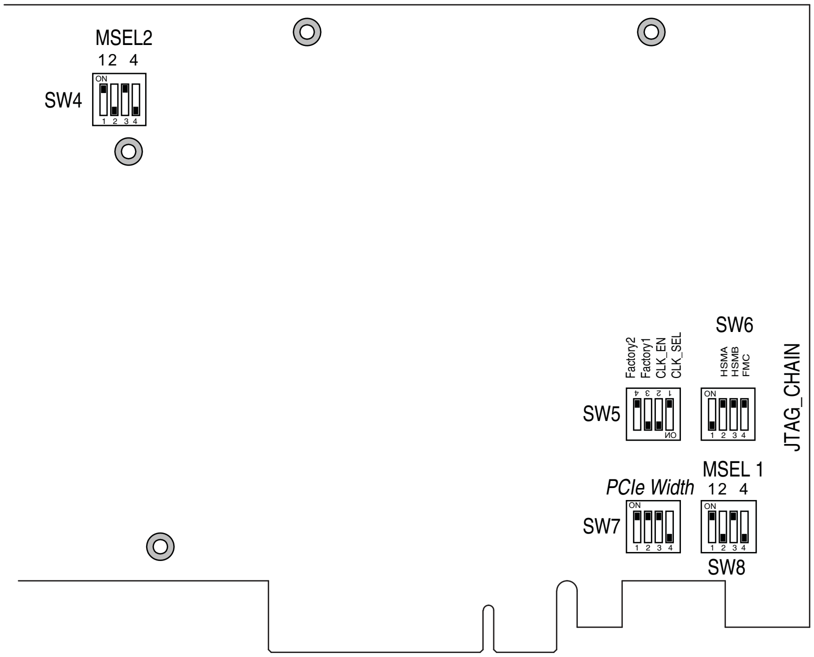


Figure 4–2 shows the switch locations and the default position of each switch on the bottom side of the board.

Figure 4–2. Switch Locations and Default Settings on the Board Bottom



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (SW4) to match Table 4–1 and Figure 4–2.

Table 4–1. SW4 FPGA2 MSEL Dip Switch Settings [(1)]

Switch	Board Label	Function	Default Position
1	FPGA2_MSEL[1]	Switch 1 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	ON
2	FPGA2_MSEL[2]	Switch 2 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF
3	—	—	ON
4	FPGA2_MSEL[4]	Switch 4 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF

Note to: Table 4–1

(1) Ensure that all MSEL setting are in a defined configuration scheme as shown in Volume 2: Device Interfaces and Integration of the *Arria V Device Handbook*.

2. Set DIP switch bank (SW5) to match Table 4–2 and Figure 4–2.

Table 4–2. SW5 Board Settings Dip Switch

Switch	Board Label	Function	Default Position
1	CLK_SEL	Switch 1 has the following options: ■ ON, (logical 0) = SMA input clock select. ■ OFF, (logical 1) = programmable oscillator clock select.	OFF
2	CLK_EN	Switch 2 has the following options: ■ ON, (logical 0) = on-board oscillator disable. ■ OFF, (logical 1) = on-board oscillator enable.	ON
3	Factory1	Switch 3 has the following options: ■ ON, (logical 0) = load the factory design for Arria V FPGA 1 from flash at power up. ■ OFF, (logical 1) = load the user design for Arria V FPGA 1 from flash at power up.	ON
4	Factory2	Switch 4 is for factory test only.	OFF

3. Set DIP switch bank (SW6) to match Table 4–3 and Figure 4–2.

Table 4–3. SW6 JTAG Dip Switch Settings

Switch	Board Label	Function	Default Position
1	—	—	OFF
2	HSMA_JTAG_EN	Switch 2 has the following options: ■ ON, (logical 0) = HCMC Port A not in JTAG chain. ■ OFF, (logical 1) = Include HCMC Port A in the JTAG chain.	ON
3	HSMB_JTAG_EN	Switch 3 has the following options: ■ ON, (logical 0) = HCMC Port B not in JTAG chain. ■ OFF, (logical 1) = Include HCMC Port B in the JTAG chain.	ON
4	FMC_JTAG_EN	Switch 4 has the following options: ■ ON, (logical 0) = FMC connector not in JTAG chain. ■ OFF, (logical 1) = Include FMC connector in the JTAG chain.	ON

4. Set DIP switch bank (SW7) to match Table 4–4 and Figure 4–2.

Table 4–4. SW7 PCIe DIP Switch Settings

Switch	Board Label	Function	Default Position
1	PCIE_PRSNT2n_x1	Switch 1 has the following options: ■ ON (0) = x1 presence detect is enabled. ■ OFF (1) = x1 presence detect is disabled.	ON
2	PCIE_PRSNT2n_x4	Switch 2 has the following options: ■ ON (0) = x4 presence detect is enabled. ■ OFF (1) = x4 presence detect is disabled.	ON
3	PCIE_PRSNT2n_x8	Switch 3 has the following options: ■ ON (0) = x8 presence detect is enabled. ■ OFF (1) = x8 presence detect is disabled.	ON
4	—	—	OFF

5. Set DIP switch bank (SW8) to match Table 4–5 and Figure 4–2.

Table 4–5. SW8 FPGA1 MSEL Dip Switch Settings *(1)*

Switch	Board Label	Function	Default Position
1	FPGA1_MSEL[1]	Switch 1 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	ON
2	FPGA1_MSEL[2]	Switch 2 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF
3	—	—	ON
4	FPGA1_MSEL[4]	Switch 4 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF

Note to: Table 4–5

(1) Ensure that all MSEL setting are in a defined configuration scheme as shown in Volume 2: Device Interfaces and Integration of the *Arria V Device Handbook*.

6. Set the board jumpers to match Table 4–6, Figure 4–1 and Figure 4–2.

Table 4–6. Jumper Settings (Part 1 of 2)

Board Reference	Board Label	Function	Default Position
J5	FMC_VCCPD	This jumper has the following options: ■ Installing the shunt on pins 1-2 provides 2.5 V on FMC_VCCPD. ■ Installing the shunt on pins 2-3 provides 3.3 V on FMC_VCCPD. ⚠ CAUTION J5 (VCCPD setting) must be set according the to voltage supplied by the FMC card to avoid damaging your development board.	Pins 1-2
J11	FMC_VCCIO_SEL	This jumper has the following options: ■ No shunt = 1.5V ■ Shunt on pins 1-2 = 1.8V ■ Shunt on pins 3-4 = 2.5V ■ Shunt on pins 5-6 = 3.3V Note: When setting this jumper to 3.3 V, make sure the FMC_VCCPD is on the correct setting (J5 shunt on pins 2-3).	Pins 3-4
J14	FAN2	Powers the fan for FPGA 2.	Installed

Table 4–6. Jumper Settings (Part 2 of 2)

Board Reference	Board Label	Function	Default Position
J28	FMC_VCCIO_SRC	This jumper has the following options: ■ Installing the shunt on pins 1-2 powers bank 4B when there is no FMC card installed or the FMC card does not provide a voltage for this rail. The voltage on this depends on the voltage selected on J11. ■ Installing the shunt on pins 2-3 powers bank 4B when an FMC card is installed and provides the power needed for this bank. The max voltage on this is 3.3 V. Do not install an FMC with a higher rated card. Note: FMC is not available for rev. A boards.	Pins 1-2
J23	FAN1	Powers the fan for FPGA 1.	Installed

For more information about the FPGA board settings, refer to the *Arria V GT FPGA Development Board Reference Manual*.

5. Board Update Portal

The Arria V GT FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the Load Selector (SW5.3) in the on (factory) position, the Arria V GT FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 and hardware 2 portion of flash memory and provides useful kit-specific links and design resources.

☞ After successfully updating the user hardware 1 and/or hardware 2 flash memory, you can load the user design from flash memory into the FPGA. To do so, set the Load Selector (SW5.3) to the off (user) position and power cycle the board. (The design stored in user hardware 1 is used to configure FPGA 1 when the board is power cycled.) To configure FPGA 1 with the design stored in user hardware 2, push and release the PGM1 (S2) push button the required number of times until PGM2 LED lights and then push PGM_CONF (S3) to configure the FPGA.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

☞ Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. With the board powered down, set the Load Selector (SW5.3) to the on (factory) position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router and obtains an IP address. The LCD on the board displays the IP address.

4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   ☞ You can click *Arria V GT FPGA Development Kit* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the Arria V GT FPGA Development Kit page to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 and user hardware 2 portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

☞ Design files available from the Arria V GT FPGA Development Kit page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field; otherwise, leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete. The file takes about 20 seconds to upload.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the Load Selector (SW5.3) to the off (user) position, and power cycle the board (SW1).

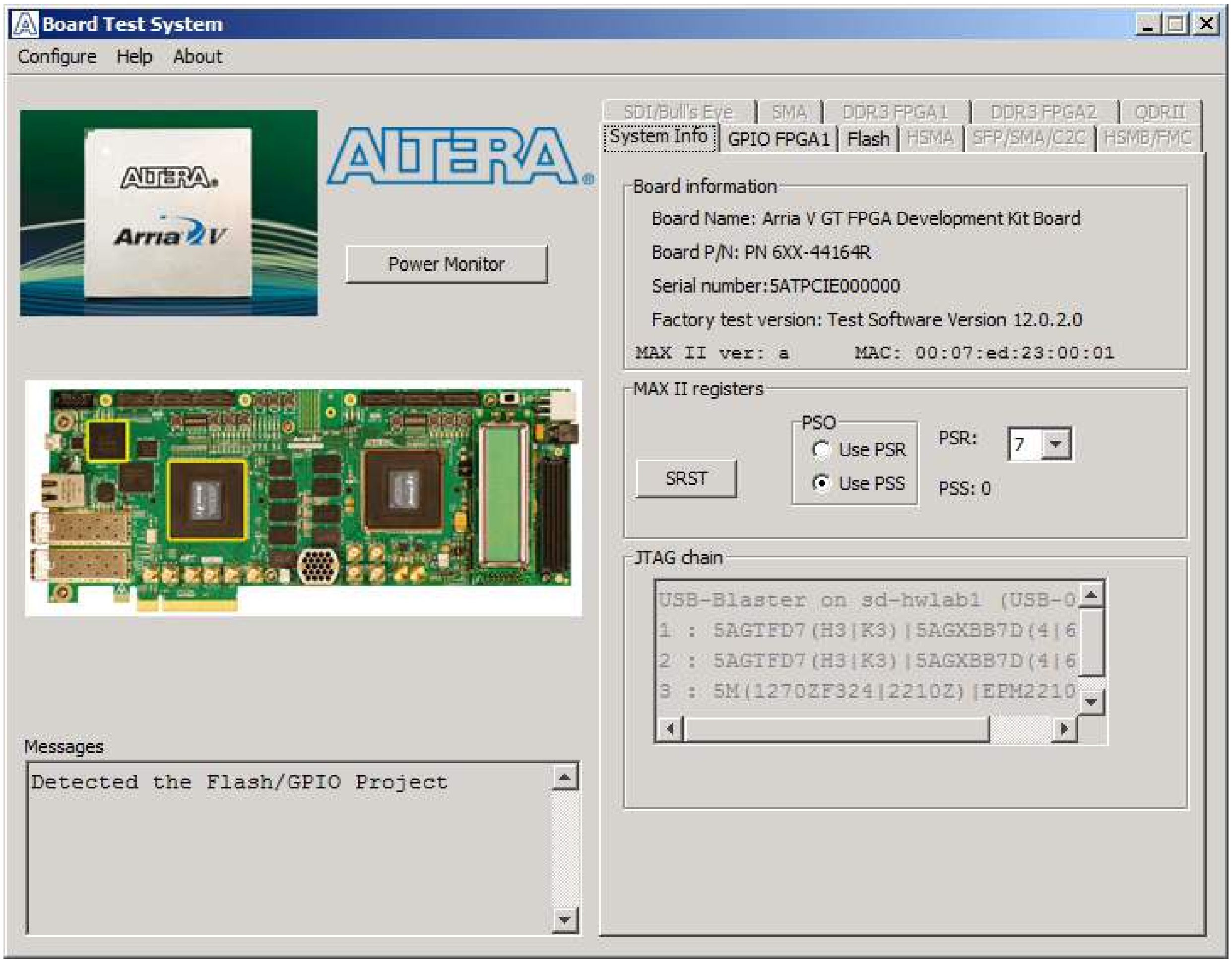
☞ As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 and/or user hardware 2 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

6. Board Test System

The kit includes a design example and an application called the Board Test System (BTS) to test the functionality of the Arria V GT FPGA development board and supported daughtercards. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing. The BTS is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Development Kit" on page 3–3.

The Board Test System GUI communicates over the JTAG bus to a test design running in the Arria V GT device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Board Name: Arria V GT FPGA Development Kit Board

Board P/N: PN 6XX-44164R

Serial number:5ATPCIE000000

Factory test version: Test Software Version 12.0.2.0

MAX II ver: a MAC: 00:07:ed:23:00:01

○ Use PSR

● Use PSS

PSR: 7

PSS: 0

```
USB-Blaster on sd-hwlab1 (USB-0
1  :  5AGTFD7(H3|K3)|5AGXBB7D(4|6
2  :  5AGTFD7(H3|K3)|5AGXBB7D(4|6
3  :  5M(1270ZF324|2210Z)|EPM2210
```

```
Detected the Flash/GPIO Project
```

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

☞ To use the Power Monitor GUI, the MAX II device needs to be programmed with the default factory MAX II design.

☞ The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, follow these steps:

1. Connect the USB cable to the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ45 connector.
3. Ensure that the development board switches and jumpers are set to the default positions as shown in the "Factory Default Switch and Jumper Settings" section starting on page 4–2.
4. Set the Load Selector (SW5.3) to the off (user) position.

   For more information about the board's DIP switch and jumper settings, refer to the *Arria V GT FPGA Development Board Reference Manual*.

5. Turn on the power to the board. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO, Ethernet, and flash memory tests.

   CAUTION To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

☞ On Windows, click **Start** > **All Programs** > **Altera** > **Arria V GT FPGA Development Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Arria V GT FPGA development board's flash memory ships preconfigured with the design that corresponds to the GPIO tab.

☞ If you power up your board with your own design programmed into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

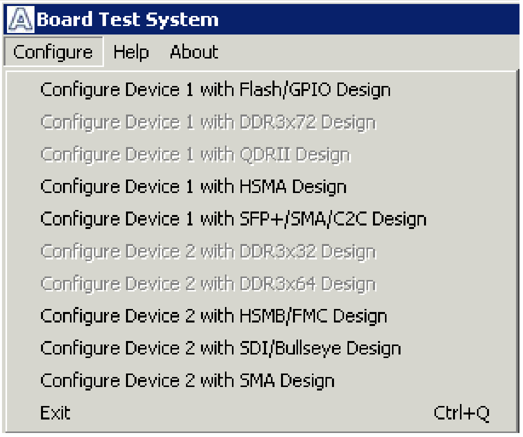
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Use the Configure menu (Figure 6–2) to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 6–2. The Configure Menu


Board Test System
Configure
Help
About
Configure Device 1 with Flash/GPIO Design
Configure Device 1 with DDR3x72 Design
Configure Device 1 with QDRII Design
Configure Device 1 with HSMA Design
Configure Device 1 with SFP+/SMA/C2C Design
Configure Device 2 with DDR3x32 Design
Configure Device 2 with DDR3x64 Design
Configure Device 2 with HSMB/FMC Design
Configure Device 2 with SDI/Bullseye Design
Configure Device 2 with SMA Design
Exit
Ctrl+Q

To configure the FPGA with a test system design, perform the following steps:

1. Make sure there are no conflicts between the Quartus II software version and the Board Test System GUI version.

2. On the Configure menu, click the configure command that corresponds to the functionality you wish to test. The design begins running in the FPGA, and the corresponding GUI application tabs that interface with the design are now enabled.

   ☞ If you use the Quartus II Programmer for configuration, rather than the Board Test System GUI, you may need to restart the GUI.

The System Info Tab

The **System Info** tab shows the board's current configuration. Figure 6–1 on page 6–1 shows the **System Info** tab. The tab displays the contents of the MAX II registers, the JTAG chain, the board's MAC address, and other details stored on the board.

The following sections describe the controls on the **System Info** tab.

Board Information

The **Board information** controls display static information about your board.

- **Board Name**—Indicates the official name of the board, given by the Board Test System.
- **Board P/N**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **MAX II ver**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\examples** directory. Newer revisions of this code might be available on the Arria V GT FPGA Development Kit page of the Altera website.
- **MAC**—Indicates the MAC address of the board.

MAX II Registers

The **MAX II registers** control allows you to view and change the current MAX II register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

Table 6–1. MAX II Registers (Part 1 of 2)

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the up to eight (0-7) pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.

Table 6–1. MAX II Registers (Part 2 of 2)

Register Name	Read/Write Capability	Description
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated PGM LED (D12-D14) based on the following encoding: ■ 0 = PGM LED (D14) and corresponds to the flash memory page for the factory hardware design ■ 1 = PGM LED (D13) and corresponds to the flash memory page for the user hardware 1 design ■ 2 = PGM LED (D12) and corresponds to the flash memory page for the user hardware 2 design

- **PSO**—Sets the MAX II PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX II PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–1 for more information.
- **PSS**—Displays the MAX II PSS register value. Refer to Table 6–1 for the list of available options.
- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX II register values. Refer to Table 6–1 for more information.

☞ Because the **System Info** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST, or changing the PSO value, can cause the Board Test System to stop running.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Arria V GT Device 1, Arria V GX Device 2, and MAX II are always in the JTAG chain. SW6 selects whether HSMA, HSMB, and FMC are in the chain. Set the SW6 switch in the off position to include the interface in the JTAG chain. Refer to Table 4–3 for detailed settings.

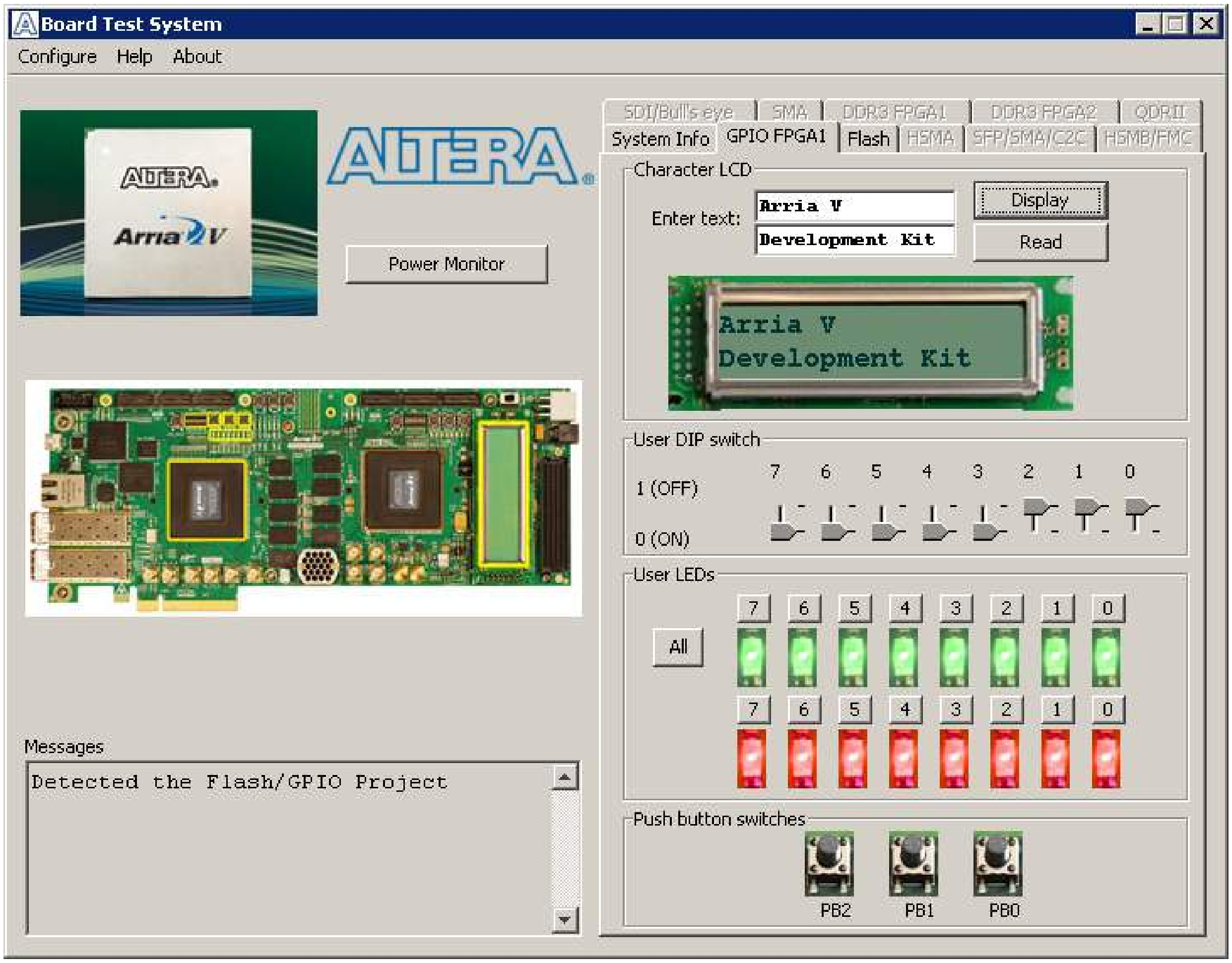
☞ If you plug in an external USB-Blaster cable to the JTAG header (J1), the On-Board USB-Blaster II is disabled.

For details on the JTAG chain, refer to the *Arria V GT FPGA Development Board Reference Manual.* For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

The GPIO FPGA 1 Tab

The **GPIO FPGA 1** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses. Figure 6–3 shows the **GPIO FPGA 1** tab.

Figure 6–3. The GPIO FPGA 1 Tab



Enter text: Arria V

Development Kit

```
Arria V
Development Kit
```

```
Detected the Flash/GPIO Project
```

The following sections describe the controls on the **GPIO FPGA 1** tab.

Character LCD

The **Character LCD** controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**. Click **Read** to read the currently shown on the LCD display.

☞ If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switch

The read-only **User DIP switches** control displays the current positions of the switches in the user DIP switch bank (SW2). Change the switches on the board to see the graphical display change accordingly.

User LEDs

The **User LEDs** control displays the current state of the user LEDs for FPGA 1. To toggle the board LEDs, click the **0** to **7** buttons to toggle red or green LEDs, or click the **All** button.

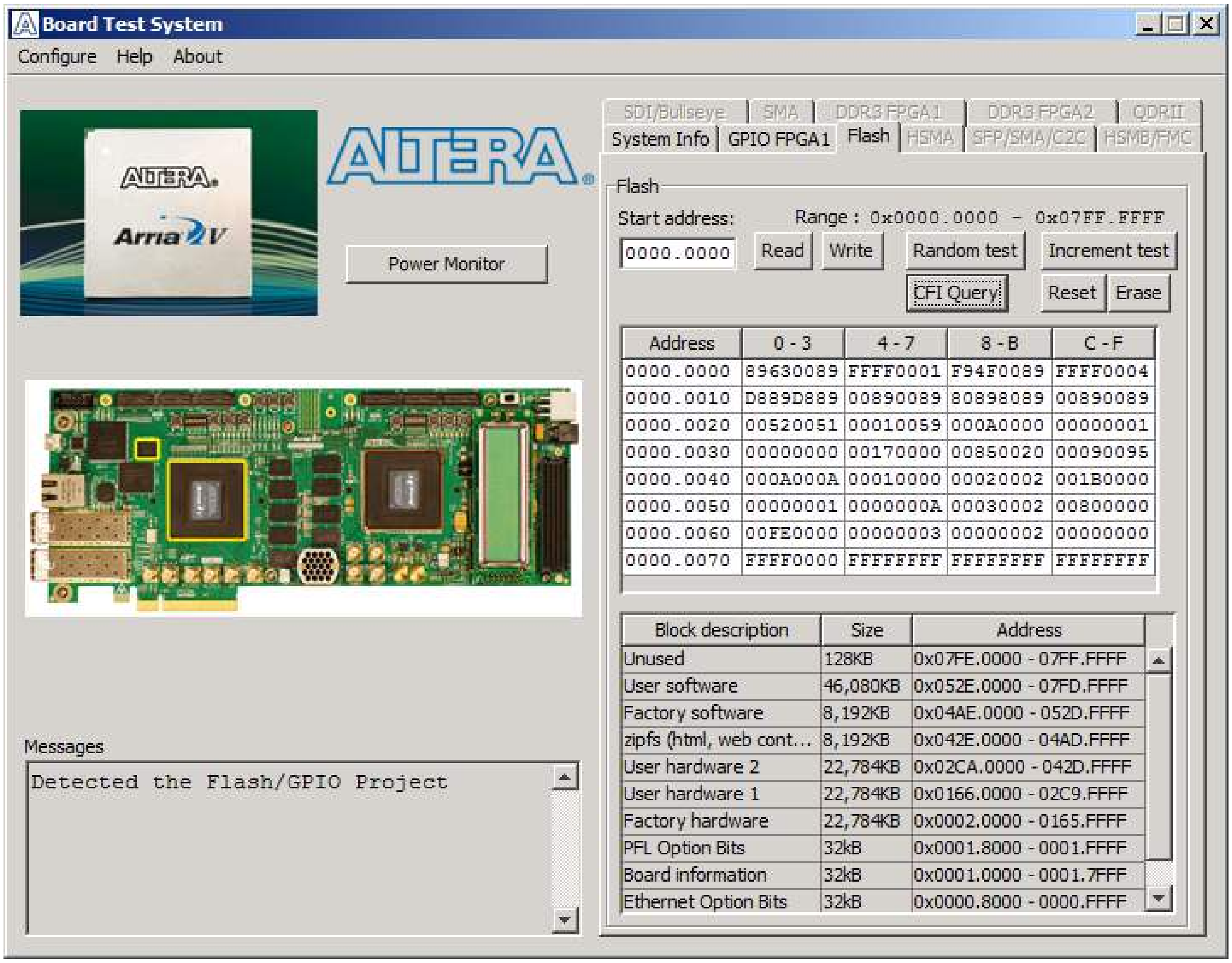
Push Button Switches

The read-only **Push button switches** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The Flash Tab

The **Flash** tab (Figure 6–4) allows you to read and write flash memory on your board.

Figure 6–4. The Flash Tab



Start address: 0000.0000

Range : 0x0000.0000 – 0x07FF.FFFF

Address	0 - 3	4 - 7	8 - B	C - F
0000.0000	89630089	FFFF0001	F94F0089	FFFF0004
0000.0010	D889D889	00890089	80898089	00890089
0000.0020	00520051	00010059	000A0000	00000001
0000.0030	00000000	00170000	00850020	00090095
0000.0040	000A000A	00010000	00020002	001B0000
0000.0050	00000001	0000000A	00030002	00800000
0000.0060	00FE0000	00000003	00000002	00000000
0000.0070	FFFF0000	FFFFFFFF	FFFFFFFF	FFFFFFFF

Block description	Size	Address
Unused	128KB	0x07FE.0000 - 07FF.FFFF
User software	46,080KB	0x052E.0000 - 07FD.FFFF
Factory software	8,192KB	0x04AE.0000 - 052D.FFFF
zipfs (html, web cont...	8,192KB	0x042E.0000 - 04AD.FFFF
User hardware 2	22,784KB	0x02CA.0000 - 042D.FFFF
User hardware 1	22,784KB	0x0166.0000 - 02C9.FFFF
Factory hardware	22,784KB	0x0002.0000 - 0165.FFFF
PFL Option Bits	32kB	0x0001.8000 - 0001.FFFF
Board information	32kB	0x0001.0000 - 0001.7FFF
Ethernet Option Bits	32kB	0x0000.8000 - 0000.FFFF

Messages

```
Detected the Flash/GPIO Project
```

The following sections describe the controls on the **Flash** tab.

Read

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table. The flash memory addresses display in the format the Nios II processor within the FPGA uses, that is, each flash memory address is offset by 0x0800.0000. Valid are entries are 0x0000.0000 through 0x07FF.FFFF.

☞ If you enter an address outside of the flash memory address space, a warning message identifies the valid flash memory address range.

Write

The **Write** control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

☞ To prevent overwriting the dedicated portions of flash memory, the application limits the user-writable flash memory address range to the uppermost 128 KB memory block, as shown in Figure 6–1 on page 6–1 and Table A–1 on page A–1).

Random Test

Starts a random data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

CFI Query

The **CFI Query** control updates the memory table, displaying the CFI ROM table contents from the flash device.

Increment Test

Starts an incrementing data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

Reset

The **Reset** control executes the flash device’s reset command and updates the memory table displayed on the **Flash** tab.

Erase

Erases flash memory, which is limited to a scratch page in the upper 128K block.

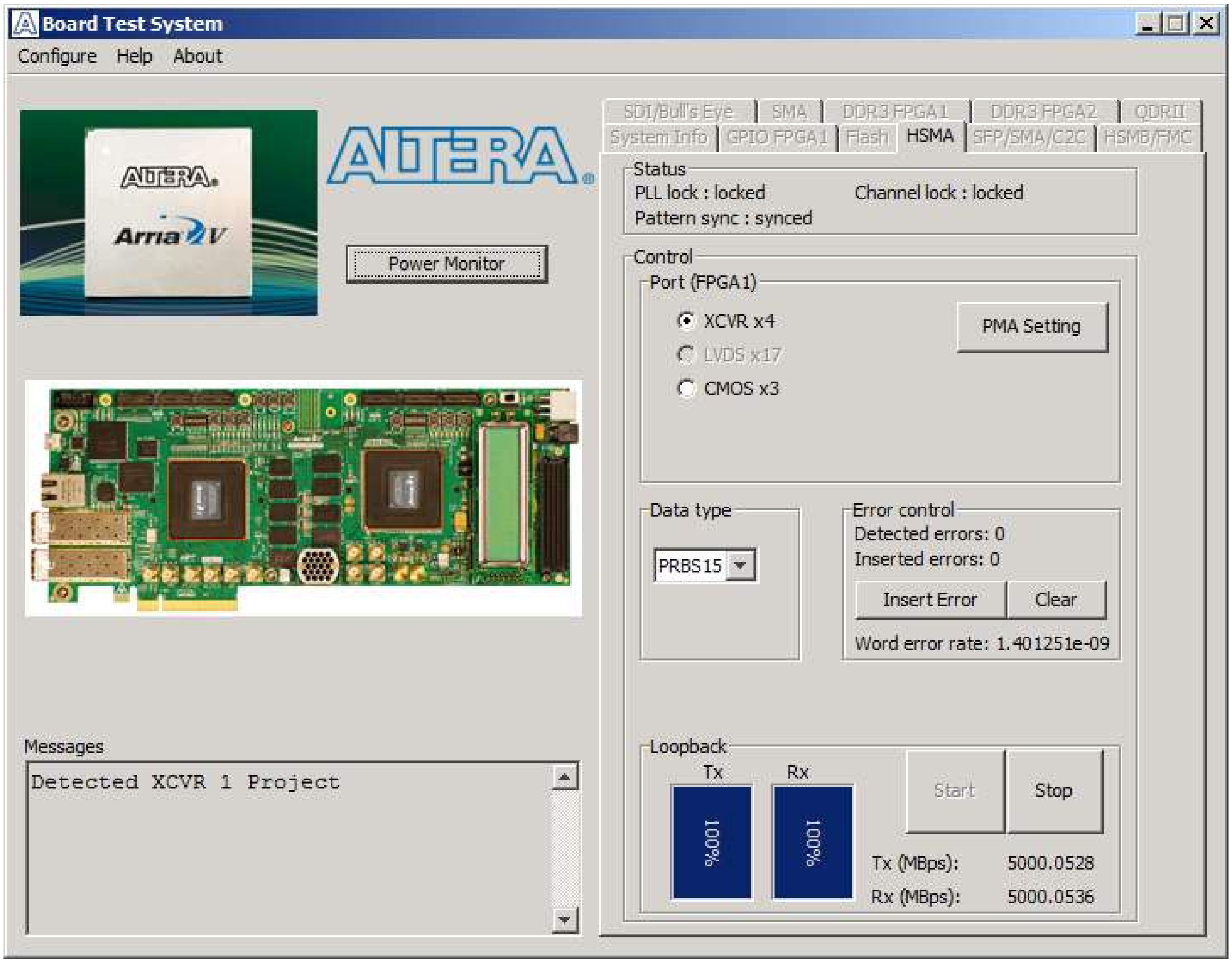
Flash Memory Map

Displays the flash memory map for the Arria V GT FPGA Development Kit.

The HSMA Tab

The **HSMA** tab (Figure 6–5) allows you to perform loopback tests on the transceiver (XCVR) and CMOS ports.

Figure 6–5. The HSMA Tab



Board Test System
Configure Help About
Power Monitor
SDI/Bull's Eye | SMA | DDR3 FPGA1 | DDR3 FPGA2 | QDRII
System Info | GPIO FPGA1 | Flash | HSMA | SFP/SMA/C2C | HSMB/FMC
PMA Setting
Insert Error
Clear
Start
Stop
100%
100%
Messages

Status
PLL lock : locked
Channel lock : locked
Pattern sync : synced

Control
Port (FPGA1)
● XCVR x4
○ LVDS x17
○ CMOS x3

Data type
PRBS15

Error control
Detected errors: 0
Inserted errors: 0
Word error rate: 1.401251e-09

Loopback
Tx Rx
Tx (MBps): 5000.0528
Rx (MBps): 5000.0536

```
Detected XCVR 1 Project
```

You must have the loopback HSMA installed on the HSMC Port A connector that you are testing for this test to work correctly.

The following sections describe the controls on the **HSMA** tab.

Status

The **Status** control displays the following status information during the loopback test:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port (FPGA1)

The **Port (FPGA1)** control allows you to specify which interface to test. The following port tests are available.

Design run at 10 Gbps:

- **XCVR x4**

Design run at 50 Mbps:

- **CMOS x3**

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters (at 50MHz) that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals between the receiver and the transmitter. Enter the following values to enable the serial loopbacks:

  `0` = high speed serial transceiver signals to loopback on the board
  `1` = serial loopback
  `2` = reverse serial loopback pre-CDR
  `4` = reverse serial loopback post-CDR

- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in the transactions for transceivers. The LVDS design uses PRBS8, and the CMOS design uses PRBS3. The following data types are available for transceiver analysis:

- **PRBS7**—Selects pseudo-random 7-bit sequences.
- **PRBS15**—Selects pseudo-random 15-bit sequences.
- **PRBS23**—Selects pseudo-random 23-bit sequences.
- **PRBS31**—Selects pseudo-random 31-bit sequences.
- **HF1**—highest frequency divide-by-2 data pattern 10101010.
- **HF2**—next highest frequency divide-by-4 data pattern 1100110011001100.
- **HF3**—second lowest frequency divide-by-8 data pattern 1111000011110000.

- **LF** —lowest frequency divide-by-40 data pattern.

  ☞ Settings HF1, HF2, HF3, LF are for transmit observation only.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.
- **Word error rate**—Detected word errors/total received words.

Start

The **Start** control initiates transaction performance analysis.

Stop

The **Stop** control terminates transaction performance analysis.

Loopback

These controls display current transaction performance analysis information collected since you last clicked **Start**:

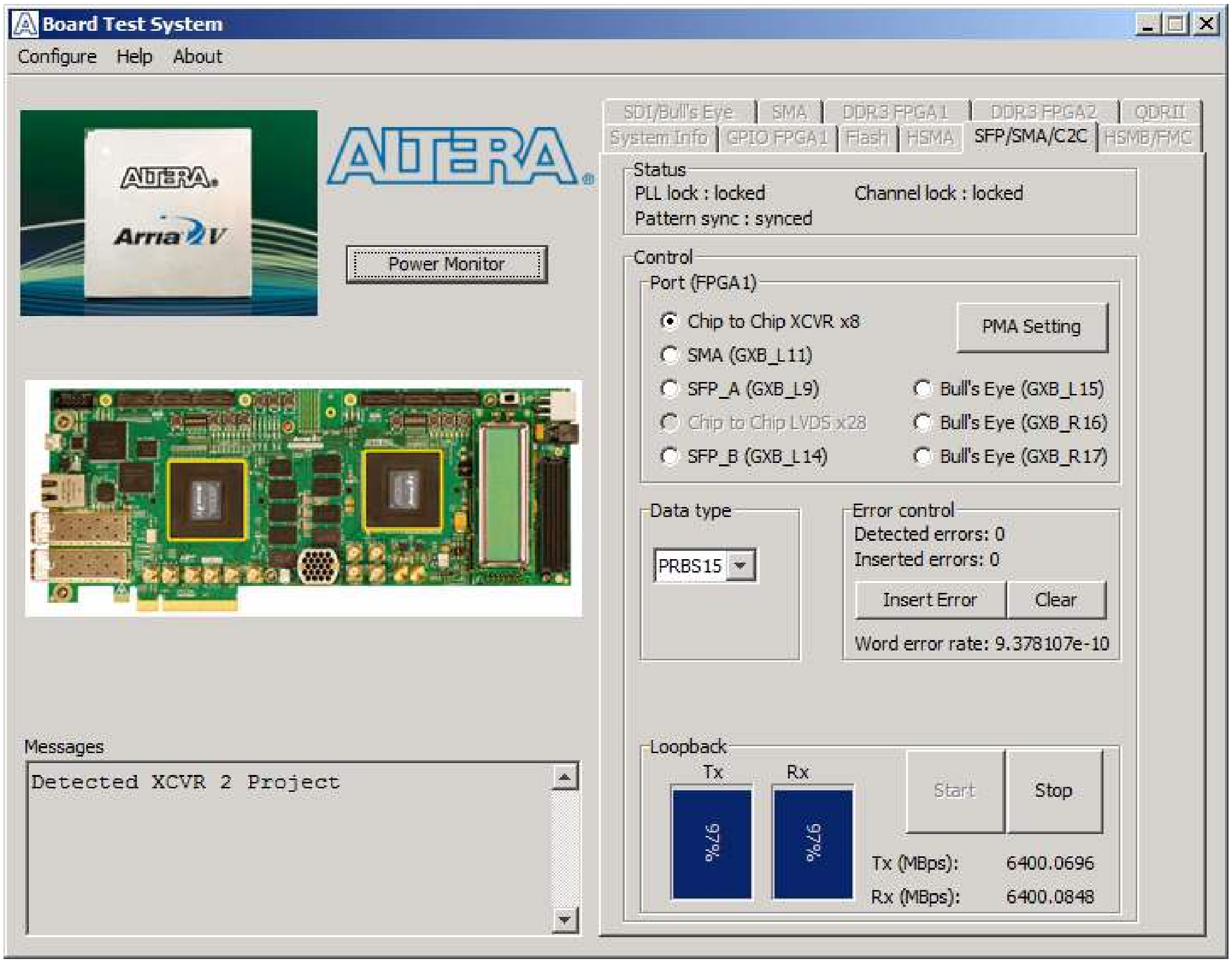
- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

The SFP/SMA/C2C Tab

The **SFP/SMA/C2C** tab (Figure 6–6) allows you to run test designs using the respective transceiver interfaces on FPGA 1.

To run the SFP+ designs using this GUI, use the USER1_DIPSW to enable or disable SFP lasers. To turn the SFP_A laser on, ensure that USER1_DIPSW[4] is in the OFF position (toward the HSMC connector). To turn on the SFP_B laser, ensure that USER1_DIPSW[5] is in the OFF position.

Figure 6–6. The SFP/SMA/C2C Tab



Status
PLL lock : locked
Channel lock : locked
Pattern sync : synced

Control
Port (FPGA1)
● Chip to Chip XCVR x8
○ SMA (GXB_L11)
○ SFP_A (GXB_L9)
○ Chip to Chip LVDS x28
○ SFP_B (GXB_L14)
○ Bull's Eye (GXB_L15)
○ Bull's Eye (GXB_R16)
○ Bull's Eye (GXB_R17)

Data type: PRBS15

Error control
Detected errors: 0
Inserted errors: 0
Word error rate: 9.378107e-10

Loopback
Tx (MBps): 6400.0696
Rx (MBps): 6400.0848

Messages

```
Detected XCVR 2 Project
```

The following sections describe the controls on the **SFP/SMA/C2C** tab.

Status

The **Status** control displays the following status information during the loopback test:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded.

- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port (FPGA1)

The **Port (FPGA1)** control allows you to specify which interface to test. The following port tests are available.

- **Chip to Chip XCVR x8** (HSMA design run at 6.4 Gbps)

Designs run at 10 Gbps:

- **SMA (GXB_L11)**
- **SFP_A (GXB_L9)**
- **SFB_B (GXB_L14)**
- **Bull's Eye (GXB_L15)**
- **Bull's Eye (GXB_R16)**
- **Bull's Eye (GXB_R17)**

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals between the receiver and the transmitter. Enter the following values to enable the serial loopbacks:

  `0` = high speed serial transceiver signals to loopback on the board
  `1` = serial loopback
  `2` = reverse serial loopback pre-CDR
  `4` = reverse serial loopback post-CDR

- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS7**—Selects pseudo-random 7-bit sequences.
- **PRBS15**—Selects pseudo-random 15-bit sequences.

- **PRBS23**—Selects pseudo-random 23-bit sequences.
- **PRBS31**—Selects pseudo-random 31-bit sequences.
- **HF1**—highest frequency divide-by-2 data pattern 10101010.
- **HF2**—next highest frequency divide-by-4 data pattern 1100110011001100.
- **HF3**—second lowest frequency divide-by-8 data pattern 1111000011110000.
- **LF SMA, SFP, Bull's Eye**—lowest frequency divide-by-40 data pattern.
- **LF**—Chip-to-chip divide-by-32 data pattern.

☞ Settings HF1, HF2, HF3, LF are for transmit observation only.

Error Control

The **Error control** control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.
- **Word error rate**—Detected word errors/total received words.

Loopback

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

Start

The **Start** control initiates transaction performance analysis.

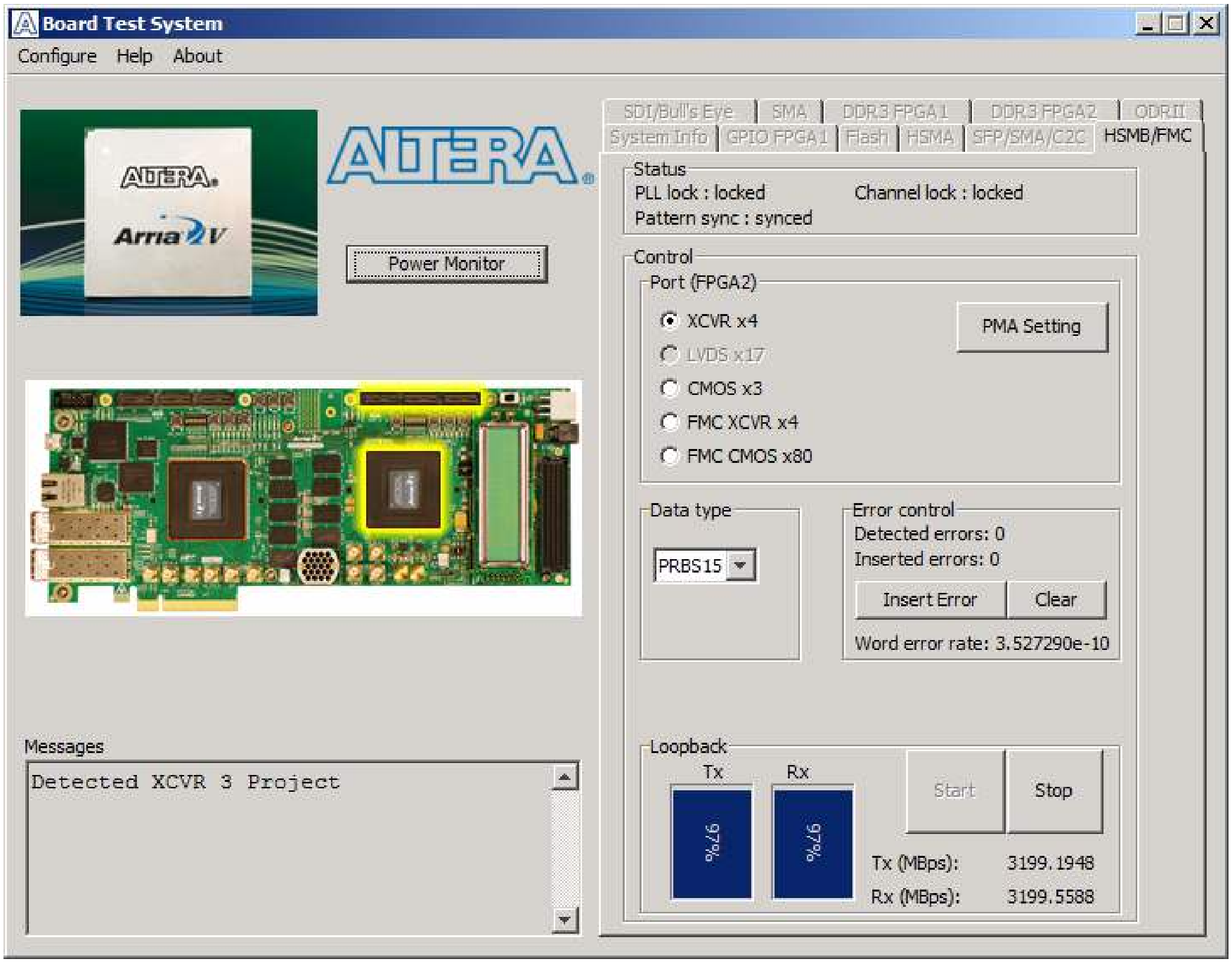
Stop

The **Stop** control terminates transaction performance analysis.

The HSMB/FMC Tab

The **HSMB/FMC** tab (Figure 6–7) allows you to perform loopback tests on the XCVR and CMOS ports.

Figure 6–7. The HSMB/FMC Tab



Status
PLL lock : locked
Channel lock : locked
Pattern sync : synced

Control
Port (FPGA2)
● XCVR x4
○ LVDS x17
○ CMOS x3
○ FMC XCVR x4
○ FMC CMOS x80

Data type
PRBS15

Error control
Detected errors: 0
Inserted errors: 0
Word error rate: 3.527290e-10

Loopback
Tx 97%
Rx 97%
Tx (MBps): 3199.1948
Rx (MBps): 3199.5588

Messages
```
Detected XCVR 3 Project
```

☞ You must have the loopback HSMB installed on the HSMC Port B connector that you are testing for this test to work correctly.

The following sections describe the controls on the **HSMB/FMC** tab.

Status

The **Status** control displays the following status information during the loopback test:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port (FPGA2)

The **Port (FPGA2)** control allows you to specify which interface to test. The following port tests are available:

- **XCVR x4** (HSMB design run at 6.4 Gbps)
- **CMOS x3** (HSMB design run at 25 Mbps)
- **FMC XCVR x4** (FMC design run at 6.4 Gbps)
- **FMC CMOS x80** (FMC design run at 25 Mbps)

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback—**Routes signals between the receiver and the transmitter. Enter the following values to enable the serial loopbacks:

  `0` = high speed serial transceiver signals to loopback on the board
  `1` = serial loopback
  `2` = reverse serial loopback pre-CDR
  `4` = reverse serial loopback post-CDR

- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer—**Specifies the setting for the receiver equalizer.
- **DC gain—**Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in transceiver transactions. The following data types are available for transceiver analysis:

- **PRBS7**—Selects pseudo-random 7-bit sequences.
- **PRBS15**—Selects pseudo-random 15-bit sequences.
- **PRBS23**—Selects pseudo-random 23-bit sequences.
- **PRBS31**—Selects pseudo-random 31-bit sequences.
- **HF1**—highest frequency divide-by-2 data pattern 10101010.
- **HF2**—next highest frequency divide-by-4 data pattern 1100110011001100.
- **HF3**—second lowest frequency divide-by-8 data pattern 1111000011110000.
- **LF FMC**—lowest frequency divide-by-40 data pattern.

- **LF HSMB**—lowest frequency divide-by-32 data pattern.

☞ Settings HF1, HF2, HF3, LF are for transmit observation only.

The following data types are available for CMOS analysis:

- **PRBS3**—Selects pseudo-random 3-bit sequences for HSMB x3 CMOS.
- **PRBS80**—Selects pseudo-random 80-bit sequences for FMC x80 CMOS.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.
- **Word error rate**—Detected word errors/total received words.

Loopback

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

Start

The **Start** control initiates transaction performance analysis.

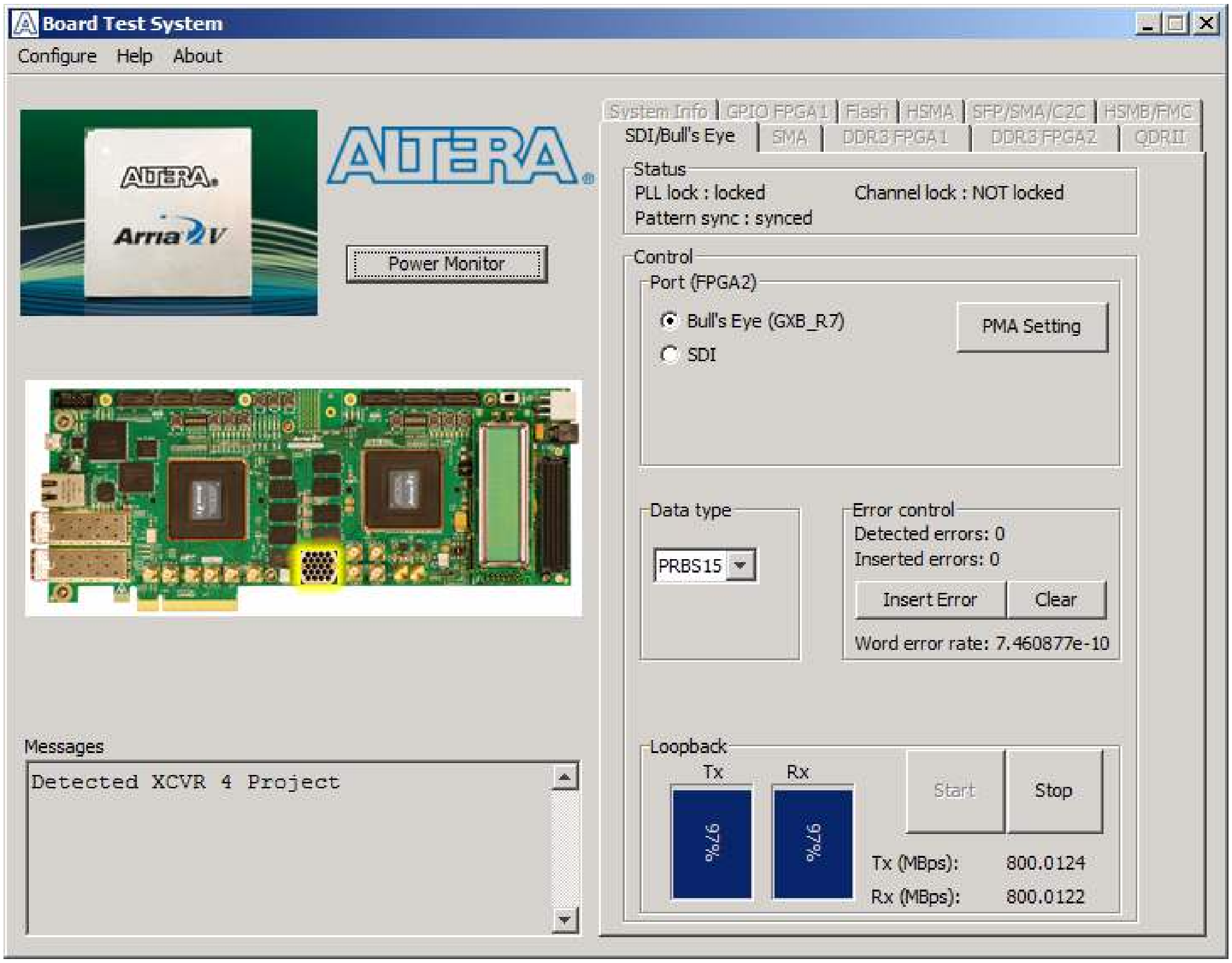
Stop

The **Stop** control terminates transaction performance analysis.

The SDI/Bull's Eye Tab

The **SDI/Bull's Eye** tab (Figure 6–8) allows you perform loopback tests on the Bull's Eye and SDI ports.

Figure 6–8. The SDI/Bull's Eye Tab



Status
PLL lock : locked
Channel lock : NOT locked
Pattern sync : synced

Control
Port (FPGA2)
● Bull's Eye (GXB_R7)
○ SDI

Data type
PRBS15

Error control
Detected errors: 0
Inserted errors: 0
Word error rate: 7.460877e-10

Loopback
Tx 97%
Rx 97%
Tx (MBps): 800.0124
Rx (MBps): 800.0122

Messages
```
Detected XCVR 4 Project
```

The following sections describe the controls on the **SDI/Bull's Eye** tab.

Status

The **Status** control displays the following status information during the loopback test:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port (FPGA2)

The **Port (FPGA2)** control allows you to specify which interface to test. The following port tests are available:

- **Bull's Eye (GXB_R7)** (design run at 6.4 Gbps)
- **SDI** (design run at 2.9 Gbps)

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals between the receiver and the transmitter. Enter the following values to enable the serial loopbacks:

  `0` = high speed serial transceiver signals to loopback on the board
  `1` = serial loopback
  `2` = reverse serial loopback pre-CDR
  `4` = reverse serial loopback post-CDR

- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS7**—Selects pseudo-random 7-bit sequences.
- **PRBS15**—Selects pseudo-random 15-bit sequences.
- **PRBS23**—Selects pseudo-random 23-bit sequences.
- **PRBS31**—Selects pseudo-random 31-bit sequences.
- **HF1**—highest frequency divide-by-2 data pattern 10101010.
- **HF2**—next highest frequency divide-by-4 data pattern 1100110011001100.
- **HF3**—second lowest frequency divide-by-8 data pattern 1111000011110000.
- **LF Bull's Eye**—lowest frequency divide-by-32 data pattern.
- **LF SDI**—lowest frequency divide-by-10 data pattern.

☞ Settings HF1, HF2, HF3, LF are for transmit observation only.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.
- **Word error rate**—Detected word errors/total received words.

Loopback

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

Start

The **Start** control initiates transaction performance analysis.

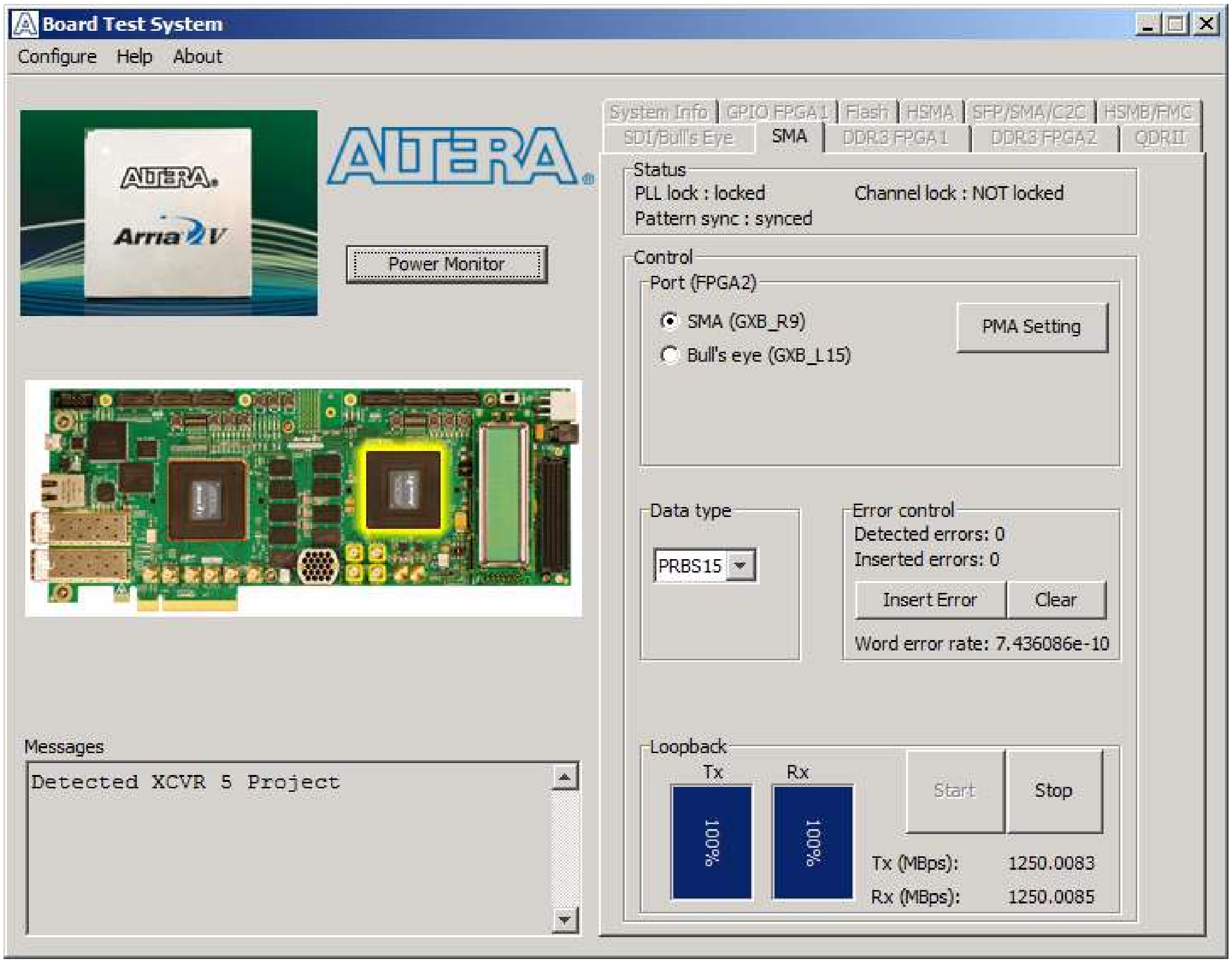
Stop

The **Stop** control terminates transaction performance analysis.

The SMA Tab

The **SMA** tab (Figure 6–9) allows you perform loopback tests on the SMA port.

Figure 6–9. The SMA Tab



Status
PLL lock : locked
Channel lock : NOT locked
Pattern sync : synced

Control
Port (FPGA2)
● SMA (GXB_R9)
○ Bull's eye (GXB_L15)

Data type
PRBS15

Error control
Detected errors: 0
Inserted errors: 0
Word error rate: 7.436086e-10

Loopback
Tx 100%
Rx 100%
Tx (MBps): 1250.0083
Rx (MBps): 1250.0085

Messages

```
Detected XCVR 5 Project
```

The following sections describe the controls on the **SMA** tab.

Status

The **Status** control displays the following status information during the loopback test:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port (FPGA2)

The **Port (FPGA2)** control allows you to specify which interface to test. The following port test is available:

- **SMA (GXB_R9)** (design run at 10 Gbps)
- **Bull's Eye (GXB_L15)** (design run at 10 Gbps)

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback—**Routes signals between the receiver and the transmitter. Enter the following values to enable the serial loopbacks:

  `0` = high speed serial transceiver signals to loopback on the board
  `1` = serial loopback
  `2` = reverse serial loopback pre-CDR
  `4` = reverse serial loopback post-CDR

- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS7**—Selects pseudo-random 7-bit sequences.
- **PRBS15**—Selects pseudo-random 15-bit sequences.
- **PRBS23**—Selects pseudo-random 23-bit sequences.
- **PRBS31**—Selects pseudo-random 31-bit sequences.
- **HF1**—highest frequency divide-by-2 data pattern 10101010.
- **HF2**—next highest frequency divide-by-4 data pattern 1100110011001100.
- **HF3**—second lowest frequency divide-by-8 data pattern 1111000011110000.
- **LF**—lowest frequency divide-by-32 data pattern.

Settings HF1, HF2, HF3, LF are for transmit observation only.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.
- **Word error rate**—Detected word errors/total received words.

Start

The **Start** control initiates transaction performance analysis.

Stop

The **Stop** control terminates transaction performance analysis.

Loopback

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

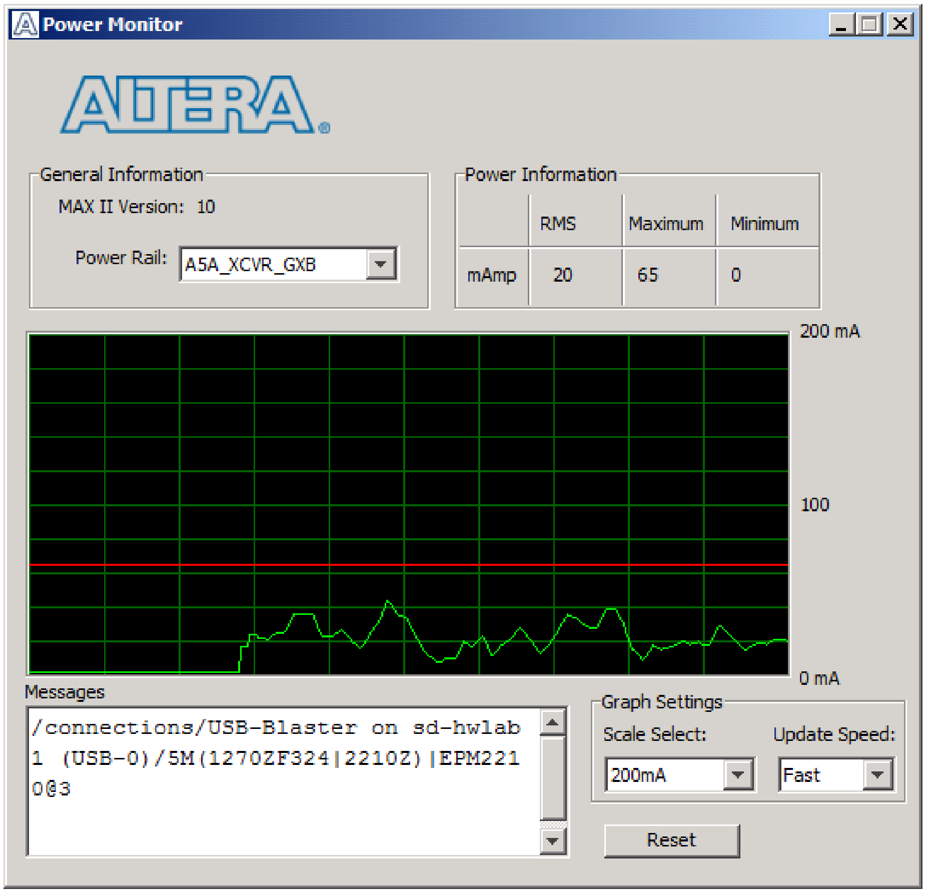
The Power Monitor

The Power Monitor measures and reports current power information for the board. To start the application, click **Power Monitor** in the Board Test System application.

☞ You can also run the Power Monitor as a stand-alone application. **PowerMonitor.exe** resides in the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\examples\board_test_system** directory. On Windows, click **Start** > **All Programs** > **Altera** > **Arria V GT FPGA Development Kit** <*version*> > **Power Monitor** to start the application.

The Power Monitor communicates with the MAX II device on the board through the JTAG bus. A power monitor circuit attached to the MAX II device allows you to measure the power that the Arria V GT FPGA is consuming. Figure 6–10 shows the Power Monitor.

Figure 6–10. The Power Monitor



General Information

MAX II Version: 10

Power Rail: A5A_XCVR_GXB

Power Information

	RMS	Maximum	Minimum
mAmp	20	65	0

Messages

```
/connections/USB-Blaster on sd-hwlab
1 (USB-0)/5M(1270ZF324|2210Z)|EPM221
0@3
```

Graph Settings

Scale Select: 200mA

Update Speed: Fast

The following sections describe the Power Monitor controls.

General Information

The **General information** controls display the following information about the MAX II device:

- **MAX II Version**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\factory_recovery** and <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\examples\max2** directories. Newer revisions of this code might be available on the Arria V GT FPGA Development Kit page of the Altera website.
- **Power Rail**—Selects the power rail to measure. After selecting the desired rail, click **Reset** to refresh the screen with new board readings.

A table with the power rail information is available in the *Arria V GT FPGA Development Board Reference Manual*.

Power Information

The **Power information** control displays current, maximum, and minimum power readings for the following units:

- **mAmp**

Power Graph

The power graph displays the mA power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

Graph Settings

The following **Graph settings** controls allow you to define the look and feel of the power graph:

- **Scale Select**—Specifies the amount to scale the power graph. Select a smaller number to zoom in to see finer detail. Select a larger number to zoom out to see the entire range of recorded values.
- **Update Speed**—Specifies how often to refresh the graph.

Reset

This **Reset** control clears the graph, resets the minimum and maximum values, and restarts the Power Monitor.

Calculating Power

The Power Monitor calculates power by measuring two different voltages with the LT2418 A/D and applying the equation $P = V \times I$ to determine the power consumption. The LT2418 measures the voltage after the appropriate sense resistor (*Vsense*) and the voltage drop across that sense resistor (*Vdif*). The current (*I*) is calculated by dividing the measured voltage drop across the resistor by the value of the sense resistor ($I = Vdif/R$). Through substitution, the equation for calculating power becomes $P = V \times I = Vsense \times (Vdif/R) = (Vsense) \times (Vdif) \times (1/.003)$, except for the A5A_VCCINT and A5B_VCCINT rails which uses 0.001 Ohms for R and A5A_VCCD_PLL_1.5V and A5B_VCCD_PLL_1.5V, which use 0.009 Ohms.

You can verify the power numbers shown in the Power Monitor with a digital multimeter that is capable of measuring microvolts to ensure you have enough significant digits for an accurate calculation. Measure the voltage on one side of the resistor (the side opposite the power source) and then measure the voltage on the other side. The first measurement is *Vsense* and the difference between the two measurements is *Vdif*. Plug the values into the equation to determine the power consumption.

The Clock Control

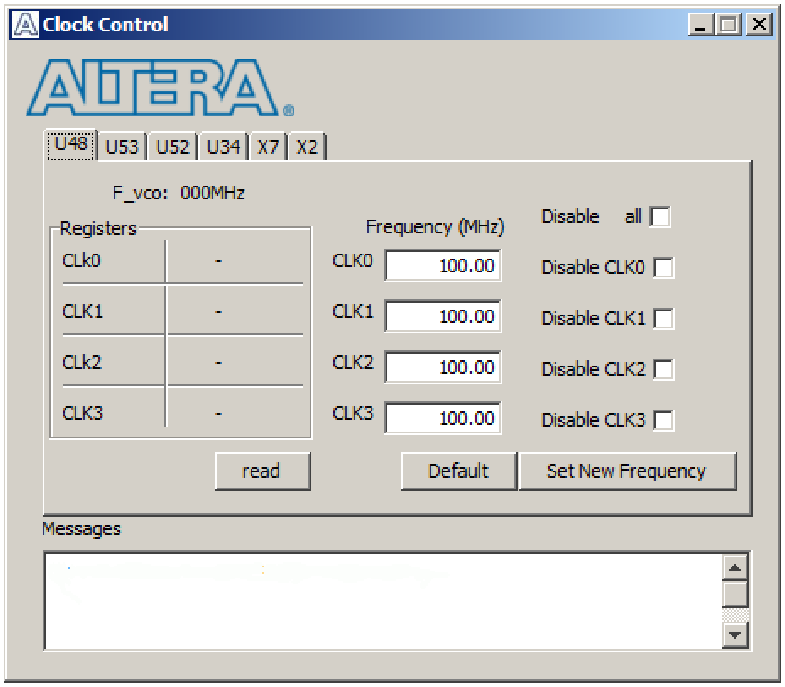
The Clock Control application sets the Si570 and Si571 programmable oscillators to any frequency between 10 MHz and 810 MHz with eight digits of precision to the right of the decimal point. The Si570 oscillator drives a 1-to-6 buffer that drives a copy of the clock to the top and bottom edges of each FPGA in addition to REFCLK1 on the left side of each FPGA. There are also four Si5338A custom devices, which output 4 programmable clocks to each FPGA. There are two of these devices dedicated to each FPGA. Each Si5338A device provides three transceiver reference clocks to the FPGA as well as an additional clock to one of the edges of the FPGA. In addition, Clk1 on U53 drives a 1-to-2 clock buffer to output clocks to REFCLK3 on the left side of FPGA 1 and to a Samtec Bullseye SMA connector (J16).

The Clock Control application runs as a stand-alone application. **ClockControl.exe** resides in the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\examples\board_test_system** directory. On Windows, click **Start** > **All Programs** > **Altera** > **Arria V GT FPGA Development Kit** <*version*> > **Clock Control** to start the application.

For more information about the Si570, Si571, and Si5338A and the Arria V GT FPGA development board's clocking circuitry and clock input pins, refer to the *Arria V GT FPGA Development Board Reference Manual*.

The Clock Control communicates with the MAX II device on the board through the JTAG bus. The Si570 and Si571 (X7, X2) programmable oscillators are connected to the MAX II device through a 2-wire serial bus. Figure 6–11 shows the Clock Control.

Figure 6–11. The Clock Control



F_vco: 000MHz

Registers

CLk0	-
CLK1	-
CLk2	-
CLK3	-

Frequency (MHz)

Disable all □

CLK0	100.00	Disable CLK0 □
CLK1	100.00	Disable CLK1 □
CLK2	100.00	Disable CLK2 □
CLK3	100.00	Disable CLK3 □

The following sections describe the Clock Control controls.

Registers

The **Registers** control shows the current values from the Si570, Si571, and Si5338A registers.

Frequency (MHz)

This control allows you to change the frequency of the Si570 and Si571, but you cannot read the value of this clock via the GUI. However, the Si5338A allows you to read the output frequencies by clicking **read**, which may take time to read. You may also change the output frequency to any of the clocks from 0.16 to 710 MHz. Once you power cycle the board, your settings will be reset to the default values, except for the Si570 and Si571 devices.

For more information about the Si570, and Si571 registers, refer to the *Si570/Si571* data sheet available on the Silicon Labs website (www.silabs.com).

Disable

The Si5338A GUI allows you to disable clock outputs if desired.

Read

This control reads the current frequency setting for the Si5338A associated with the active tab.

Default

This control sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set New Frequency

The **Set New Frequency** control sets the programmable oscillator frequency for the selected clock to the value in the **Target frequency** control. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

Configuring the FPGA Using the Quartus II Programmer

You can use the Quartus II Programmer to configure the FPGA with a specific **.sof**. Before configuring the FPGA, ensure that the Quartus II Programmer and the USB-Blaster driver are installed on the host computer, the USB cable is connected to the FPGA development board, power to the board is on, and no other applications that use the JTAG chain are running.

To configure the Arria V GT FPGA, perform the following steps:

1. Start the Quartus II Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Add File** and select the path to the desired **.sof**.
4. Turn on the **Program/Configure** option for the added file.

5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Using the Quartus II programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

Samtec High-speed Bull’s Eye Connector

This kit has a Samtec Bull’s Eye connector with transceivers and a clock output from the clock buffer (U25).

For details on the pinout, refer to the *Arria V GT FPGA Development Board Reference Manual*.

For details on how to use the Bull’s Eye interface, refer to the Altera Arria V GX FPGA Development Kits page on the Samtec website.

For information on how to install the cable using the cable tool, refer to the **bullyseye-instructions.pdf** file that resides in the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\documents**. directory.

A. Programming the Flash Memory Device

As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. This appendix describes the preprogrammed contents of the common flash interface (CFI) flash memory device on the Arria V GT FPGA development board and the Nios II EDS tools involved with reprogramming the user portions of the flash memory device.

The Arria V GT FPGA development board ships with the CFI flash device preprogrammed with a default factory FPGA configuration for running the Board Update Portal design example and a default user configuration for running the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus II software.

For more information about Altera development tools, refer to the Design Software page of the Altera website.

CFI Flash Memory Map

Table A–1 shows the default memory contents of the 1-Gb CFI flash device. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

Table A–1. Byte Address Flash Memory Map

Block Description	Size KB	Address Range
Unused	128	0x07FE.0000 - 0x07FF.FFFF
User software	46,080	0x052E.0000 - 0x07FD.FFFF
Factory software	8,192	0x04AE.0000 - 0x052D.FFFF
Zipfs (html, web content)	8,192	0x042E.0000 - 0x04AD.FFFF
User hardware 2	22,784	0x02CA.0000 - 0x042D.FFFF
User hardware 1	22,784	0x0166.0000 - 0x02C9.FFFF
Factory hardware	22,784	0x0002.0000 - 0x0165.FFFF
PFL option bits	32	0x0001.8000 - 0x0001.FFFF
Board information	32	0x0001.0000 - 0x0001.7FFF
Ethernet option bits	32	0x0000.8000 - 0x0000.FFFF
User design reset vector	32	0x0000.0000 - 0x0000.7FFF

CAUTION

Altera recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Altera tools. If you unintentionally overwrite the factory hardware or factory software image, refer to "Restoring the Flash Device to the Factory Settings" on page A–4.

Preparing Design Files for Flash Programming

You can obtain designs containing prepared **.flash** files from the Arria V GT FPGA Development Kit page of the Altera website or create **.flash** files from your own custom design.

The Nios II EDS **sof2flash** command line utility converts your Quartus II-compiled **.sof** into the **.flash** format necessary for the flash device. Similarly, the Nios II EDS **elf2flash** command line utility converts your compiled and linked Executable and Linking Format File (**.elf**) software design to **.flash**. After your design files are in the **.flash** format, use the Board Update Portal or the Nios II EDS **nios2-flash-programmer** utility to write the **.flash** files to the user hardware 1 and user software locations of the flash memory.

For more information about Nios II EDS software tools and practices, refer to the Embedded Software Development page of the Altera website.

Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Quartus II software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:
   - For Quartus II **.sof** files:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0x01660000
--pfl --optionbit=0x00018000 --programmingmode=PS↵
```

   - For Nios II **.elf** files:

```
elf2flash --base=0x0 --end=0x07FFFFFF --reset=0x052E0000 --input=<yourfile>_sw.elf
--output=<yourfile>_sw.flash
--boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec↵
```

The resulting **.flash** files are ready for flash device programming. If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to **.flash** format and concatenate them into one **.flash** file before using the Board Update Portal to upload them.

The Board Update Portal standard **.flash** format conventionally uses either <*filename*>**_hw.flash** for hardware design files or <*filename*>**_sw.flash** for software design files.

Programming Flash Memory Using the Board Update Portal

Once you have the necessary **.flash** files, you can use the Board Update Portal to reprogram the flash memory. Refer to "Using the Board Update Portal to Update User Designs" on page 5–2 for more information.

If you have generated a **.sof** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

Programming Flash Memory Using the Nios II EDS

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly. To program the **.flash** files or any compatible S-Record File (**.srec**) to the board using **nios2-flash-programmer**, perform these steps:

1. Set the Load Selector (SW5.3) to the on (factory) (factory design) to load the Board Update Portal design from flash memory on power up.
2. Attach the USB-Blaster cable and power up the board.
3. If the board has powered up and the LCD displays either *Connecting...* or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD or if the Config Done LED (D16) does not illuminate, continue to step 4 to load the FPGA with a flash-writing design.
4. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 6–27 for more information.
5. Click **Add File** and select <*install dir*> **\kits\arriaVGT_5agtfd7kf40_fpga\factory_recovery\a5gtd7k3_fpga_bup.sof**.
6. Turn on the **Program/Configure** option for the added file.
7. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The flash device is ready for programming.
8. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
9. In the Nios II command shell, navigate to the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\factory_recovery** directory (or to the directory of the **.flash** files you created in "Creating Flash Files Using the Nios II EDS" on page A–2) and type the following Nios II EDS command:

Because two FPGA devices are hardwired in the JTAG chain, and it is possible to configure Nios II CPU devices on both FPGAs simultaneously, **nios2-flash-programmer** commands may require the `--device=<device index>` and `--instance=<instance>` arguments.

```
nios2-flash-programmer -d 1 -i 0 --base=0x0 <yourfile>_hw.flash ↵
```

10. After programming completes, if you have a software file to program, type the following Nios II EDS command:

```
nios2-flash-programmer -d 1 -i 0 --base=0x0 <yourfile>_sw.flash ↵
```

Programming the board is now complete.

For more information about the **nios2-flash-programmer** utility, refer to the *Nios II Flash Programmer User Guide*.

Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the FPGA development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "Factory Default Switch and Jumper Settings" on page 4–2.
2. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 6–27 for more information.
3. Click **Add File** and select <*install dir*> **\kits\arriaVGT_5agtfd7kf40_fpga\factory_recovery\a5gtd7k3_fpga_bup.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D16) illuminates indicating that the flash device is ready for programming.
6. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
7. In the Nios II command shell, navigate to the <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\factory_recovery** directory and type the following command to run the restore script:

   ```
   ./restore.sh ↵
   ```

   Restoring the flash memory might take several minutes. Follow any instructions that appear in the Nios II command shell.
8. After all flash programming completes, cycle the POWER switch (SW1) off then on.
9. Using the Quartus II Programmer, click **Add File** and select <*install dir*> **\kits\arriaVGT_5agtfd7kf40_fpga\factory_recovery\a5gtd7k3_fpga_bup.sof**.
10. Turn on the **Program/Configure** option for the added file.
11. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D16) illuminates indicating the flash memory device is now restored with the factory contents.
12. Cycle the POWER switch (SW1) off then on to load and run the restored factory design.
13. The restore script cannot restore the board's MAC address automatically. In the Nios II command shell, type the following Nios II EDS command:

    ```
    nios2-terminal -d 1 -i 0↵
    ```

    and follow the instructions in the terminal window to generate a unique MAC address.

☞ Because two FPGA devices are hard wired in the JTAG chain, and it is possible to configure Nios II CPU devices on both FPGAs simultaneously, **nios2-flash-programmer** commands may require the `--device=<`*`device index`*`>` and `--instance=<`*`instance`*`>` arguments.

For more information about the **nios2-flash-programmer** utility, refer to the *Nios II Flash Programmer User Guide*. To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Arria V GT FPGA Development Kit page of the Altera website.

Restoring the MAX II CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX II CPLD on the FPGA development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "Factory Default Switch and Jumper Settings" on page 4–2.
2. Launch the Quartus II Programmer.
3. Click **Auto Detect**.
4. Click **Add File** and select <*install dir*>**\kits\arriaVGT_5agtfd7kf40_fpga\factory_recovery\max2.pof**.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX II CPLD. Configuration is complete when the progress bar reaches 100%.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Arria V GT FPGA Development Kit page of the Altera website.

Additional Information

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
November 2012	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact [1]	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

[1] You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <*file name*> and <*project name*>**.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.

Visual Cue	Meaning
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
☞	The hand points to information that requires special attention.
ⓘ	The question mark directs you to a software help system with related information.
👣	The feet direct you to another document or website with related information.
🎥	The multimedia icon directs you to a related multimedia presentation.
⚠ CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
⚡ WARNING	A warning calls attention to a condition or possible situation that can cause you injury.
✉	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
💬	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.