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Kind regards,

Team Nexperia

# PHD34NQ10T

N-channel TrenchMOS standard level FET

Rev. 03 — 14 December 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies

### 1.4 Quick reference data

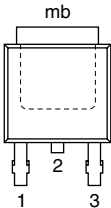
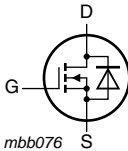
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	-	-	35	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	-	136	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 17\text{ A}; T_j = 25\text{ °C}$	-	35	40	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 34\text{ A}; V_{DS} = 80\text{ V}; T_j = 25\text{ °C}$	-	18	-	nC



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT428 (DPAK)**

[1] It is not possible to make connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHD34NQ10T	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

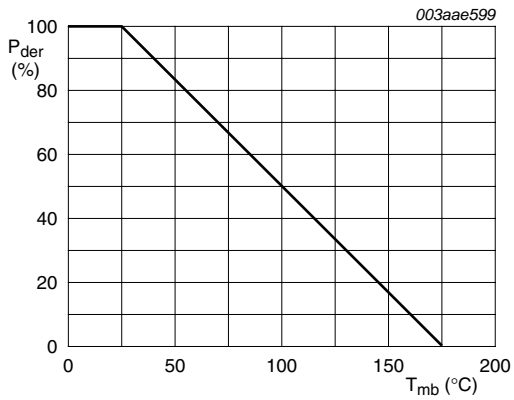
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	35	A
		$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$	-	25	A
$I_{DM}$	peak drain current	pulsed; $T_{mb} = 25\text{ °C}$	-	140	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	136	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C

### Source-drain diode

$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	35	A
$I_{SM}$	peak source current	pulsed; $T_{mb} = 25\text{ °C}$	-	140	A

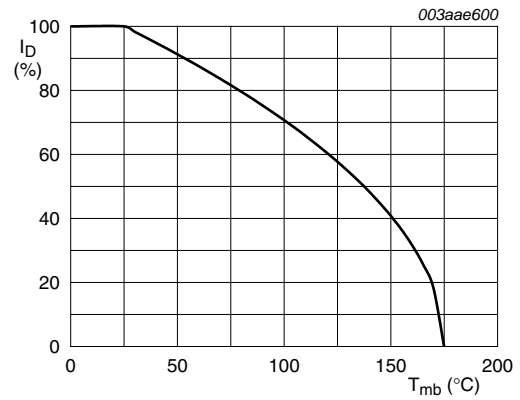
### Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 26\text{ A}; V_{sup} \leq 25\text{ V}; \text{unclamped}; t_p = 100\text{ }\mu\text{s}; R_{GS} = 50\text{ }\Omega$	-	170	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 25\text{ V}; V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; R_{GS} = 50\text{ }\Omega; \text{unclamped}$	-	35	A



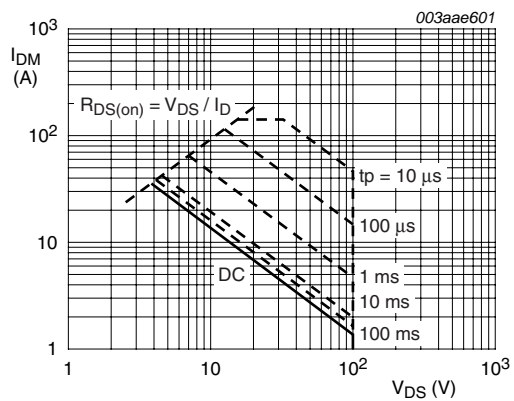
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



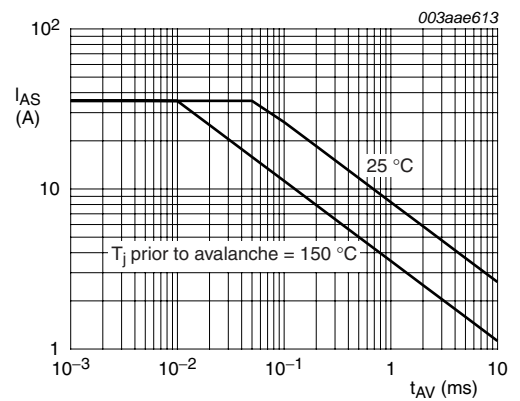
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



unclamped inductive load

Fig 4. Single-shot avalanche rating; avalanche current as a function of avalanche period

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board ; minimum footprint	-	50	-	K/W

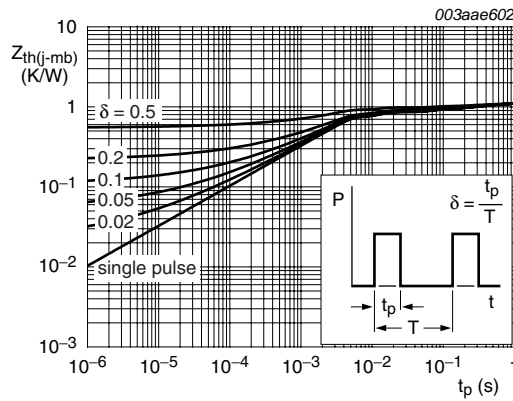


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	89	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	4.4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 17 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	-	108	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 17 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	35	40	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 34 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	40	-	nC
$Q_{GS}$	gate-source charge		-	7	-	nC
$Q_{GD}$	gate-drain charge		-	18	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	1704	-	pF
$C_{oss}$	output capacitance		-	227	-	pF
$C_{rss}$	reverse transfer capacitance		-	140	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 1.5 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5.6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	12	-	ns
$t_r$	rise time		-	55	-	ns
$t_{d(off)}$	turn-off delay time		-	48	-	ns
$t_f$	fall time		-	38	-	ns
$L_D$	internal drain inductance	measured from mounting base to centre of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	3.5	-	nH
$L_S$	internal source inductance	measured from source lead to source bond pad ; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 17 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 17 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	76	-	ns
$Q_r$	recovered charge		-	0.24	-	$\mu\text{C}$

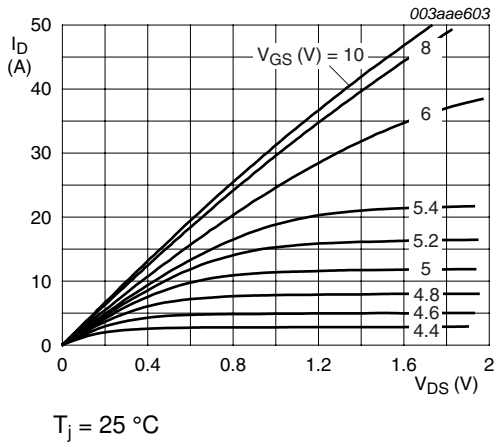


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

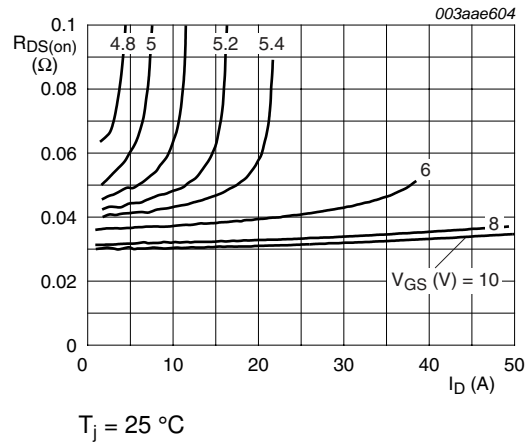


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

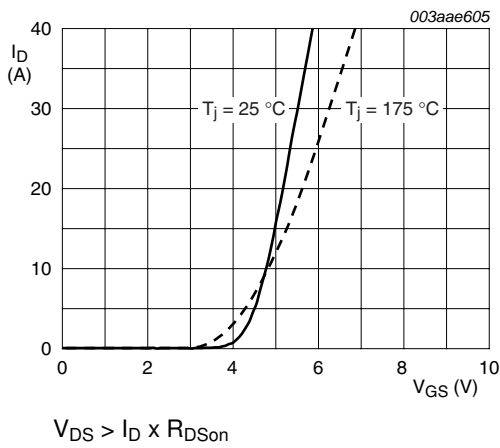


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

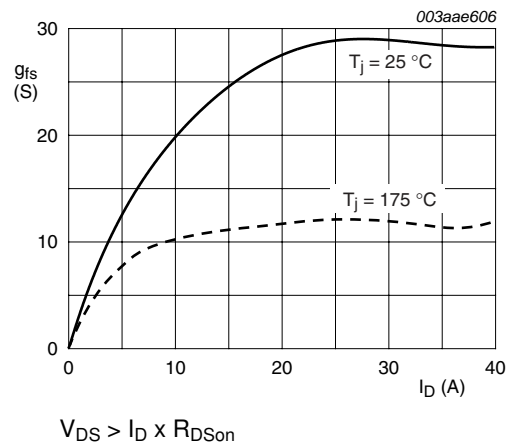
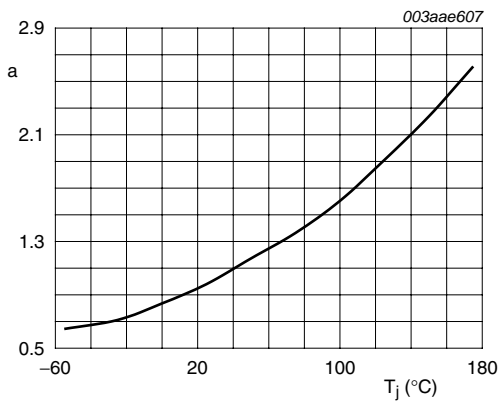


Fig 9. Forward transconductance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature

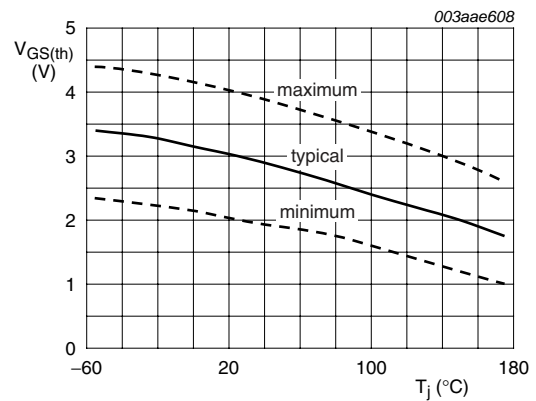
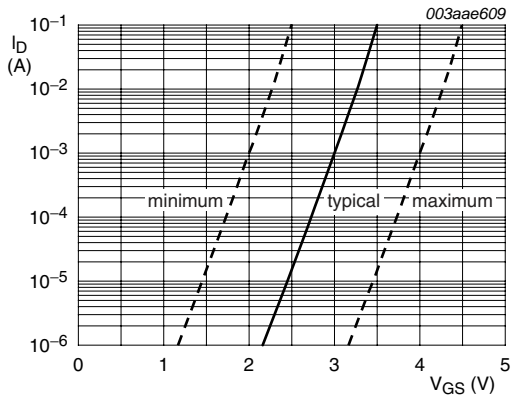
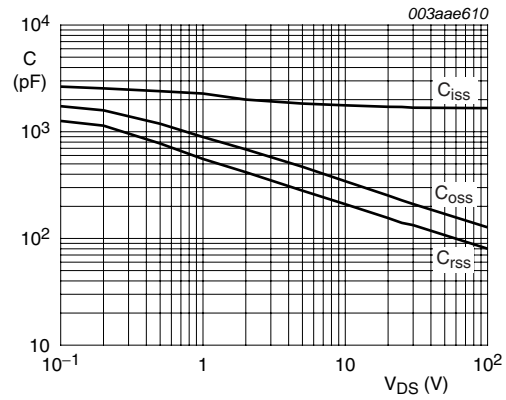


Fig 11. Gate-source threshold voltage as a function of junction temperature



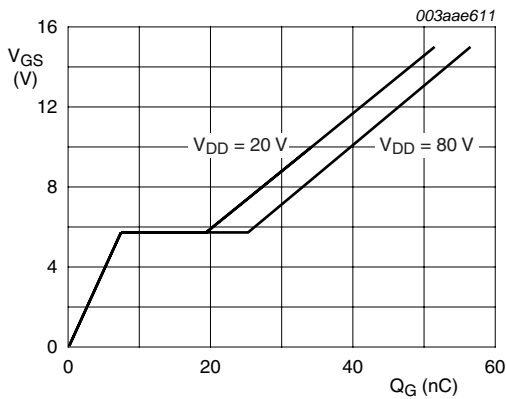
T<sub>j</sub> = 25 °C; V<sub>DS</sub> = V<sub>GS</sub>

Fig 12. Sub-threshold drain current as a function of gate-source voltage



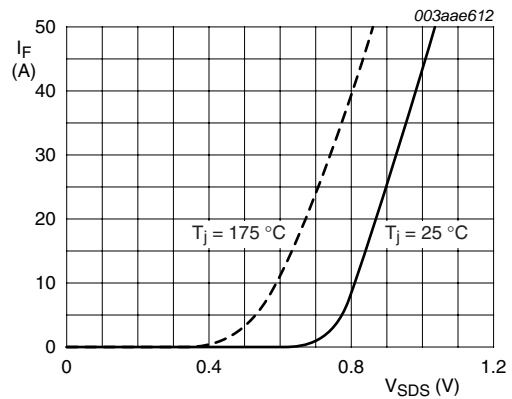
V<sub>GS</sub> = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



T<sub>j</sub> = 25 °C; I<sub>D</sub> = 34 A

Fig 14. Gate-source voltage as a function of gate charge; typical values



V<sub>GS</sub> = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

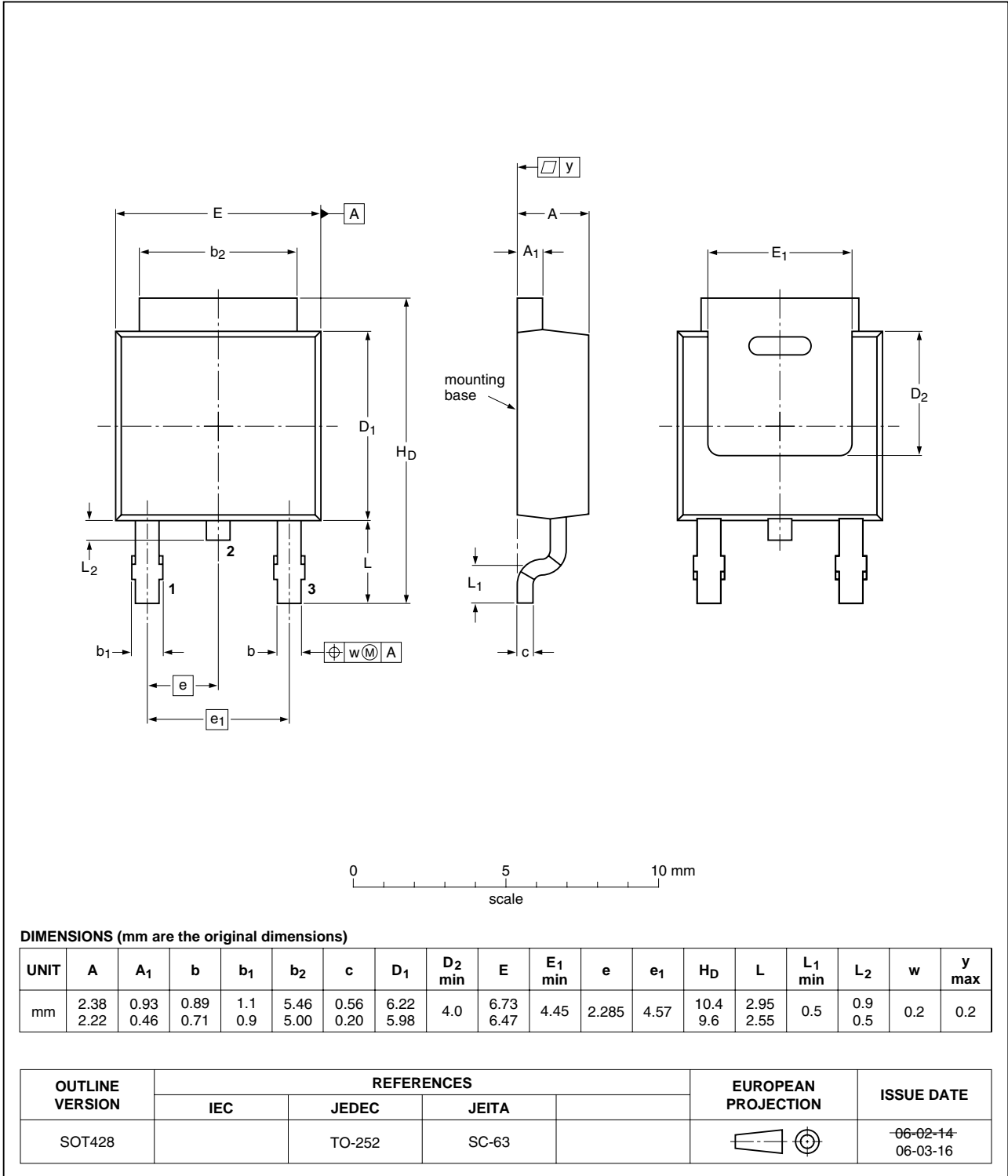


Fig 16. Package outline SOT428 (DPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD34NQ10T v.3	20101214	Product data sheet	-	PHB_PHD_PHP34NQ10T v.2
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number PHD34NQ10T separated from data sheet PHB_PHD_PHP34NQ10T v.2.</li></ul>		
PHB_PHD_PHP34NQ10T v.2	20031101	Product data sheet	-	PHB_PHD_PHP34NQ10T v.1

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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