For LCD panel backlight

Pb Free
ROHM Electronic Components

White LED driver IC (under development)

BD8108FM

rev. 0.14

● Outline

BD8108FM is a white LED driver of high-withstand-voltage (36V).
Step-up DC/DC converter and constant current output 4ch are built-in in 1chip.
The brightness can be controlled by either PWM or VDAC.

● Features

1) Input voltage range 4.5 ~ 30V
2) Built-in Step-up DC/DC controller
3) Built-in current driver 4ch (150mA max.) for LED drive
4) Compatible with PWM light-modulating 0.38 ~ 99.5%
5) Built-in protective functions (UVLO, OVP, TSD, OCP)
6) Built-in abnormal-status-detecting function (open/short)
7) HSOP-M28 package

● Application

Car navigation backlight and small & medium-sized LCD panel etc.

● Absolute maximum ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Power supply voltage (Pin : 1)	VCC	36	V
Load switch output voltage (Pin : 2)	VLOADSW	36	V
LED output voltage(Pin : 12,14,15,17)	VLED	36	V
FAIL output voltage (Pin : 3,20)	VOL	7	V
Input voltage (Pin : 5,6,10,11,24)	VIN	-0.3 ~ 7 < VCC	V
VDAC input voltage (Pin : 8)	VDAC	-0.3 ~ 7 < VCC	V
Allowable loss	Pd	2.20 ※1	W
Junction temperature	Tjmax	150	℃
Operating temperature range	Topr	-40 ~ +95	℃
Storage temperature range	Tstg	-55 ~ +150	℃
LED maximum output current (Pin : 12,14,15,17)	ILED	150 ※2 ※3	mA

※1 It is mounted on a glass epoxy board of 70mm×70mm×1.6mm. And the allowable loss is reduced at a rate of 17.6mw/℃ at the time of over 25℃.

※2 Dispersion between columns of LED maximum output current and V_F is correlated. Please refer to data on a separate sheet.

※3 Amount of the current per 1ch.

● Operating condition (Ta=25℃)

Item	Symbol	Target value	Unit
Power supply voltage (Pin : 1)	VCC	4.5 ~ 30	V
Oscillating frequency range	FOSC	50 ~ 550	kHz
External synchronization frequency range ※4 ※5(Pin : 6)	FSYNC	fosc ~ 550	kHz
External synchronization pulse duty range (Pin : 6)	FSDUTY	40 ~ 60	%

※4 Please connect SYNC to GND when external synchronization frequency is not used.

※5 Do not do such things as switching over to internal oscillating frequency while external synchronization frequency is used.

2007.Jan.

● Electric characteristic (Unless otherwise specified, VCC=12V Ta=25℃)

	Symbol	Target value			Unit	Condition
		Minimum	standard	Maximum		
Circuit current	ICC	2.5	6	10	mA	EN=2V, SYNC=VREG, RT=OPEN PWM=OPEN, ISET=OPEN, CIN=1μF
Standby current	IST	-	0	2	μA	EN=Low
[VREG Part (VREG)]						
Reference voltage	VREG	4.5	5	5.5	V	IREG=-10mA, CREG=1μF
[SW Part (SWOUT,CS)]						
SWOUT upper ON resistance	RONH	0.05	3	7	Ω	ION=-10mA
SWOUT lower ON resistance	RONL	0.05	2	5	Ω	ION=10mA
Overcurrent protection operating voltage	VDCS	0.3	0.4	0.5	V	VCS=sweep up
[error－amplifier (COMP,SS)]						
LED control voltage	VLED	0.7	0.8	0.9	V	
COMP sink current	ISKCP	40	100	200	μA	VLED=2V, Vcomp=1V
COMP source current	ISCCP	-200	-100	-40	μA	VLED=0V, Vcomp=1V
SS charging current	ISS	-14	-10	-6	μA	VSS = 1.0V
SS maximum voltage	VMXSS	2.0	2.5	3.0	V	EN = High
SS standby current	ISTSS	-	0	2	μA	EN = Low
[Oscillator Part (RT,SWOUT)]						
Oscillating frequency	FOSC	250	300	350	KHz	RT=100kΩ
[OVP Part (OVP)]						
Overvoltage-detecting reference voltage	VDOVP	1.86	2.0	2.14	V	VOVP=Sweep up
OVP hysteresis width	VDOHS	0.35	0.45	0.55	V	VOVP=Sweep down
[UVLO Part (VREG)]						
Reduced-voltage detecting reference voltage	VDUVLO	2.5	2.8	3.1	V	VREG=Sweep down
UVLO hysteresis width	VDUHS	50	100	200	mV	VREG=Sweep up
[Load switch Part (open drain) (LOADSW)]						
Load switch Low voltage	VLDL	0.05	0.15	0.3	V	ILOAD=10mA
[LED output Part (LED1-4,ISET,PWM,VDAC,OVP)]						
LED current relative dispersion width	△ ILED1	-	3	-	%	ILED=50mA
LED current absolute dispersion width	△ ILED2	-	5	-	%	ILED=50mA
ISET voltage	VISET	1.92	2.0	2.08	V	
PWM light modulation	Duty	0.38	-	99.5	%	FPWM=150Hz, ILED=50mA ※1, 2, 3
PWM frequency	FPWM	0	-	20	KHz	Duty=50% , ILED=50mA ※2, 3
VDAC gain	GVDAC	20	25	30	mA/V	VDAC=0 ~ 2V, ILED=50mA ※2, 3
Open detecting voltage 1	VDOP1	0.05	0.15	0.3	V	VLED= Sweep down, VOVP > VDOP2, VSS ≧ VMXSS
Open detecting voltage 2	VDOP2	1.56	1.7	1.84	V	VOVP= Sweep up, VLED > VDOP1, VSS VMXSS
Short detecting voltage	VDSHT	4.0	4.5	5.0	V	VLED= Sweep up, , VSS ≧ VMXSS
[Logic input (EN,SYNC,PWM,LEDEN1,LEDEN2)]						
Input High voltage	VINH	3.0	-	5.5	V	
Input Low voltage	VINL	GND	-	0.8	V	
Input inflowing current	IIN	18	35	53	μA	VIN=5V (SYNC,PWM,LEDEN1,LEDEN2)
Input inflowing current	IEN	13	25	38	μA	VEN=5V (EN)
[FAIL output (open drain) (FAIL1,FAIL2)]						
FAIL Low voltage	VFLL	0.05	0.1	0.2	V	IOL=1mA

◎ There is no radiation-proof design in this product.

※ 1 0%,100% input is possible

※ 2 ILED=VDAC÷RISET×3300

※ 3 ILED=VISET÷RISET×3300, VDAC > VISET

● Reference data (unless otherwise specified, Ta=25℃)

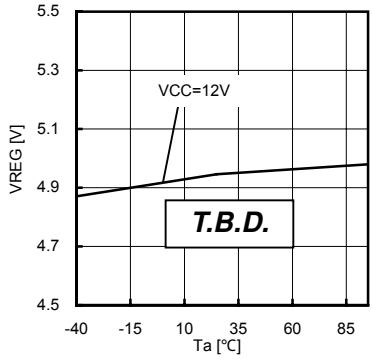


Fig.1 VREG temperature characteristic

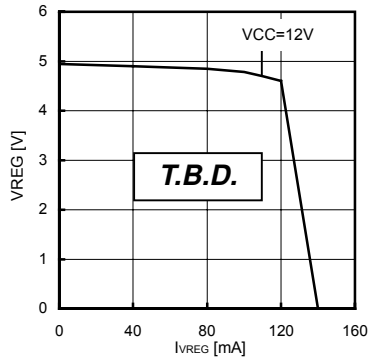


Fig.2 VREG current capacity

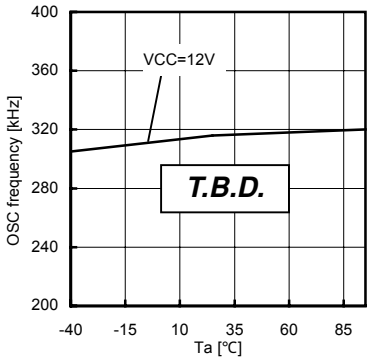


Fig.3 OSC temperature characteristic

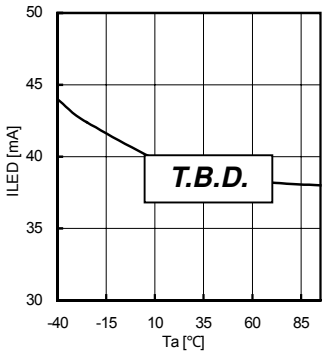


Fig.4 ILED's dependence on VLED

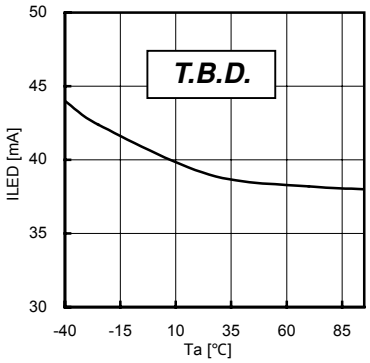


Fig.5 ILED temperature characteristic

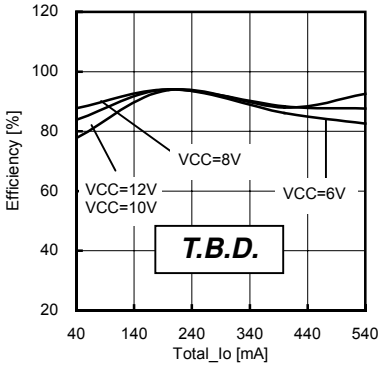


Fig.6 efficiency

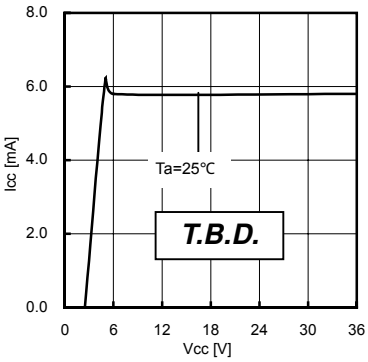


Fig.7 ICC-VCC

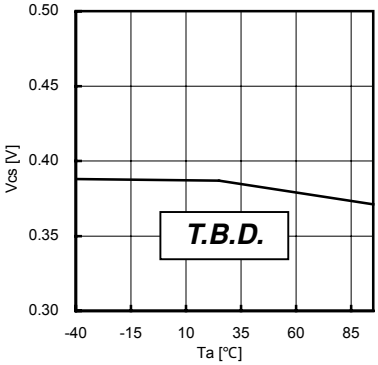


Fig.8 overcurrent detecting voltage temperature characteristic

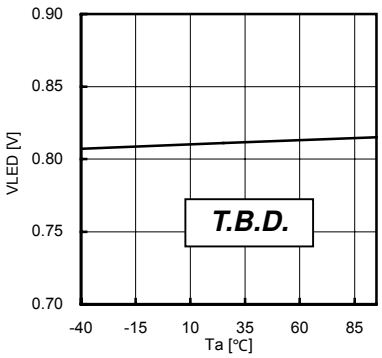


Fig.9 VLED temperature characteristic

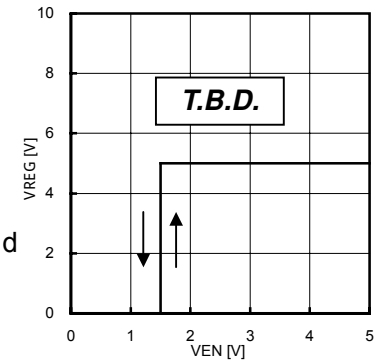


Fig.10 EN threshold voltage

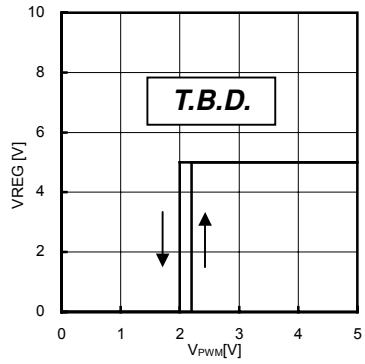


Fig.11 PWM threshold voltage

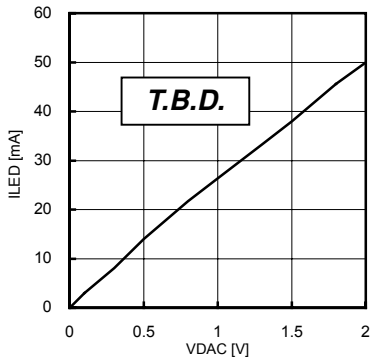


Fig.12 VDAC gain

● Block diagram

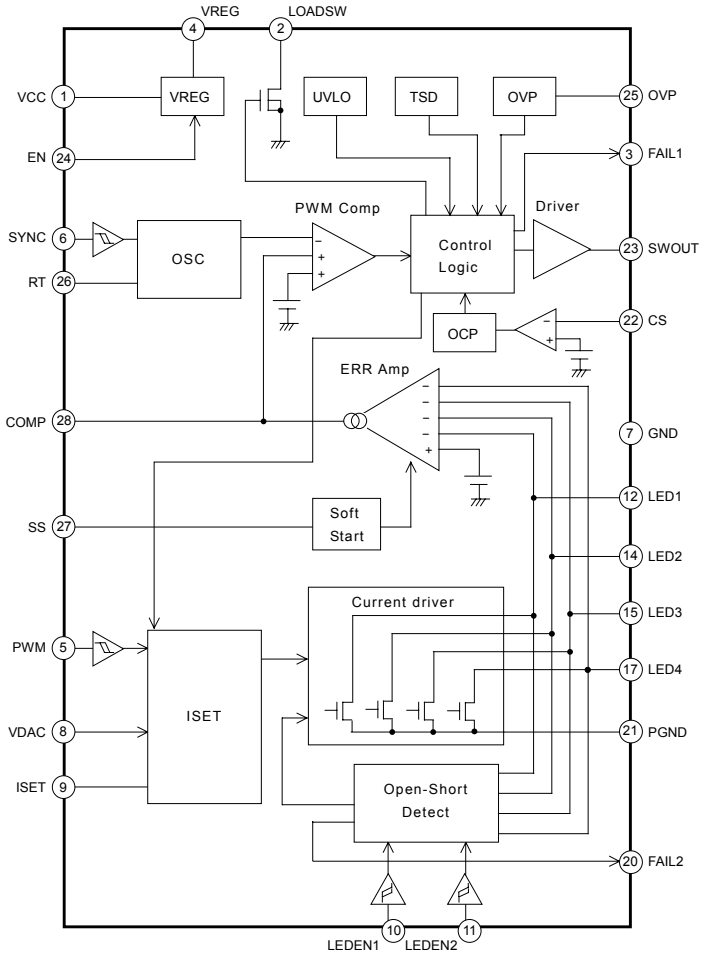


Fig.13

● Pin layout drawing

BD8108FM (HSOP-M28)

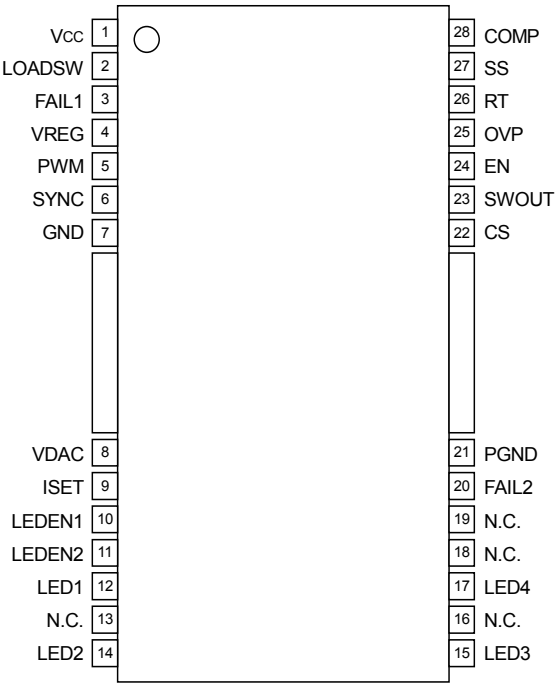


Fig.14

● Terminal Number ・ Terminal name

PIN NO.	Name of terminal	function
1	VCC	Input power supply terminal
2	LOADSW	FET connection for load switch
3	FAIL1	Output signal at abnormal time
4	VREG	Internal constant voltage output
5	PWM	PWM light modulating input terminal
6	SYNC	External synchronization signal input terminal
7	GND	GND of small signal Part
8	VDAC	DC variable light-modulating input terminal
9	ISET	LED resistor for setting the output current
10	LEDEN1	LED output terminal enable terminal 1
11	LEDEN2	LED output terminal enable terminal 2
12	LED1	LED output terminal
13	-	N.C.
14	LED2	LED output terminal
15	LED3	LED output terminal
16	-	N.C
17	LED4	LED output terminal
18	-	N.C.
19	-	N.C.
20	FAIL2	LED open/short detecting output signal
21	PGND	LED output GND terminal
22	CS	DC/DC terminal for output current detecting
23	SWOUT	DC/DC switching output terminal
24	EN	Enable terminal
25	OVP	Overvoltage detecting terminal

●5V constant voltage（VREG）

5V (Typ.) is generated from VCC input voltage when EN=H. This voltage is used as a power supply of the internal circuit, and also when the device pins need to be fixed to H voltage.

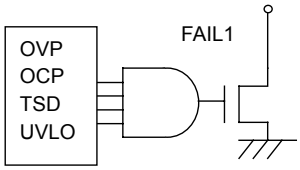
UVLO is built-in in VREG, and the circuit begins to operate when the voltage is more than 2.9V (Typ.) and stops when the voltage is less than 2.8V (Typ.).

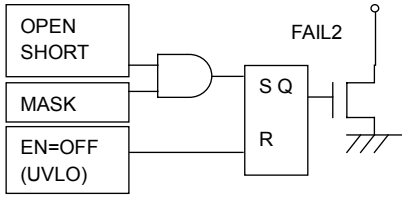
Please connect Creg=10uF (Typ.) to VREG terminal for phase compensation. The circuit's operation becomes remarkably unstable when Creg is not connected.

● Self-diagnosis function

The operating condition of the built-in protection circuit is transmitted to FAIL1 and FAIL2 output pins (open drain).

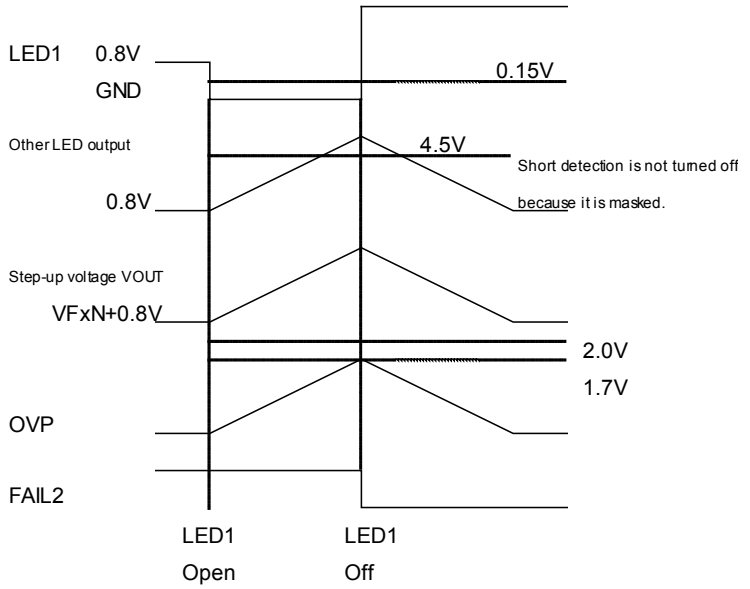
When UVLO, OVP, OCP or TSD is operated, FAIL1 output becomes L SWOUT is fixed to L, and the step-up conversion is stopped. For OCP, SWOUT is fixed to L for only 1 cycle of FOSC because of the pulse-to-pulse mode operation. For UVLO, OVP, TSD operations, LED output pins become open (Hi-Z) . When FAIL1 becomes L, LOADSW is turned off as they are inverted to each other.





FAIL2 output becomes L when open or short is detected. The open/short detection is a latch mode, and the latch is released by ON/OFF (UVLO) of EN. The device judges as open when LED output is lower than 0.15V (Typ.) as well as when the voltage of OVP terminal reaches 1.7V (Typ.). The short is detected when LED output becomes more than 4.5V (Typ.). Therefore, there is a possible scenario that short detection cannot be carried out if the difference between LED terminal voltage at the time of being normal and LED terminal voltage at the time of being abnormal is less than 3.7V (4.5V-0.8V) (Typ.). As for short detection hereon, if one LED in some column of LED output, for example, becomes short mode, and is in the status of nothing but VF being low, then cathode voltage is in the status of nothing but VF being high. LED short detection and OCP are separate protection circuits. Please take care because short detection is masked as soon as open/short is detected. However, the open detection operates. An additional capacitance added to LED output slows down the operation and the short may be detected.

For the two FAIL output pins, add pull-up resistors for each as they are open drain.



● Constant-current driver

Please turn off the output with LEDEN if there is constant-current driver output that is not used. The truth-table is shown below. If constant-current driver output that is not used is not treated with LEDEN but is made open, then the open detection will operate. Also, please do not short the driver output to GND as the inputs of the error amplifier cannot be deactivated with LEDEN. Instead keep the driver output to open or short it to VREG.

LED EN		LED			
〈1〉	〈2〉	1	2	3	4
L	L	ON	ON	ON	ON
H	L	ON	ON	ON	OFF
L	H	ON	ON	OFF	OFF
H	H	ON	OFF	OFF	OFF

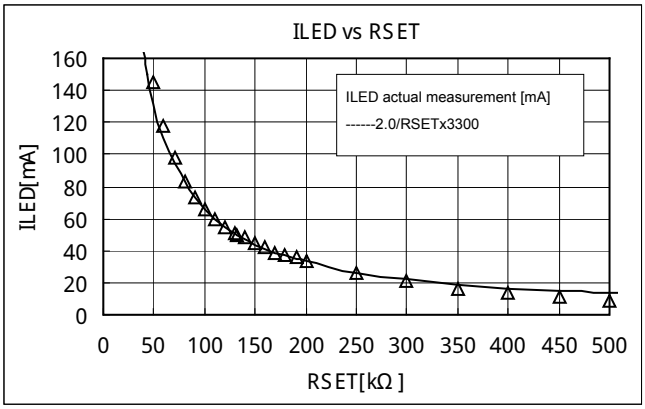
・**Setting method of output current**

ILED=min[VDAC , VISET(=2.0V)] / RSET x 3300 [mA]

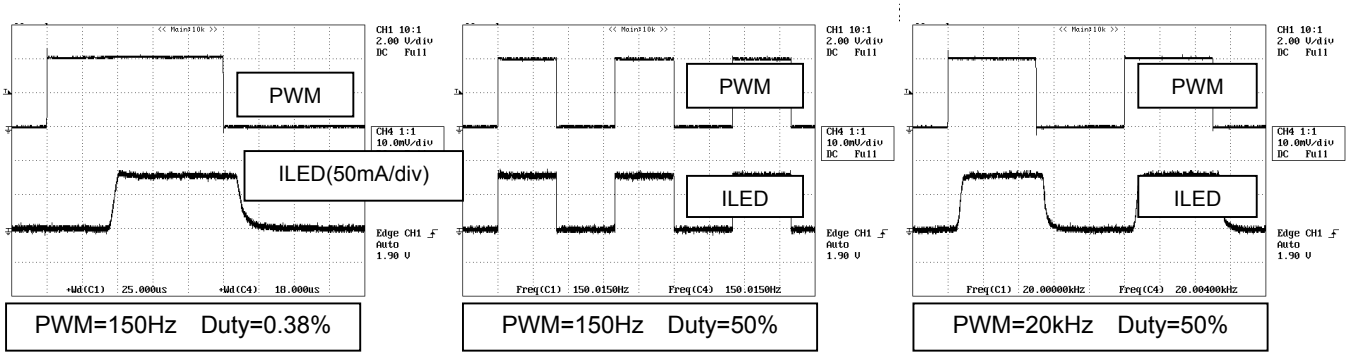
min[VDAC , 2.0V] means the selection of smaller value is between VDAC or VISET(=2.0V).

3300 (Typ.) is a constant number determined by the circuit inside.

When the output current needs to be controlled with VDAC, please input in the range of 0.1 ~ 2.0V. In the case of more than 2.0V, the value of VISET is selected in such a way that it is given by the above-mentioned calculating formula. Please connect VDAC with VREG if VDAC is not to be used. The open state of VDAC will cause malfunction. Please do not change the LED EN status during the PWM operation. The following diagram shows the relation between RISET and ISET.



For the intensity control with PWM, the ON/OFF of current driver is controlled by PWM terminal. The duty ratio of PWM terminal becomes the duty ratio of ILED. Please fix the PWM terminal to H if PWM intensity control is not to be used (100%). It becomes brightest at the time of 100%. It is recommended to use a low-pass filter (cut off frequency: 30 kHz) for the PWM pin.



● **Step-up DC/DC controller**

・**Number of LEDs in series connection**

Output voltage of the step-up converter is controlled such that the LED output pin becomes 0.8V (Typ.). Step-up operation is performed only when LED output is operating. When more than one LED outputs are operating, the LED output in the column in which the LED's VF is the highest is controlled in such a way that it becomes 0.8V (Typ.).

The voltage of other LED outputs are increased with the portion of variation becomes high voltage. Please use the following equation to calculate allowable VF variation.

VF variation allowable voltage 3.7V (Typ.)

= short detecting voltage 4.5V (Typ.) − LED control voltage 0.8V (Typ.)

In addition, pay attention to the number of LED's connection in series because it has the following limits. In case of the open detection, 85% of OVP setting voltage becomes trigger, so the maximum value of step-up voltage under normal operation becomes 30.6V=36V x 0.85 and 30.6V / VF > maximum N number.

・ **Overvoltage protection circuit OVP**

For the OVP terminal, apply the voltage divider of the step-up converter output. The setting value of OVP is determined by LED's total numbers in series connection and VF variation. Please also take OVPx0.85, which is the open detection trigger, into consideration when determining OVP setting voltage. Once the OVP operates, the OVP is released when step-up voltage drops to 77.5% of OVP setting voltage.

Suppose ROVP1 (step-up voltage side) ,ROVP2 (GND side) and step-up voltage VOUT,

Then VOUT>=(ROVP1+ROVP2)/ROVP2 x 2.0V. The OVP operates at the time of ROVP1=330kΩ, ROVP2=22kΩ and VOUT= over 32V.

・**Oscillating frequency FOS of step-up DC/DC converter**

Triangular wave oscillating frequency can be set by connecting a resistor to RT (26Pin). RT determines the charging & discharging currents for internal condenser, and the frequency changes. Please refer to the following theoretical formula when setting the RT's resistance. The range of 62.6kΩ ~ 523kΩ is recommended. The setting that deviates from the frequency range in the following diagram may cause the switching to stop and has no guarantee of proper operation, so please be careful.

30×10^{6}[V/A/S] is a constant number (±16.6%) determined by the circuit inside, and α is the correction factor.

(RT :α = 50kΩ: 0.98 , 60 kΩ: 0.985, 70 kΩ: 0.99, 80 kΩ: 0.994, 90 kΩ: 0.996, 100kΩ: 1.0,
150kΩ: 1.01, 200kΩ: 1.02,300kΩ: 1.03 , 400kΩ: 1.04 , 500kΩ: 1.045)

$$fosc = \frac{30 \times 10^{6}}{RT\ [\Omega]} \times \alpha\ [kHz]$$

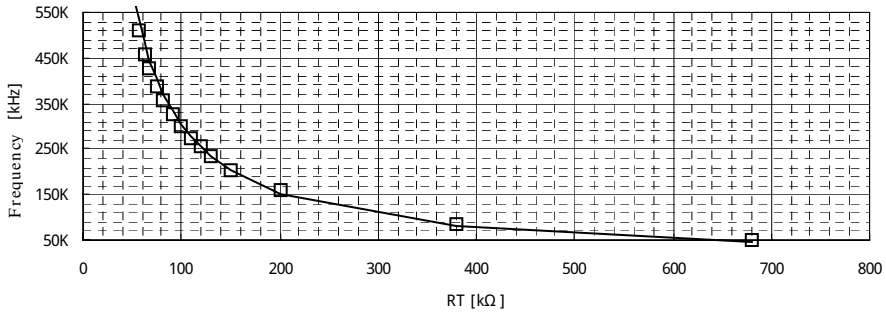


Fig.15 RT versus switching frequency

・ **External synchronization oscillating frequency FSYNC**

Please do not switch over to the internal oscillation etc. halfway when clock is being inputted to SYNC terminal for the purpose of external synchronization for step-up DC/DC converter. From having switched the SYNC terminal from H to L till the internal oscillating circuit begins to operate, there is a delay time of about 30usec (Typ.). For the clock inputted to SYNC terminal, only the rising edge is effective. Moreover, if external input frequency is later than internal oscillating frequency, the internal oscillating circuit begins to operate after the above-mentioned delay time, so please do not input something like that (the above-mentioned input).

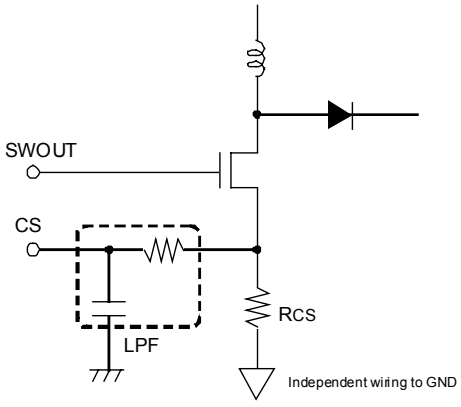
・**Overcurrent protection circuit OCP**

Please put (insert) the detecting resistor RCS between GND and the source of n-MOSFET for step-up DC/DC converter. In addition, please insert the low pass filter (LPF) with 1 ~ 2MHz cutoff frequency between the CS terminal and the detecting resistor in order to reduce the switching noise. If the time constant is too large, then the rising edge of CS terminal voltage is delayed, and it gets late that OCP operates. (RLPF=100Ω and CLPF=1000pF etc. are effective at the time of FOSC=300kHz.)

The detecting current is as follows.

IOCP=VOLIMIT0.4V / RCS [A]

OCP is of pulse by pulse mode, and SWOUT is fixed to L for only 1 cycle determined by FOSC. In addition, there is a large current line between RCS− GND, so please pay special attention and make an independent wiring to GND while board designing.



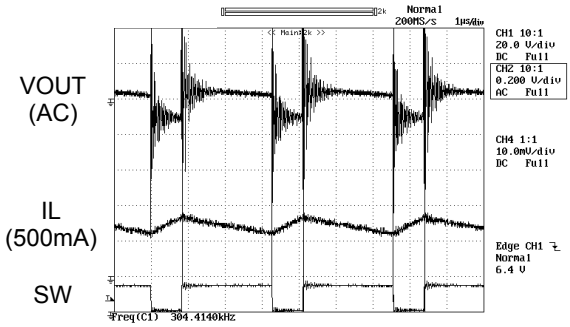


Fig.16 Ripple current & voltage

・**Soft start SS**

For this IC, the SS terminal is not used, so please use the IC with the SS terminal open.

Moreover, the open/short detecting function is masked until SS terminal voltage reaches the VSS clamp voltage 2.5V (Typ.) .

- Selection of External Parts

1. Selection of Coil (L)

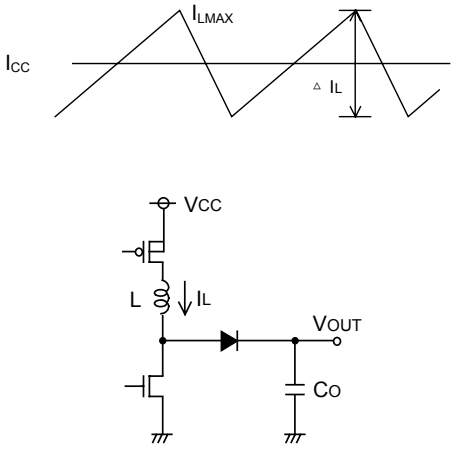


Fig.17 Output ripple current

The coil's value greatly affects the input ripple current. As shown in formula (1), the ripple current decreases as the coil becomes larger or the switching frequency increases.

$$\Delta I_L = \frac{(V_{OUT}-V_{CC}) \times V_{CC}}{L \times V_{OUT} \times f} \quad [A] \cdots (1)$$

When efficiency is represented as in (2), the input peak current is as shown in (3).

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{CC} \times I_{CC}} \quad \cdots (2)$$

$$I_{LMAX} = I_{CC} + \frac{\Delta I_L}{2} = \frac{V_{OUT} \times I_{OUT}}{V_{CC} \times \eta} + \frac{\Delta I_L}{2} \quad [A] \cdots (3)$$

※ If current which exceeds the coil's rated current value is run through the coil, the coil causes magnetic saturation and efficiency decreases. Please keep a suitable margin so that the peak current does not exceed the coil's rated current value, when selecting the current.

※ Please select coil with low resistance components (DCR and ACR) in order to minimize loss and improve efficiency.

2. Setup of Output Condenser (Co)

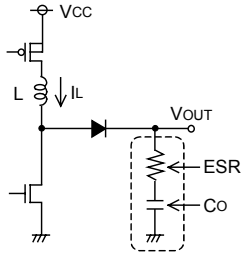


Fig.18 Output condenser

The output condenser should be decided on after careful consideration of the stable zone of the output voltage and the necessary equivalent series resistance to smooth the ripple voltage.

The output ripple voltage is decided as shown in formula (4).

$$\triangle V_{OUT} = I_{LMAX} \times R_{ESR} + \frac{1}{C_O} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f} \quad [V] \cdots (4)$$

(Δ IL: output ripple current, ESR: equivalent series resistance of Co, η : efficiency)

※ When selecting the condenser rating, keep a suitable margin for the output voltage.

3. Selection of Input Condenser (Cin)

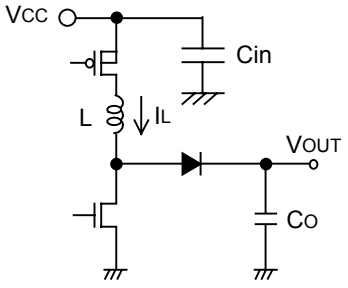


Fig.19 Input condenser

It is necessary to select a low-ESR input condenser that can adequately deal with large ripple currents in order to prevent excess voltage.
The ripple current IRMS is derived from formula (5).

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{(V_{OUT}-V_{CC}) \times V_{OUT}}}{V_{OUT}} \quad [A] \cdots (5)$$

Also, because it depends greatly on the characteristics of the power supply used for input, the wiring pattern of the substrate and the MOSFET gate-drain capacity, it is highly recommended that usage temperature, load range and MOSFET conditions are adequately confirmed.

4. About MOSFET for Load Switch and the Corresponding Soft Start

With regular booster applications, because no switch exists on the route from VCC to VO, there is the threat of output short-circuit or destruction of the commutation diode. To avoid this, please insert a PMOSFET load switch between VCC and the coil. PMOSFET that can withstand higher pressure than VCC between both the gate sources and drain sources should be selected.

Also, if a load switch soft start is desired, please insert capacity between the gate source. Refer to figure 21 when deciding on the soft start time. However, the soft start time changes depending on the gate capacity of PMOSFET.

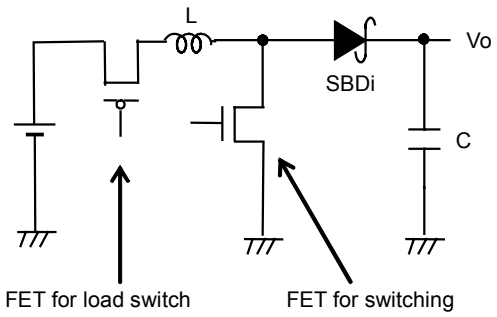


Fig.20 Load Switch Circuit Diagram

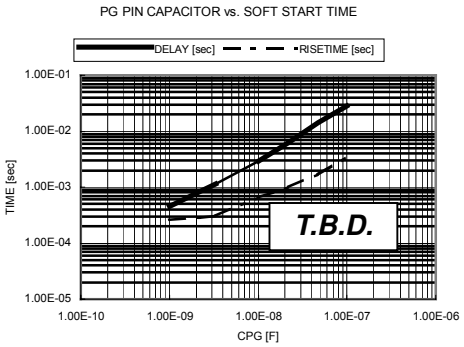


Fig.21 PG Capacity vs. Soft Start Time

5. Selection of Switching MOSFET

Although there is no problem as long as the absolute maximum rating is the rated current of L and at least C's pressure capacity and commutation diode's VF, to actualize high-speed switching, one with small gate capacity (injected charge amount) should be selected.

※ Excess current protection setup value or higher recommended.

※ High efficiency can be achieved if one with low ON resistance is selected.

6. Selection of Commutation Diode

Please select a Schottky barrier diode with greater current capability than L's rated current and reverse-pressure capacity greater than C's pressure capacity, especially with low forward voltage VF.

- Phase Compensation Setup Rules

・Stability Conditions of Applications

The stability conditions related to negative feedback are as follows:

・When the gain is 1 (0dB) and the phase-lag is under 150 ° (therefore with a phase margin of over 30º)

Also, a DC/DC converter application samples the switching frequency, so the GBW of the entire series is set to 1/10 below the switching frequency. To summarize, the characteristics targeted by the application are as below:

・When the gain is 1 (0dB) and the phase-lag is under 150 º (therefore with a phase margin of over 30 º)

・GBW (frequency at gain 0dB) at that time is 1/10 below the switching frequency

Therefore, to improve response with GBW limits, the switching frequency must be higher.

A trick to secure stability with phase compensation is to cancel the second phase-lag (-180 º) caused by the LC resonance with the second phase-lead (put in two phase-leads).

Phase-lead is by the ESR component of the output condenser and the CR of the error amp output Comp terminal.

With a DC/DC converter application, because there is always an LC resonance circuit at the output, the phase-lag at that area is -180º. When the output condenser is one with a large ESR (several Ω), such as a aluminum electrolysis condenser, there is a phase-lead of +90º, and the phase-lag is -90º. When an output condenser with low ESR such as a ceramic condenser is used, an R for the ESR component should be inserted.

LC Resonance

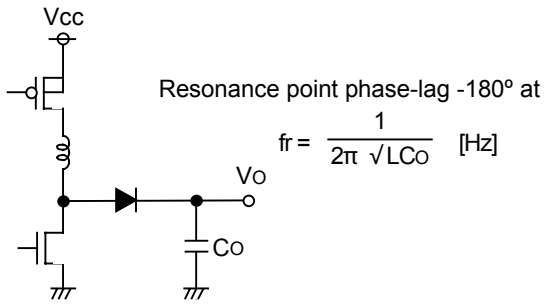


Fig.22

With ESR

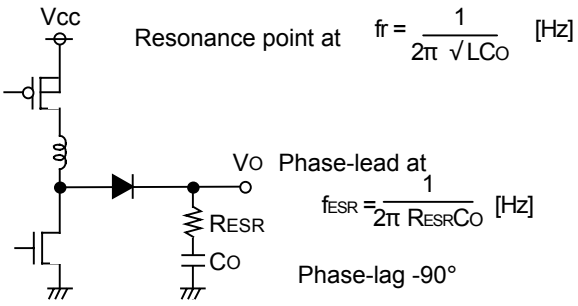


Fig.23

Because of the changes in phase characteristics caused by ESR, one lead-phase should be inserted.

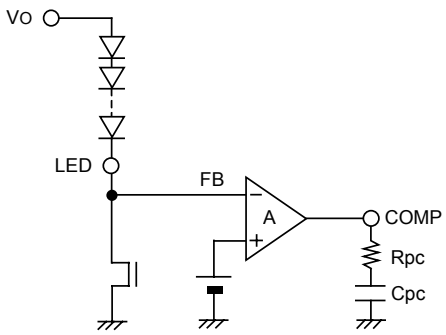


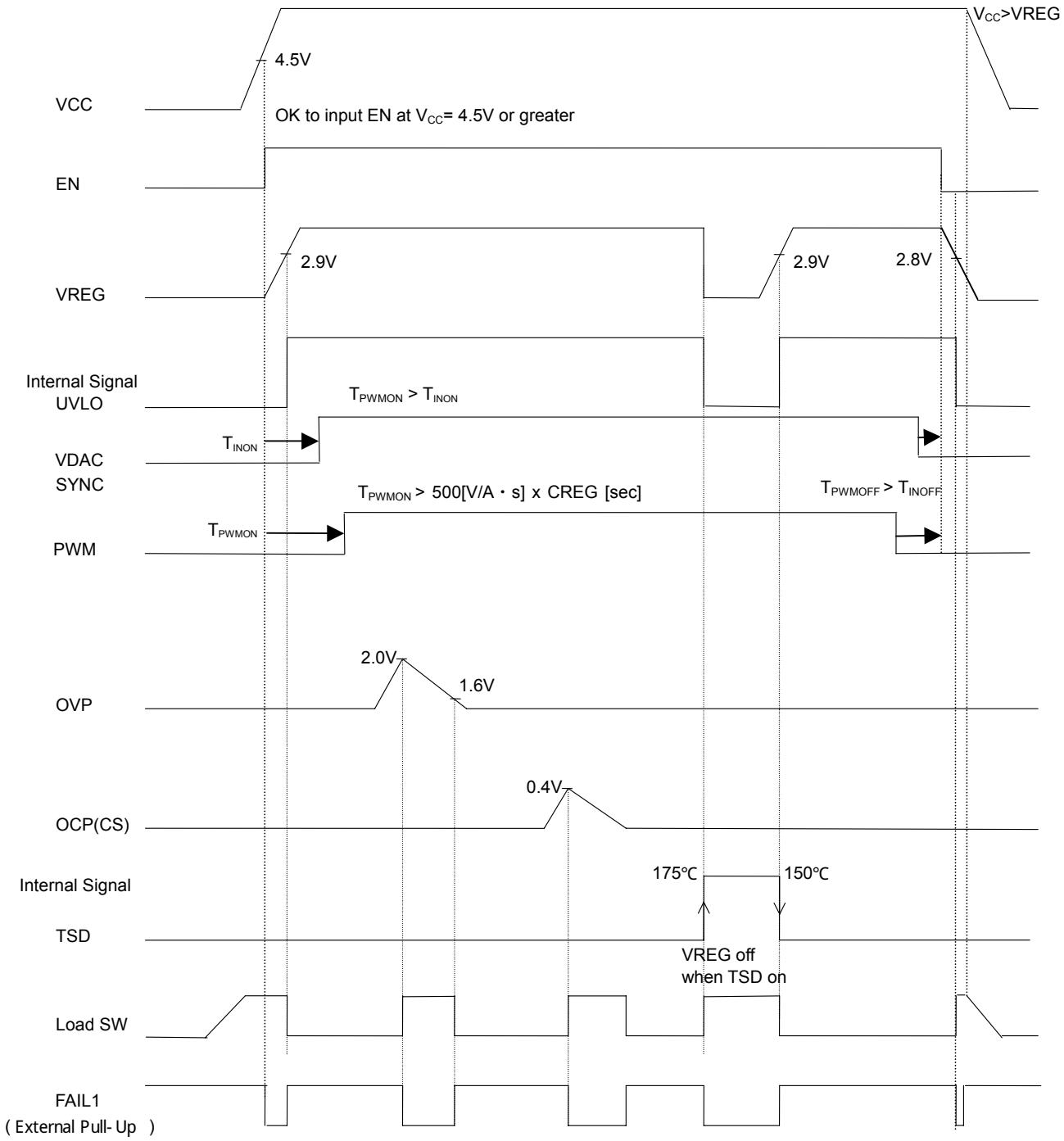
Fig.24

Phase-lead $fz = \frac{1}{2\pi\ CpcRpc}$ [Hz]

To setup the frequency to insert the phase-lead, for the aim of canceling the LC resonance, ideally it should be set in the area of the LC resonance frequency.

Because this setup was very basically designed and strict calculations have not been made, adjustments with the actual equipment may be required. Also, these characteristics change depending on factors such as different substrate layouts and load conditions, therefore when designing for mass production, adequate confirmations with actual equipment must be made.

- Sequence



※ Fix LEDEN1 and 2 before input.

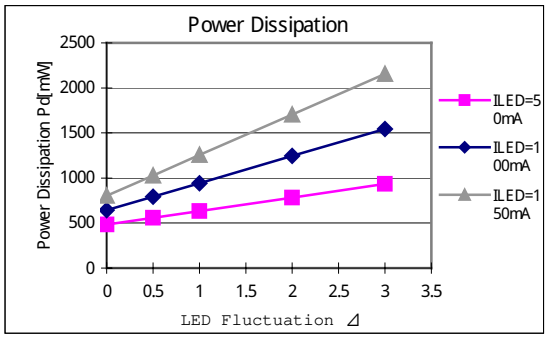
Fig.25

- Power Dissipation Calculation

Pd(N) = ICC*VCC + Ciss*Vsw*fsw*Vsw + Rload*(Iload)^2 + [VLED*N+⊿Vf*(N-1)]*ILED
ICC: Maximum circuit current
VCC: Supply power voltage
Ciss: External FET capacity
Vsw: SW gate voltage
Fsw: SE frequency
Rload: LOAD SW ON resistance
Iload: LOAD SW maximum input current
VLED: LED control voltage
N: LED parallel numeral
△ Vf: LED Vf fluctuation
ILED: LED output current

< Sample Calculation >

Pd(4) = 10mA × 30V + 500pF × 5V × 300kHz × 5V + 15Ω × $(10mA)^2$ + [0.8V × 4 + △ Vf × 3] × 100mA
If △ Vf = 3.0V,
Pd(4) = 324mW + 1220mW = 1544mW



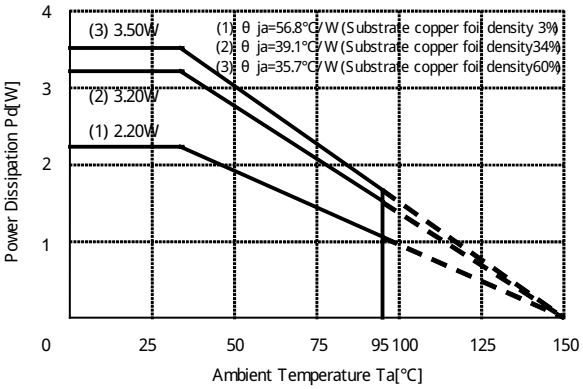


Fig.26

Note 1: The value of power dissipation is when mounted on 70mm X 70mm X 1.6mm glass epoxy substrate (1-layer platform/copper thickness 18μ m)
Note 2: The value changes with the copper foil density of the platform. However, this value represents observed value, not guaranteed value.

Pd=2200mW (968mW): Substrate copper foil density 3%
Pd=3200mW (1408mW): Substrate copper foil density34%
Pd=3500mW (1540mW): Substrate copper foil density 60% Value within brackets represent power dissipation when Ta=95℃

- Efficiency of Switching Power Supply

Efficiency η is represented in the following formula:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{Vin \times Iin} \times 100[\%] = \frac{P_{OUT}}{Pin} \times 100[\%] = \frac{P_{OUT}}{P_{D(IC)} + P_{D\alpha}} \times 100[\%]$$

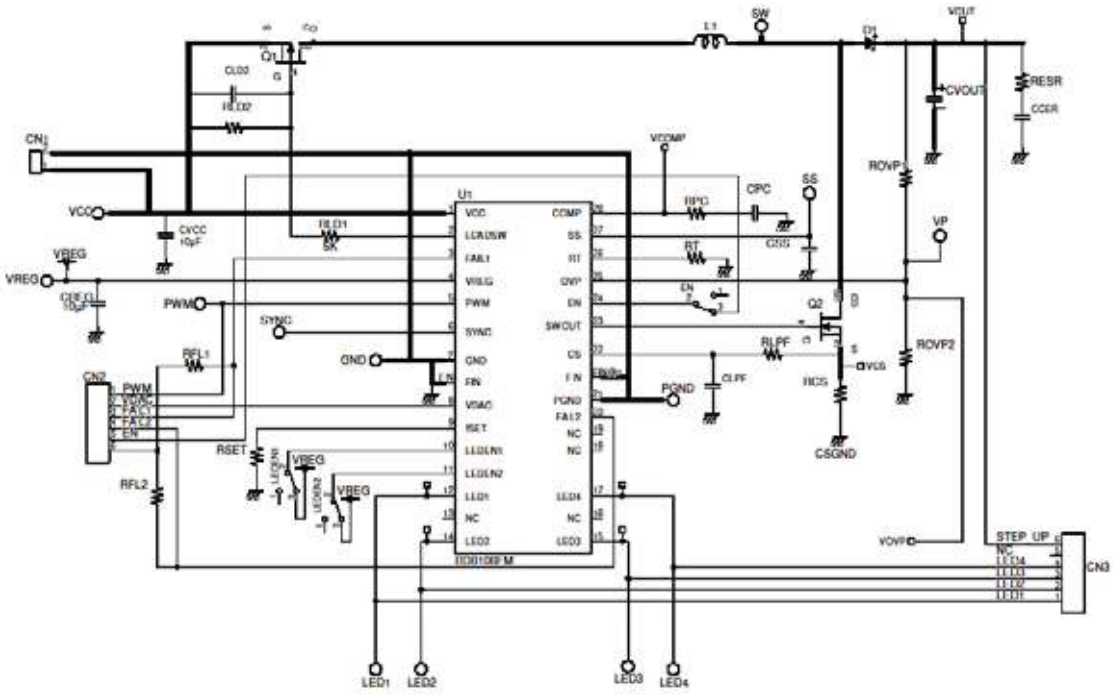
The main causes for power dissipation of the switching regulator $P_{D\alpha}$ are as listed below, and efficiency can be improved by lessening these causes.

< Main Causes of Dissipation >

1) Dissipation from ON resistance of coil and FET: PD(I^2R)
2) Gate charge-discharge dissipation: PD(Gate)
3) Switch dissipation: PD(SW)
4) Condenser's ESR dissipation: PD(ESR)
5) IC's operational current dissipation: PD(IC)

1) PD(I^2R) = I_{OUT}^2× (R_{COIL}× R_{ON}) (R_{COIL}[Ω]: coil resistance, R_{ON}[Ω]: ON resistance of FET, I_{OUT}[A]: Output current)
2) PD(Gate) = C_{SW}× f_{SW}× V_{SW} (C_{SW}[F]: Gate capacity of FET, f_{SW}[Hz]: Switching frequency, V_{SW}[V]: Gate drive voltage of FET)
3) PD(SW) = $\frac{Vin^2 \times C_{RSS} \times I_{OUT} \times f_{SW}}{I_{Drive}}$ (C_{RSS}[F]: Reciprocal transmission capacity of FET, I_{Drive}[A]: Peak

4) PD(ESR) = I_{RMS}^2× ESR (I_{RMS}[A]: Ripple current of condenser, ESR[Ω]: Equivalent Series Resistance)
5) PD(IC) = Vin× I_{CC} (I_{CC}[A] : Circuit Current)



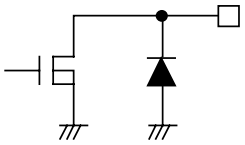
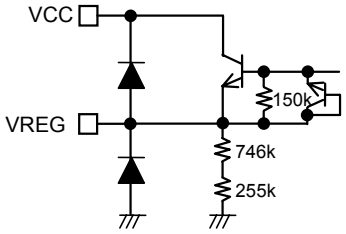
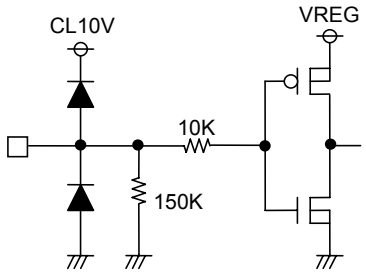
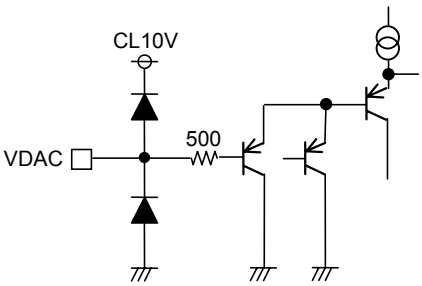
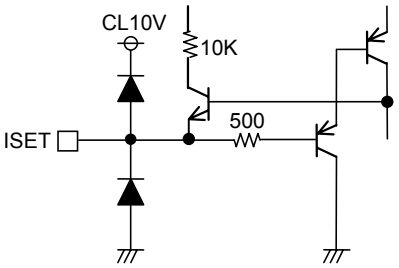
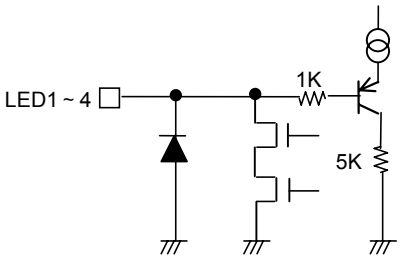
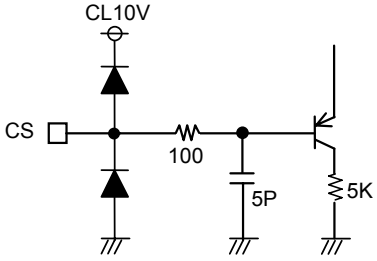
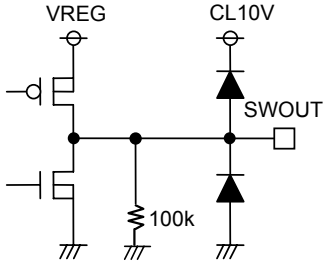
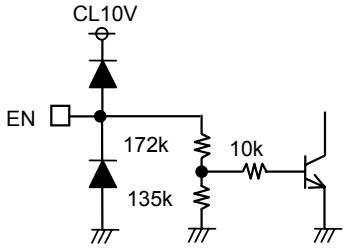
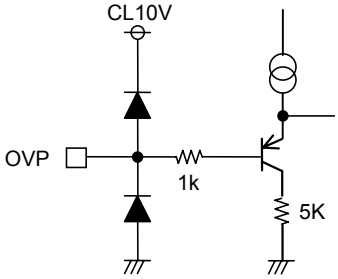
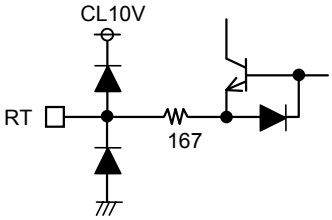
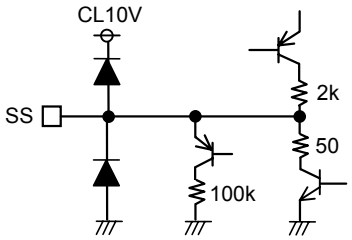
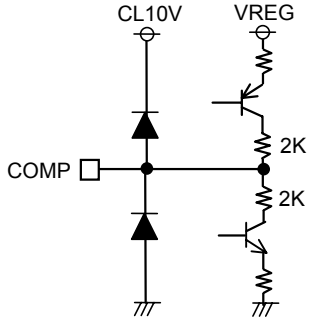
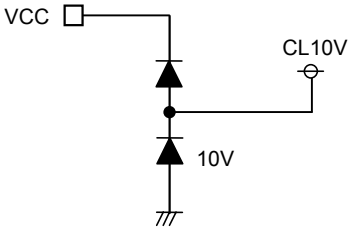
- The decoupling condensers CVCC and CREG should be placed as close as possible to the IC pin.
- There is a possibility that a large current is sent to CSGND and PGND, so each should be independently wired, and at the same time impedance should be lowered.
- Take care that there is no noise riding on 8pin VDAC, 9pin ISET, 26pin RT and 28pin Comp.
- 5pin PWM, 6pin SYNC and 12-17pin LED1-4 all switch, therefore be careful that the periphery pattern is unaffected.
- The areas with thick lines should be laid out as short as possible with wide patterns.

- PCB Board External Parts List

Setting place	Value	Product Name	Manufacturer
RLD1	5.1kΩ	MCR03Series5101	ROHM
RLD2	5.1kΩ	MCR03Series5101	ROHM
RFL1	5.1kΩ	MCR03Series5101	ROHM
RFL2	5.1kΩ	MCR03Series5101	ROHM
RPC	820Ω	MCR03Series8200	ROHM
RT	100kΩ	MCR03Series1003	ROHM
ROVP1	330kΩ	MCR03Series3303	ROHM
ROVP2	22kΩ	MCR03Series2202	ROHM
RCS	0.1Ω	MCR10SeriesR10	ROHM
RSET	100kΩ	MCR03Series1003	ROHM
CPC	2.2uF	T.B.D.	murata
CSS	-	-	-
CVCC	10uF	GRM21BB31C106KE15	murata
CREG	10uF	GRM21BB31C106KE15	murata
Q1	-	RSS090P03FU6TB	ROHM
Q2	-	SP8K22FU6TB	ROHM
L1	47uH	CDRH8D38NP-470NC	Sumida
D1	-	RB160L-60TE25	ROHM
CVOUT	220uF	25YK220M0611	Rubycon
RLPF	100Ω	MCR03Series1000	ROHM
CLPF	1000pF	T.B.D.	murata
CLD2	1uF	T.B.D.	murata

※ The above values are fixed numbers for confirmed operation when VCC=12V, LED 5-straight 4-parallel and ILED=50mA. Therefore, because the optimal value varies depending on factors such as usage conditions, the fixed numbers should be decided on after careful assessment.

- In/Output Equivalent Circuits (Terminal names surrounded by parentheses)

2. LOADSW, 3. FAIL1, 20. FAIL2	4. VREG	5. PWM, 6. SYNC, 10. LEDEN1, 11. LEDEN2
		
8. VDAC	9. ISET	12. LED1, 14. LED2, 15. LED3, 17. LED4
		
22. CS	23. SWOUT	24. EN
		
25. OVP	26. RT	27. SS
		
28. COMP	13, 16, 18, 19 N.C.	CL10V
	 N.C. is open.	

※ The value are all Typ. value.

●Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

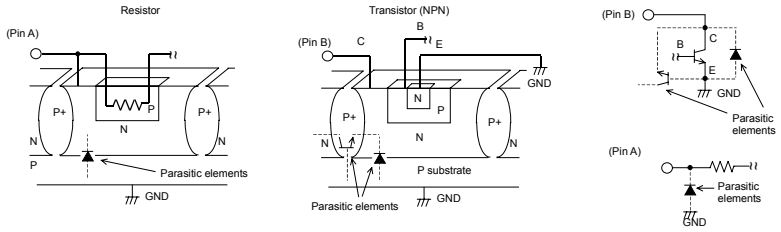
8) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when the resistors and transistors are connected to the pins as shown in Fig. 41, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

Example of a Simple Monolithic IC Architecture



9) Overcurrent protection circuits

An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. The circuit automatically resets once the junction temperature Tj drops.

Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards

At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

●Selecting a Model Name When Ordering

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