RENESAS

3.3V CMOS 16-BIT BUS TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

IDT74LVCH16646A
NOT RECOMMENDED FOR NEW DESIGNS

FEATURES:

- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 3.3V ± 0.3V, Normal Range**
- **V_{CC} = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4μ W typ. static)**
- **All inputs, outputs, and I/O are 5V tolerant**
- **Supports hot insertion**
- **Available in TSSOP package**

DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Reduced system switching noise**

APPLICATIONS:

- **5V and 3.3V mixed voltage systems**
- **Data communication and telecommunication systems**
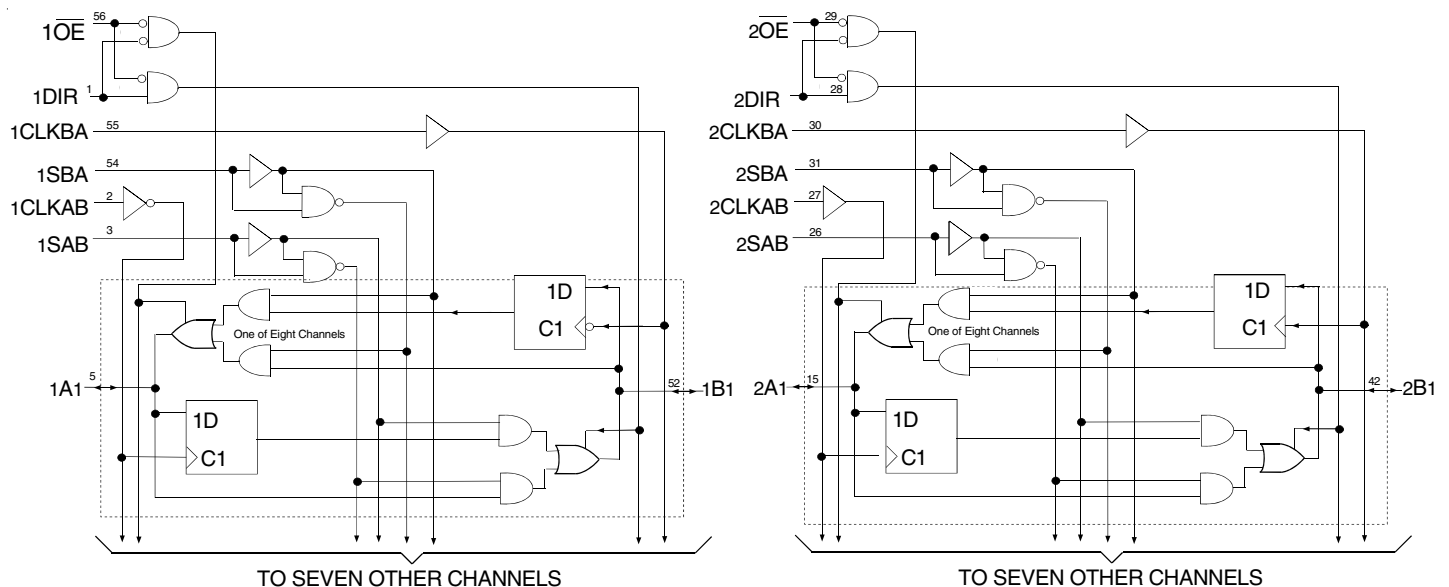
DESCRIPTION:

The LVCH16646A 16-bit bus transceiver and register is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type transceivers with 3-state D-type registers. The controls circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (DIR), over-riding Output Enable control ($\overline{OE}$) and Select lines (SAB and SBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the low-to-high transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.
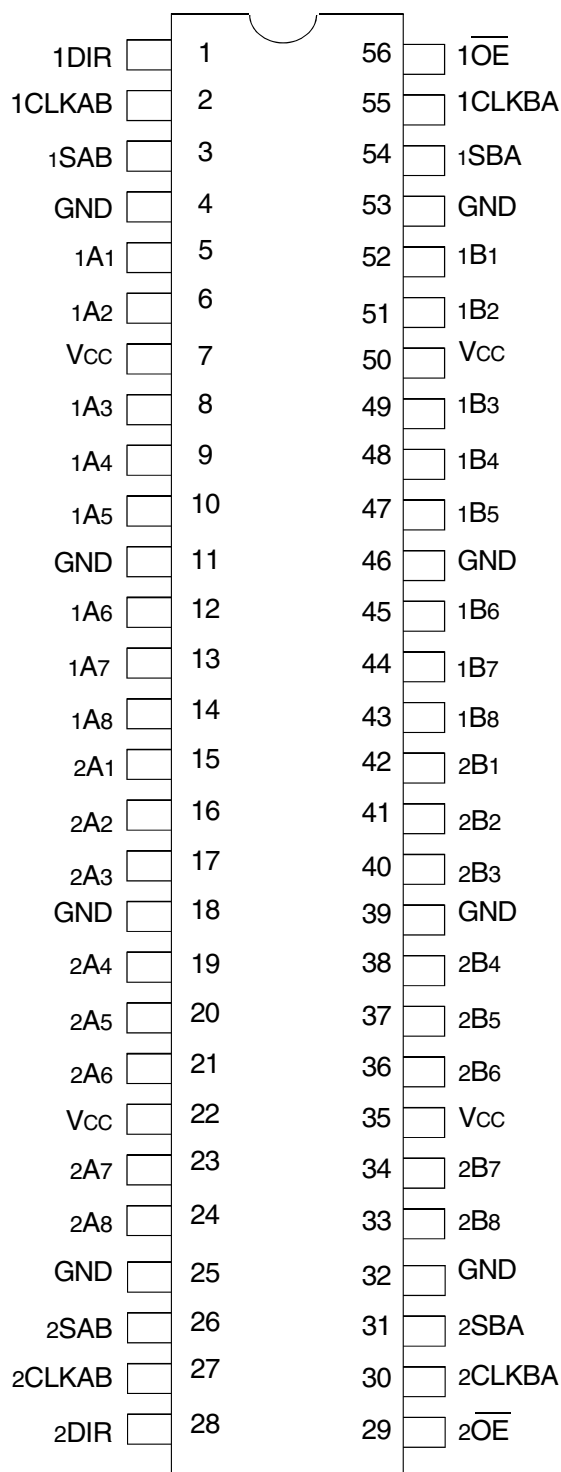
The LVCH16646A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16646A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

TO SEVEN OTHER CHANNELS

TO SEVEN OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

JANUARY 2016

DSC-3787/5

PIN CONFIGURATION

1DIR	1		56	1$\overline{OE}$
1CLKAB	2		55	1CLKBA
1SAB	3		54	1SBA
GND	4		53	GND
1A1	5		52	1B1
1A2	6		51	1B2
Vcc	7		50	Vcc
1A3	8		49	1B3
1A4	9		48	1B4
1A5	10		47	1B5
GND	11		46	GND
1A6	12		45	1B6
1A7	13		44	1B7
1A8	14		43	1B8
2A1	15		42	2B1
2A2	16		41	2B2
2A3	17		40	2B3
GND	18		39	GND
2A4	19		38	2B4
2A5	20		37	2B5
2A6	21		36	2B6
Vcc	22		35	Vcc
2A7	23		34	2B7
2A8	24		33	2B8
GND	25		32	GND
2SAB	26		31	2SBA
2CLKAB	27		30	2CLKBA
2DIR	28		29	2$\overline{OE}$

TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +6.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T$_A$ = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs[1]
	Data Register B Outputs
xBx	Data Register B Inputs[1]
	Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
x$\overline{OE}$	Output Enable Inputs
xDIR	Direction Control Inputs

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE[1]

Inputs						Data I/O[2]		
x$\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	Operation or Function
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified[2]
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified[2]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

NOTES:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   ↑ = LOW-to-HIGH transition
2. The data output functions may be enabled or disabled by various signals at the x$\overline{OE}$ or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
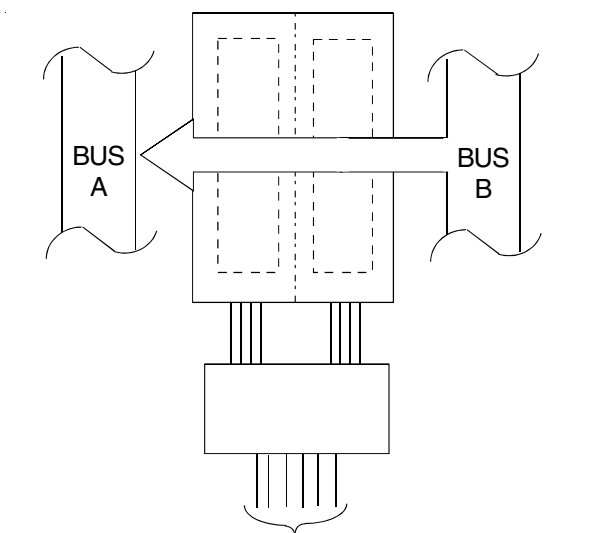
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
			3.6 ≤ V_{IN} ≤ 5.5V[2]	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	500	µA

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

xDIR	x$\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to A
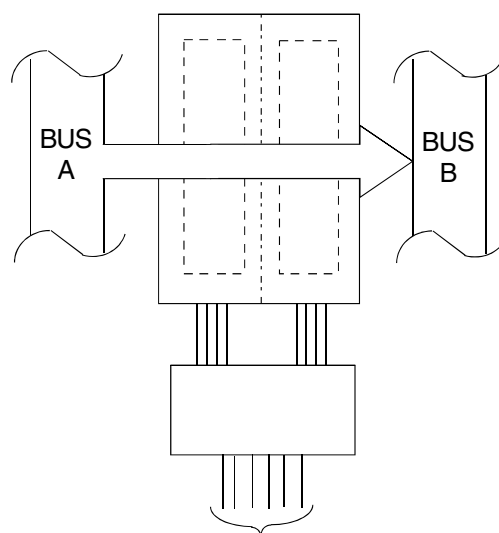
xDIR	x$\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to B
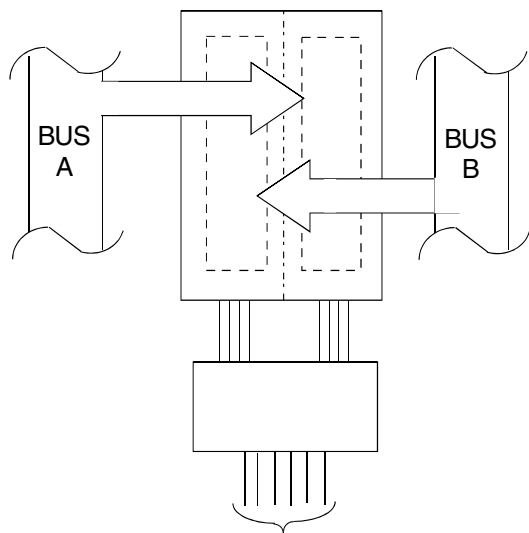
xDIR	x$\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
X	X	↑	X	X	X
X	X	X	↑	X	X
X	H	↑	↑	X	X

Storage from
A, B, or A and B
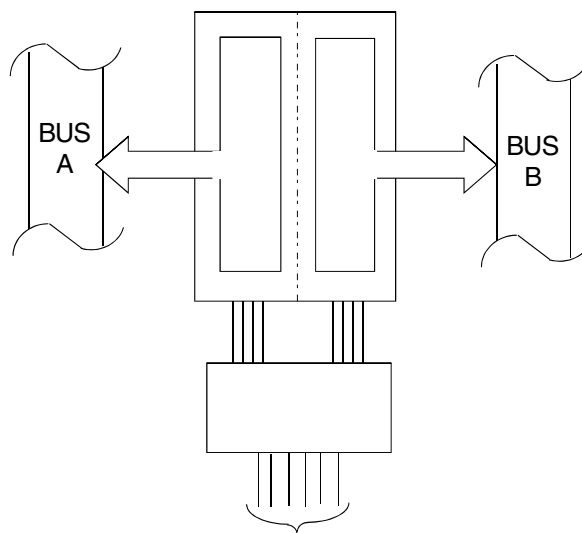
xDIR	x$\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stored
Data to A and/or B

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3V	V_I = 2V	−75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	—	—	—	µA
I_{BHL}			V_I = 0.7V	—	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	±500	µA
I_{BHLO}							

NOTES:
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = − 0.1mA	V_{CC} − 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = − 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = − 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = − 24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.
   T_A = − 40°C to + 85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per Transceiver Outputs enabled	C_L = 0pF, f = 10Mhz	60	pF
C_{PD}	Power Dissipation Capacitance per Transceiver Outputs disabled		12	

SWITCHING CHARACTERISTICS[1]

Symbol	Parameter	Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
f_{MAX}		150	—	150	—	MHz
t_{PLH}	Propagation Delay	—	6.8	1.3	5.7	ns
t_{PHL}	xAx to xBx or xBx to xAx					
t_{PLH}	Propagation Delay	—	7.9	1.8	6.7	ns
t_{PHL}	xCLKBA or xCLKAB to xAx or xBx					
t_{PLH}	Propagation Delay	—	9.2	1.7	7.7	ns
t_{PHL}	xSBA or xSAB to xAx or xBx					
t_{PZH}	Output Enable Time	—	8.5	1.3	6.9	ns
t_{PZL}	x$\overline{OE}$ to xAx or Bx					
t_{PZH}	Output Enable Time	—	8.5	1.4	7.2	ns
t_{PZL}	xDIR to xAx or Bx					
t_{PHZ}	Output Disable Time	—	7.7	2.1	6.9	ns
t_{PLZ}	x$\overline{OE}$ to xAx or Bx					
t_{PHZ}	Output Disable Time	—	7.8	2	7	ns
t_{PLZ}	xDIR to xAx or Bx					
t_{SU}	Set-up Time	3.2	—	2.9	—	ns
	xAx or xBx before CLKAB↑ or CLKBA↑					
t_H	Hold Time	0	—	0.3	—	ns
	xAx or xBx after CLKAB↑ or CLKBA↑					
t_W	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	ns
$t_{SK(o)}$	Output Skew[2]	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$ = 3.3V±0.3V	$V_{CC}^{(1)}$ = 2.7V	$V_{CC}^{(2)}$ = 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF
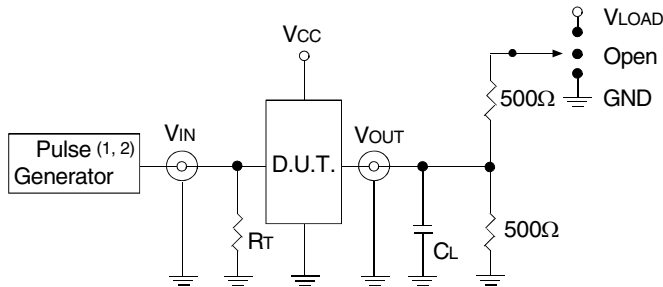
Test Circuit for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open
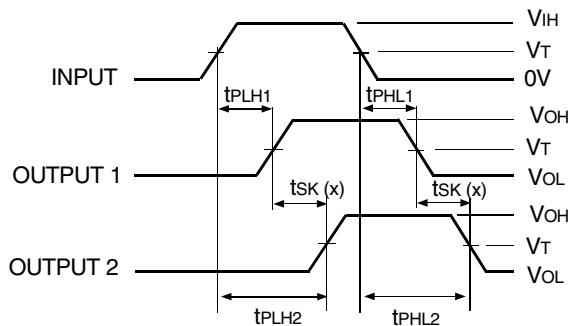
$t_{SK}(x) = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$
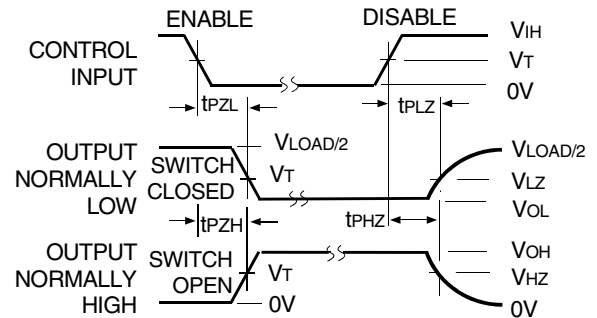
Output Skew - $t_{SK}(x)$

NOTES:
1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.
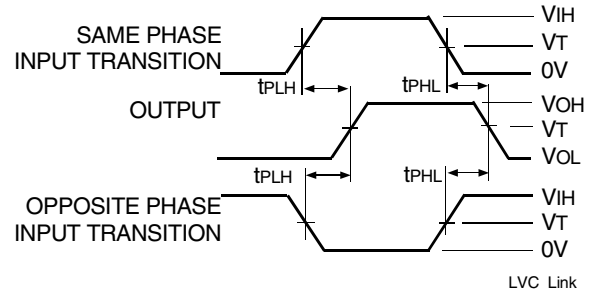
Propagation Delay

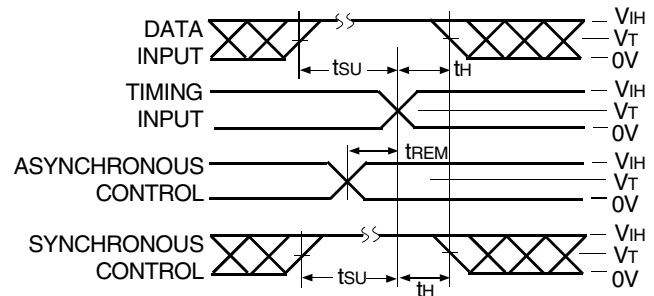*Enable and Disable Times*

NOTE:
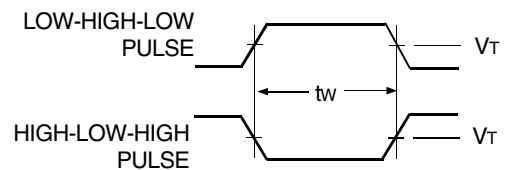1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

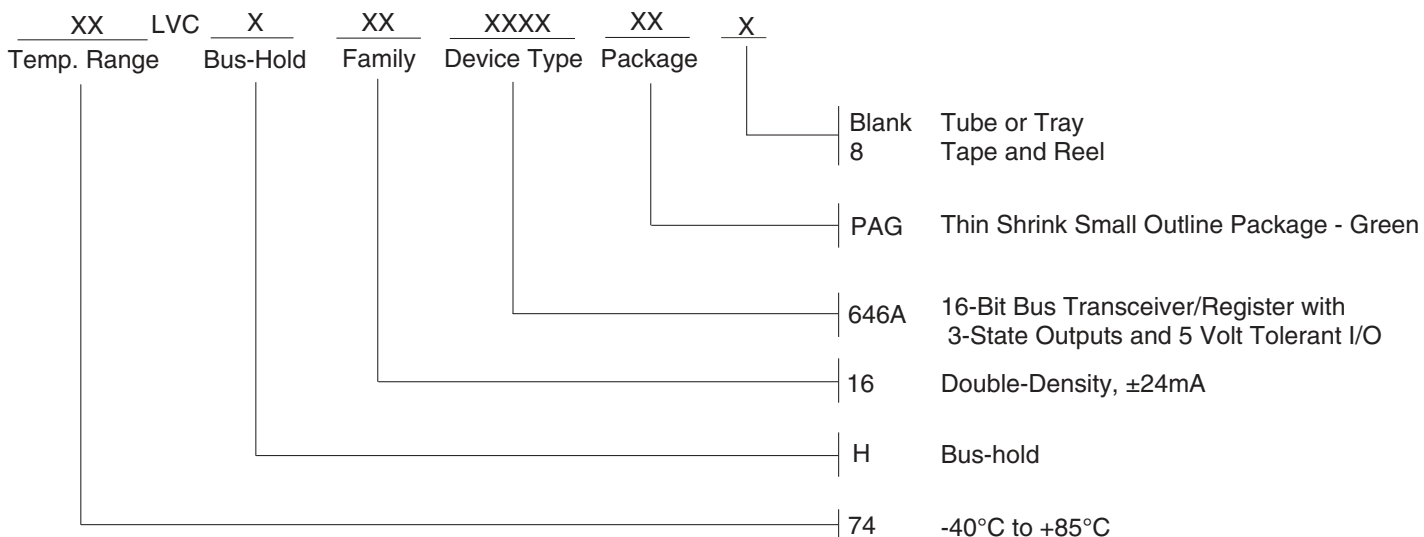*Set-up, Hold, and Release Times*

Pulse Width

ORDERING INFORMATION

```
  XX    LVC    X      XX      XXXX      XX       X
Temp. Range  Bus-Hold  Family  Device Type  Package
```

Blank	Tube or Tray
8	Tape and Reel
PAG	Thin Shrink Small Outline Package - Green
646A	16-Bit Bus Transceiver/Register with 3-State Outputs and 5 Volt Tolerant I/O
16	Double-Density, ±24mA
H	Bus-hold
74	-40°C to +85°C

DATASHEET DOCUMENT HISTORY

01/28/2016   Pg. 1, 2, 8   Updated the ordering information by removing IDT notation, non RoHS parts and adding Tape and Reel information.

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