

4086B

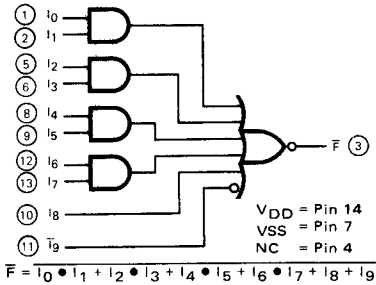
4-WIDE 2-INPUT AND-OR-INVERT GATE

DESCRIPTION — The 4086B is a 4-Wide 2-Input AND-OR-Invert (AOI) Gate with two additional inputs (I_8 and \bar{I}_9) which can be used as either expander inputs or inhibit inputs by connecting them to any standard CMOS output. A HIGH on I_8 or a LOW on \bar{I}_9 forces the Output (F) LOW independent of the other eight inputs (I_0 - I_7). The Output (F) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.

PIN NAMES

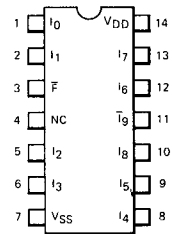
I_0 - I_8 Gate Inputs
 \bar{I}_9 Gate Input (Active LOW)
 F Output (Active LOW)

LOGIC DIAGRAM



NOTE:
 A HIGH on I_8 or a LOW on \bar{I}_9 forces the output (\bar{F}) LOW.

**CONNECTION DIAGRAM
 DIP (TOP VIEW)**



NOTE:
 The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0\text{ V}$ (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			$V_{DD} = 15\text{ V}$					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC		1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
				7.5			15			30		MAX	
	XM		0.25			0.5			1	μA	MIN, 25°C		
			7.5			15			30		MAX		

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			$V_{DD} = 15\text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, I_0 through I_8 to \bar{F}		100	180		40	80		25	64	ns	$C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$ Input Transition Times $\leq 20\text{ ns}$
t_{PHL}	I_0 through I_8 to \bar{F}		100	180		40	80		25	64	ns	
t_{PLH}	Propagation Delay, \bar{I}_9 to \bar{F}		65	100		35	50		20	40	ns	
t_{PHL}	\bar{I}_9 to \bar{F}		65	100		35	50		20	40	ns	
t_{TLH}	Output Transition Time		55	100		25	50		18	35	ns	
t_{THL}	Time		55	100		25	50		18	35	ns	

NOTES:

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

