

G3R20MT12N

1200 V 20 mΩ SiC MOSFET



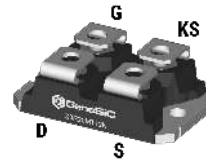
Silicon Carbide MOSFET
N-Channel Enhancement Mode

| | | |
|-----------------------------------------|---|--------|
| V _{DS} | = | 1200 V |
| R _{DS(ON)(Typ.)} | = | 20 mΩ |
| I _D (T _C = 100°C) | = | 64 A |

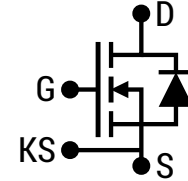
Features

- G3R™ (3rd Generation) Technology
- Softer R_{DS(ON)} v/s Temperature Dependency
- LoRing™ - Electromagnetically Optimized Design
- Smaller R_{G(INT)} and Lower Q_G
- Low Device Capacitances (C_{OSS}, C_{RSS})
- Superior Cost-Performance Index
- Robust Body Diode with Low V_F and Low Q_{RR}
- Isolated Back-Side

Package



SOT-227



D = Drain
G = Gate
S = Source
KS = Kelvin Source



Advantages

- Compatible with Commercial Gate Drivers
- Low Conduction Losses at all Temperatures
- Reduced Ringing
- Faster and More Efficient Switching
- Lesser Switching Spikes and Lower Losses
- Superior Robustness and System Reliability
- Ease of Paralleling without Thermal Runaway
- Better Power Density and System Efficiency

Applications

- Solar Inverters
- Motor Drives
- EV Charging
- High Voltage DC-DC Converters
- Switched Mode Power Supplies
- UPS
- Smart Grid Transmission and Distribution
- Induction Heating and Welding

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

| Parameter | Symbol | Conditions | Values | Unit | Note |
|-----------------------------------|-----------------------------------|--------------------------------------------------------------|------------|------|---------|
| Drain-Source Voltage | V _{DS(max)} | V _{GS} = 0 V, I _D = 100 μA | 1200 | V | |
| Gate-Source Voltage (Dynamic) | V _{GS(max)} | | -10 / +22 | V | |
| Gate-Source Voltage (Static) | V _{GS(op)-ON} | Recommended Operation | +15 to +18 | V | |
| | V _{GS(op)-OFF} | | -5 to -3 | | |
| Continuous Forward Current | I _D | T _C = 25°C, V _{GS} = -5 / +15 V | 90 | A | Fig. 15 |
| | | T _C = 100°C, V _{GS} = -5 / +15 V | 64 | | |
| | | T _C = 135°C, V _{GS} = -5 / +15 V | 46 | | |
| Pulsed Drain Current | I _{D(pulse)} | t _p ≤ 3μs, D ≤ 1%, V _{GS} = 15 V, Note 1 | 300 | A | Fig. 14 |
| Power Dissipation | P _D | T _C = 25°C | 314 | W | Fig. 16 |
| Non-Repetitive Avalanche Energy | E _{AS} | L = 1.7 mH, I _{AS} = 30.0 A | 750 | mJ | |
| Operating and Storage Temperature | T _j , T _{stg} | | -55 to 175 | °C | |

Thermal/Package Characteristics

| Parameter | Symbol | Conditions | Values | | | Unit | Note |
|-------------------------------------|-------------------|--------------------|--------|------|------|------|---------|
| | | | Min. | Typ. | Max. | | |
| Thermal Resistance, Junction - Case | R _{thJC} | | | | 0.48 | °C/W | Fig. 13 |
| Weight | W _T | | | 28.0 | | g | |
| Mounting Torque | T _M | Screws to Heatsink | | | 1.5 | Nm | |
| Terminal Connection Torque | T _C | M4 Screws | | | 1.3 | Nm | |

Electrical Characteristics (At $T_C = 25^\circ\text{C}$ Unless Otherwise Stated)

| Parameter | Symbol | Conditions | Values | | | Unit | Note |
|-----------------------------------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------|------|---------------|------------|
| | | | Min. | Typ. | Max. | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$ | 1200 | | | V | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$ | | 1 | | μA | |
| Gate Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = 22\text{ V}$ | | | 100 | nA | |
| | | $V_{DS} = 0\text{ V}, V_{GS} = -10\text{ V}$ | | | -100 | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 35.0\text{ mA}$ | 1.8 | 2.70 | | V | Fig. 9 |
| | | $V_{DS} = V_{GS}, I_D = 35.0\text{ mA}, T_j = 175^\circ\text{C}$ | | 2.05 | | | |
| Transconductance | g_{fs} | $V_{DS} = 10\text{ V}, I_D = 60\text{ A}$ | | 29.2 | | S | Fig. 4 |
| | | $V_{DS} = 10\text{ V}, I_D = 60\text{ A}, T_j = 175^\circ\text{C}$ | | 32.9 | | | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 15\text{ V}, I_D = 60\text{ A}$ | | 20 | | mΩ | Fig. 5-8 |
| | | $V_{GS} = 15\text{ V}, I_D = 60\text{ A}, T_j = 175^\circ\text{C}$ | | 29 | | | |
| | | $V_{GS} = 18\text{ V}, I_D = 60\text{ A}$ | | 17 | 22.5 | | |
| | | $V_{GS} = 18\text{ V}, I_D = 60\text{ A}, T_j = 175^\circ\text{C}$ | | 25 | | | |
| Input Capacitance | C_{iss} | | | 5814 | | pF | Fig. 11 |
| Output Capacitance | C_{oss} | | | 177 | | | |
| Reverse Transfer Capacitance | C_{rss} | | | 14.2 | | | |
| C_{oss} Stored Energy | E_{oss} | $V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$ | | 69 | | μJ | Fig. 12 |
| C_{oss} Stored Charge | Q_{oss} | | | 257 | | nC | |
| Effective Output Capacitance (Energy Related) | $C_{o(er)}$ | | | 216 | | pF | Note 2 |
| Effective Output Capacitance (Time Related) | $C_{o(tr)}$ | | | 321 | | | |
| Gate-Source Charge | Q_{gs} | $V_{DS} = 800\text{ V}, V_{GS} = -5 / +15\text{ V}$ | | 50 | | nC | Fig. 10 |
| Gate-Drain Charge | Q_{gd} | $I_D = 60\text{ A}$ | | 70 | | | |
| Total Gate Charge | Q_g | Per IEC607478-4 | | 180 | | | |
| Internal Gate Resistance | $R_{G(int)}$ | $f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$ | | 1.3 | | Ω | |
| Turn-On Switching Energy (Body Diode) | E_{on} | $T_j = 25^\circ\text{C}, V_{GS} = -5/+15\text{V}, R_{G(ext)} = 1\ \Omega, L = 32.0\ \mu\text{H}, I_D = 60\text{ A}, V_{DD} = 800\text{ V}$ | | 492 | | μJ | Fig. 22,26 |
| Turn-Off Switching Energy (Body Diode) | E_{off} | | | 201 | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 800\text{ V}, V_{GS} = -5/+15\text{V}$ $R_{G(ext)} = 1\ \Omega, L = 32.0\ \mu\text{H}, I_D = 60\text{ A}$ Timing relative to V_{DS} , Inductive load | | 45 | | ns | Fig. 24 |
| Rise Time | t_r | | | 18 | | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 20 | | | |
| Fall Time | t_f | | | 11 | | | |

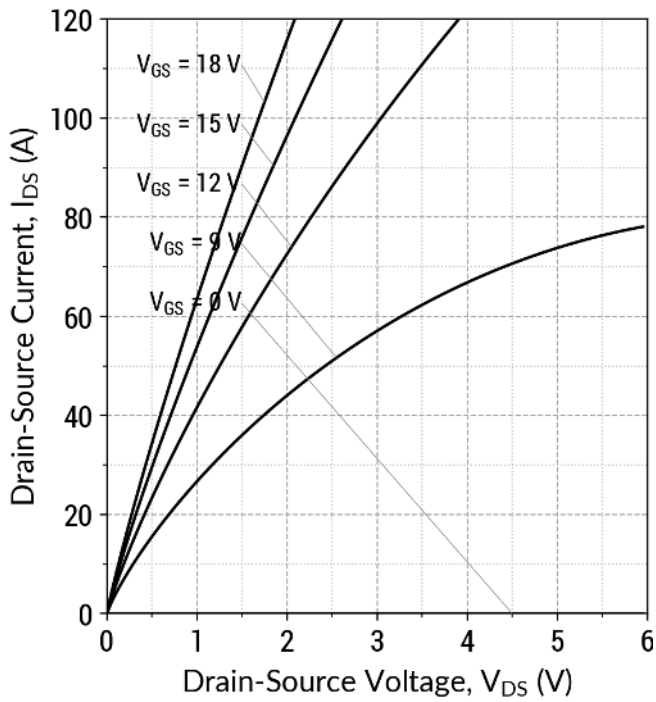
Note 1: Pulse Width t_p Limited by $T_{j(max)}$

Note 2: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 800V.
 $C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{oss} while V_{DS} is rising from 0 to 800V.

Reverse Diode Characteristics

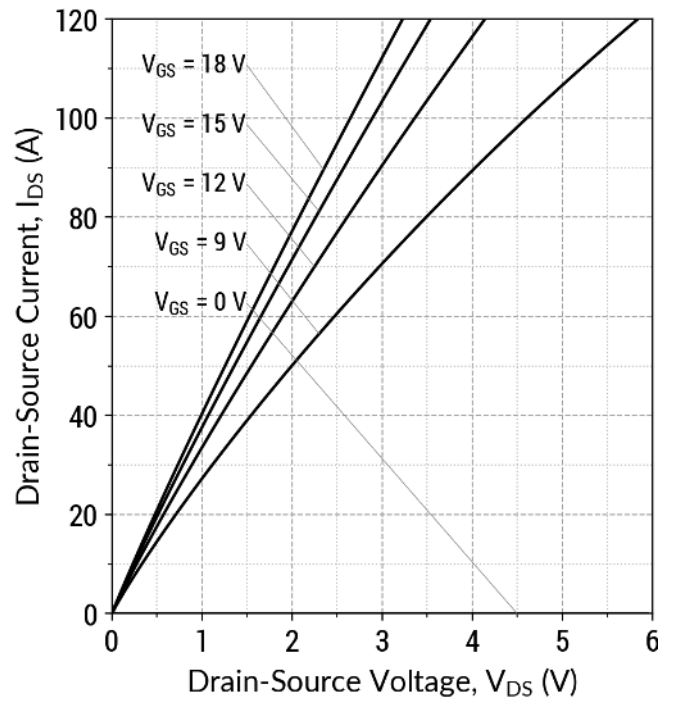
| Parameter | Symbol | Conditions | Values | | | Unit | Note |
|----------------------------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------|--------|------|------|------|------------|
| | | | Min. | Typ. | Max. | | |
| Diode Forward Voltage | V_{SD} | $V_{GS} = -5\text{ V}, I_{SD} = 30\text{ A}$ | | 4.6 | | V | Fig. 17-18 |
| | | $V_{GS} = -5\text{ V}, I_{SD} = 30\text{ A}, T_j = 175^\circ\text{C}$ | | 4.2 | | | |
| Continuous Diode Forward Current | I_S | $V_{GS} = -5\text{ V}, T_c = 100^\circ\text{C}$ | 33 | | | A | |
| Diode Pulse Current | $I_{S(\text{pulse})}$ | $V_{GS} = -5\text{ V}, \text{Note 1}$ | | 132 | | A | |
| Reverse Recovery Time | t_{rr} | | | 35 | | ns | |
| Reverse Recovery Charge | Q_{rr} | $V_{GS} = -5\text{ V}, I_{SD} = 60\text{ A}, V_R = 800\text{ V}$ $dif/dt = 1000\text{ A}/\mu\text{s}, T_j = 25^\circ\text{C}$ | | 240 | | nC | |
| Peak Reverse Recovery Current | I_{rm} | | | 14 | | A | |
| Reverse Recovery Time | t_{rr} | | | 54 | | ns | |
| Reverse Recovery Charge | Q_{rr} | $V_{GS} = -5\text{ V}, I_{SD} = 60\text{ A}, V_R = 800\text{ V}$ $dif/dt = 1000\text{ A}/\mu\text{s}, T_j = 175^\circ\text{C}$ | | 600 | | nC | |
| Peak Reverse Recovery Current | I_{rm} | | | 21 | | A | |

Figure 1: Output Characteristics ($T_j = 25^\circ\text{C}$)



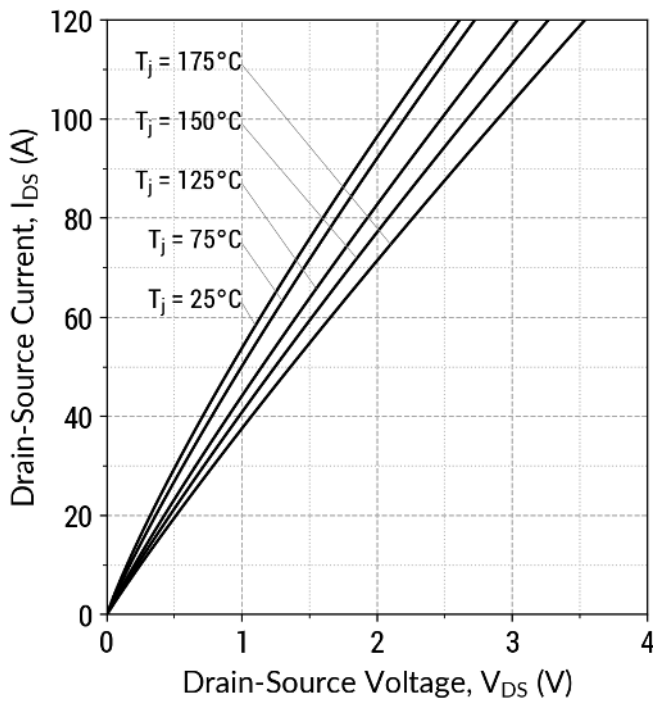
$$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$$

Figure 2: Output Characteristics ($T_j = 175^\circ\text{C}$)



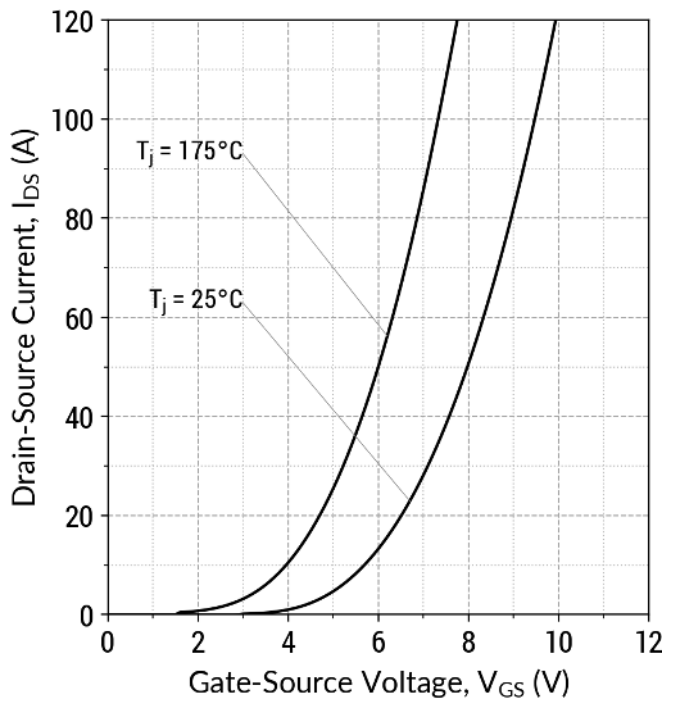
$$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$$

Figure 3: Output Characteristics ($V_{GS} = 15\text{ V}$)



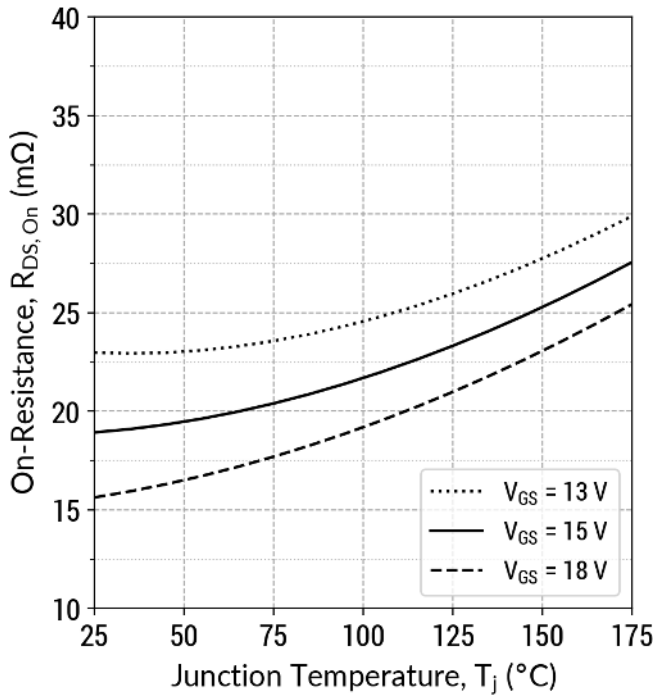
$$I_D = f(V_{DS}, T_j); t_P = 250 \mu\text{s}$$

Figure 4: Transfer Characteristics ($V_{DS} = 10\text{ V}$)



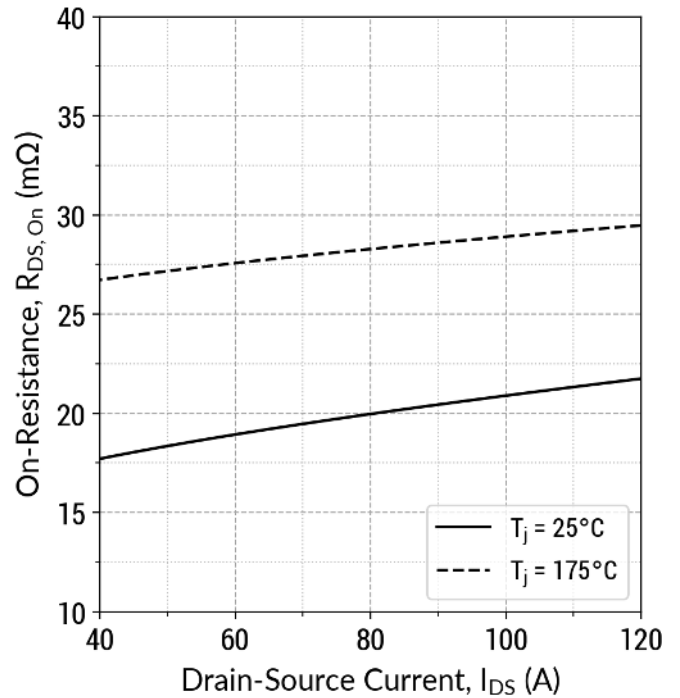
$$I_D = f(V_{GS}, T_j); t_P = 100 \mu\text{s}$$

Figure 5: On-State Resistance v/s Temperature



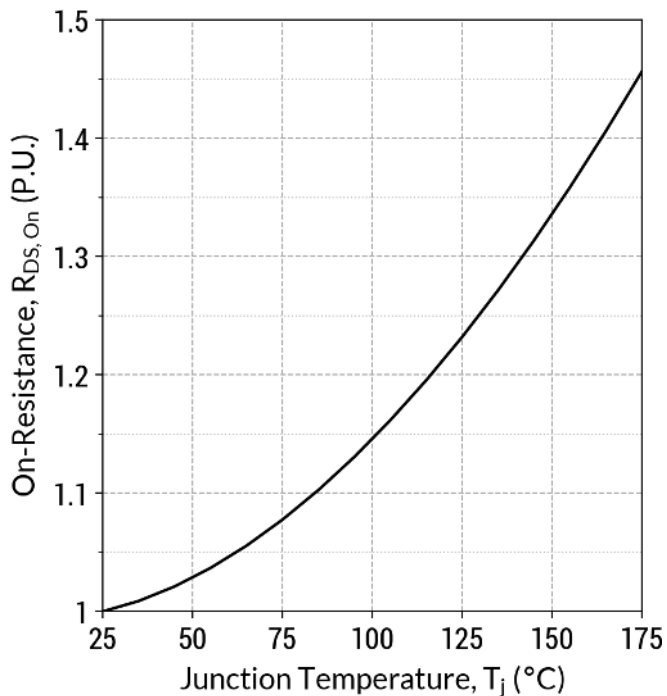
$R_{DS(on)} = f(T_j, V_{GS}); t_p = 250 \mu s; I_D = 60$ A

Figure 6: On-State Resistance v/s Drain Current



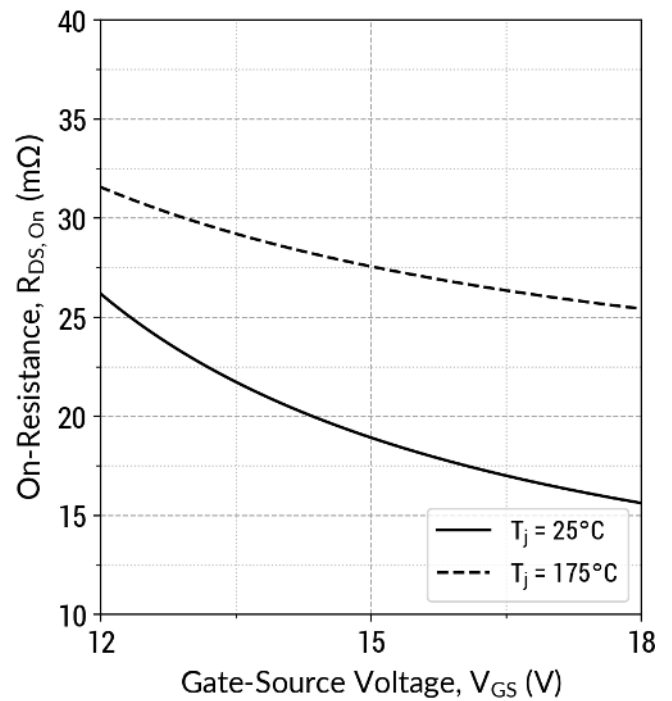
$R_{DS(on)} = f(T_j, I_D); t_p = 250 \mu s; V_{GS} = 15$ V

Figure 7: Normalized On-State Resistance v/s Temperature



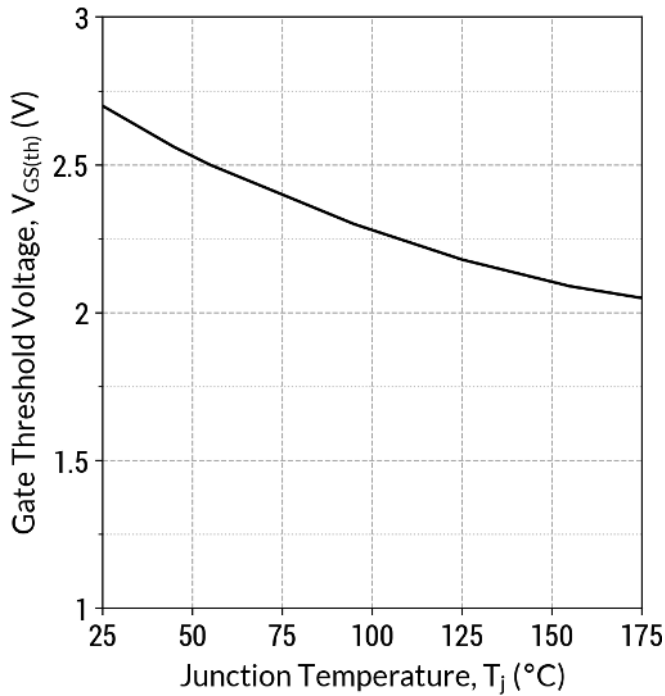
$R_{DS(on)} = f(T_j); t_p = 250 \mu s; I_D = 60$ A; $V_{GS} = 15$ V

Figure 8: On-State Resistance v/s Gate Voltage



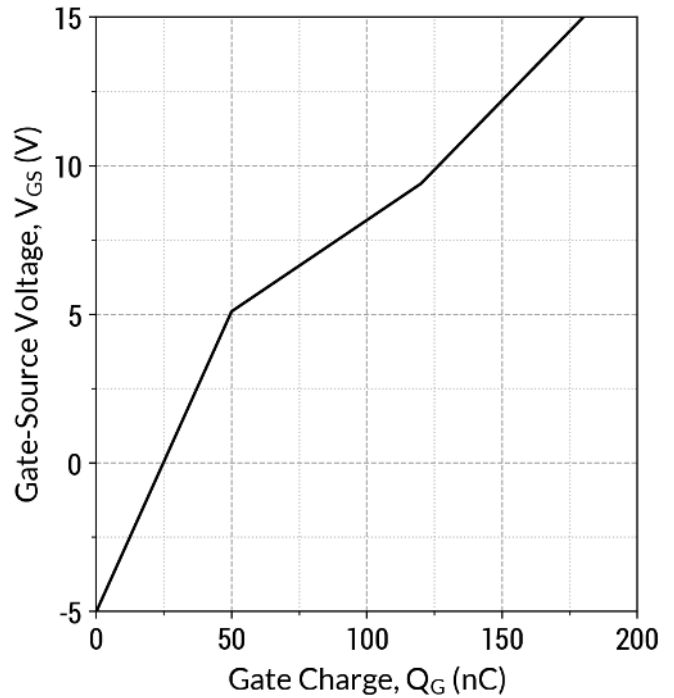
$R_{DS(on)} = f(T_j, V_{GS}); t_p = 250 \mu s; I_D = 60$ A

Figure 9: Threshold Voltage Characteristics



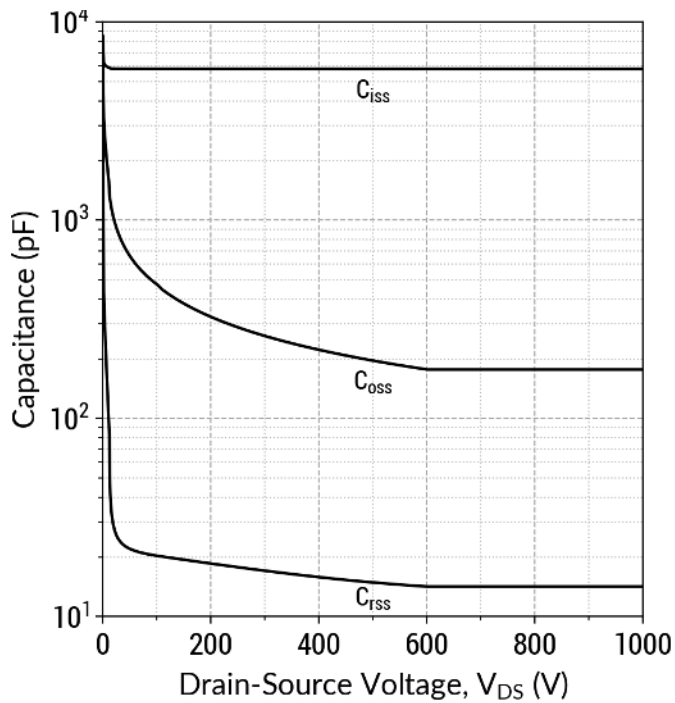
$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 35.0 \text{ mA}$

Figure 10: Gate Charge Characteristics



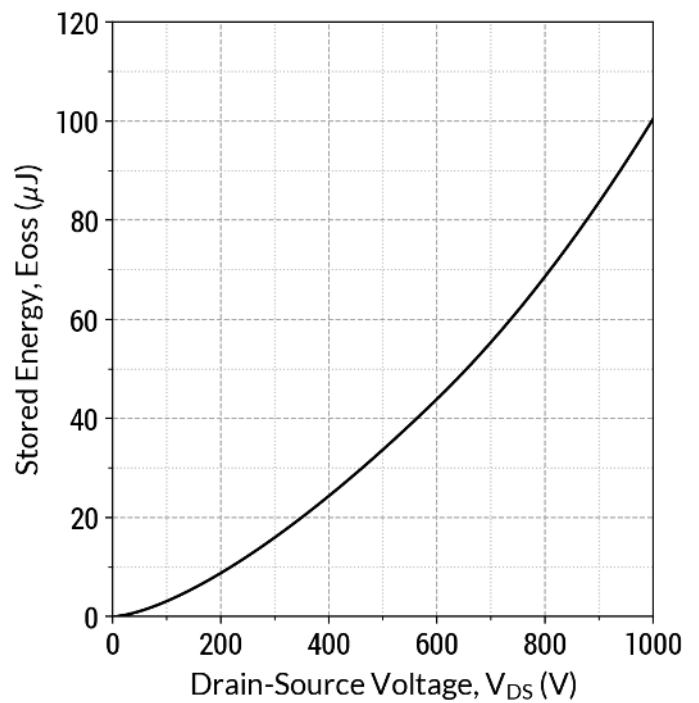
$I_D = 60 \text{ A}; V_{DS} = 800 \text{ V}; T_c = 25^\circ\text{C}$

Figure 11: Capacitance v/s Drain-Source Voltage



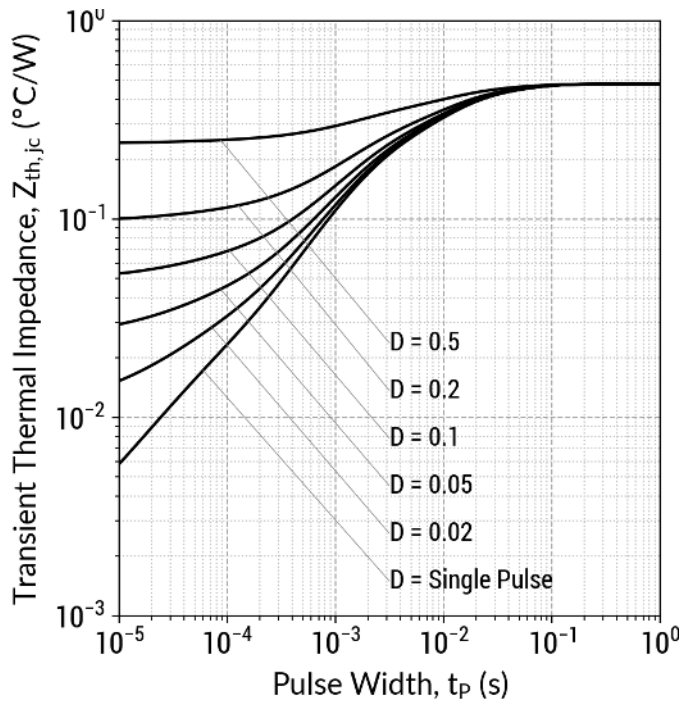
$f = 1 \text{ MHz}; V_{AC} = 25 \text{ mV}$

Figure 12: Output Capacitor Stored Energy



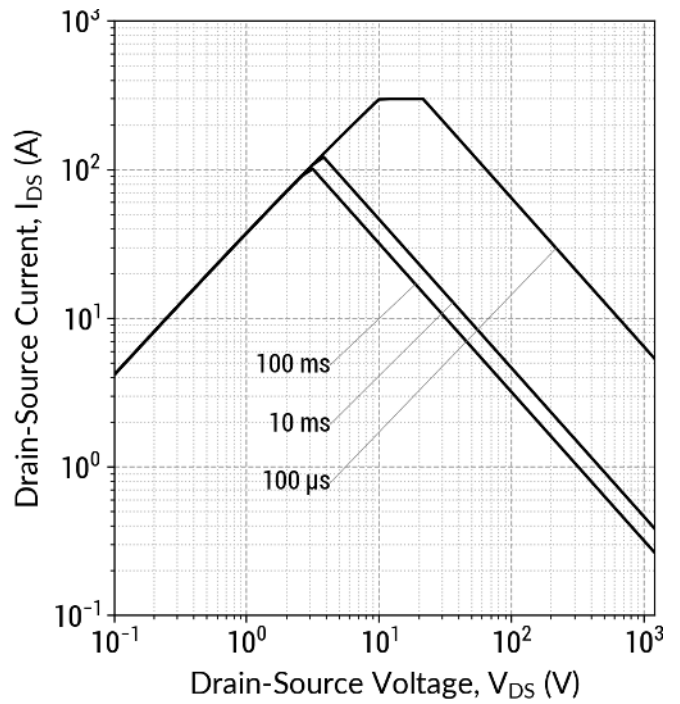
$E_{oss} = f(V_{DS})$

Figure 13: Transient Thermal Impedance



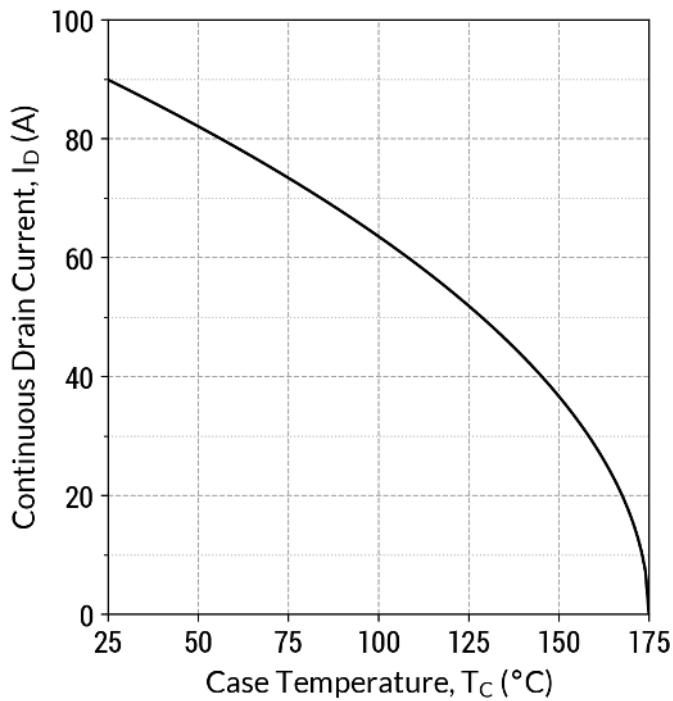
$Z_{th,jc} = f(t_p, D); D = t_p/T$

Figure 14: Safe Operating Area ($T_c = 25^\circ\text{C}$)



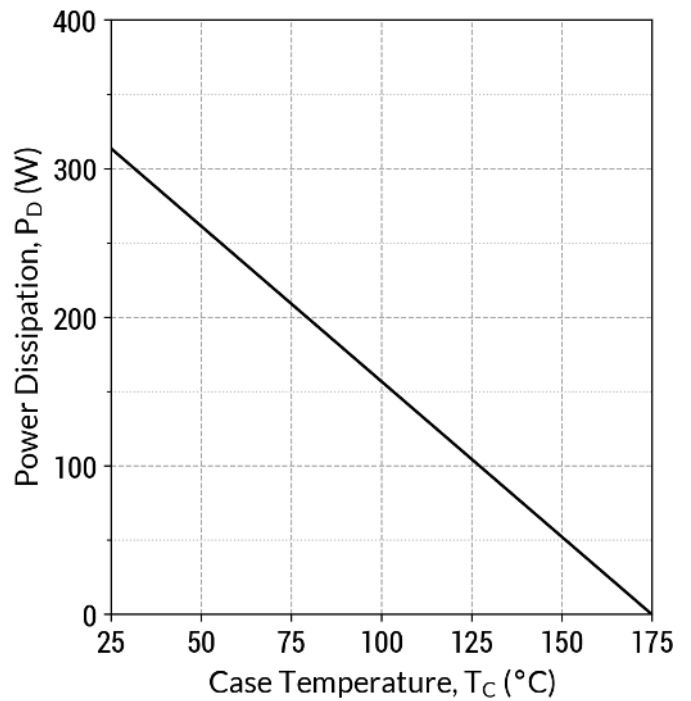
$I_D = f(V_{DS}, t_p); T_j \leq 175^\circ\text{C}; D = 0$

Figure 15: Current De-rating Curve



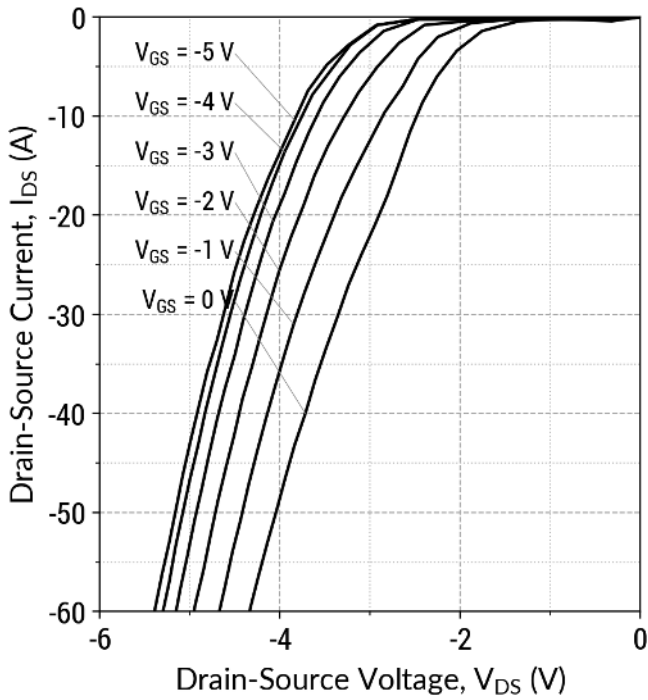
$V_{GS} = 15\text{ V}; I_D = f(T_C); T_j \leq 175^\circ\text{C}$

Figure 16: Power De-rating Curve



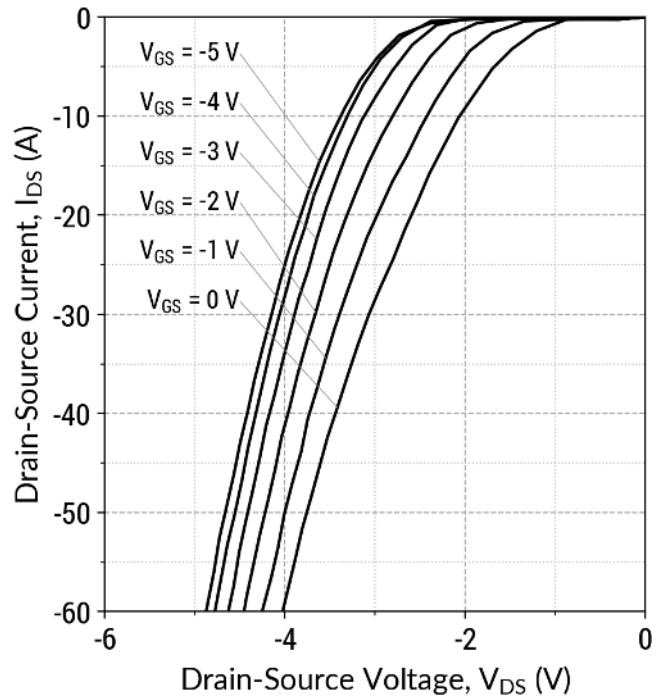
$P_D = f(T_C); T_j \leq 175^\circ\text{C}$

Figure 17: Body Diode Characteristics ($T_j = 25^\circ\text{C}$)



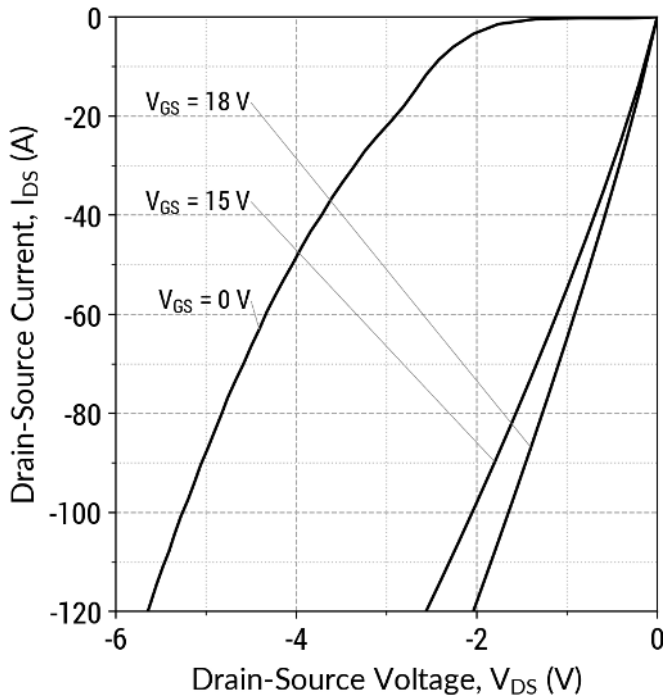
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 18: Body Diode Characteristics ($T_j = 175^\circ\text{C}$)



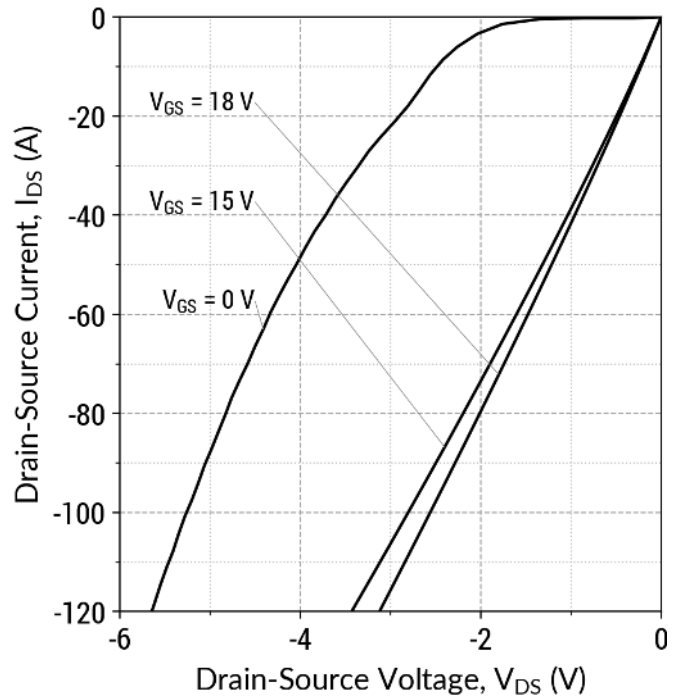
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 19: Third Quadrant Characteristics ($T_j = 25^\circ\text{C}$)



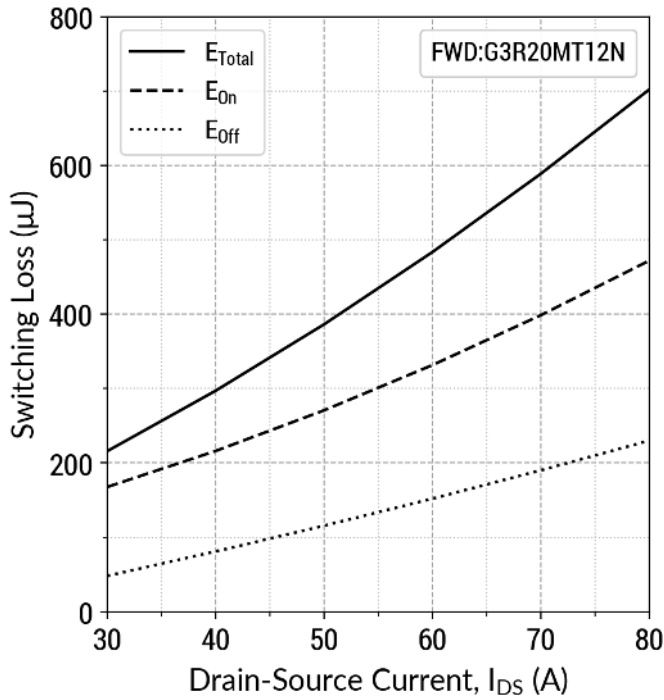
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 20: Third Quadrant Characteristics ($T_j = 175^\circ\text{C}$)



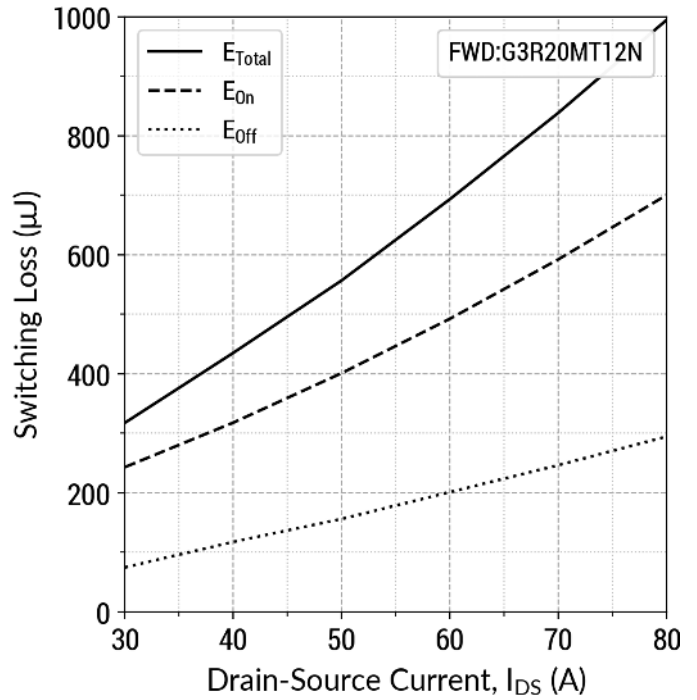
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 21: Inductive Switching Energy v/s Drain Current ($V_{DD} = 600V$)



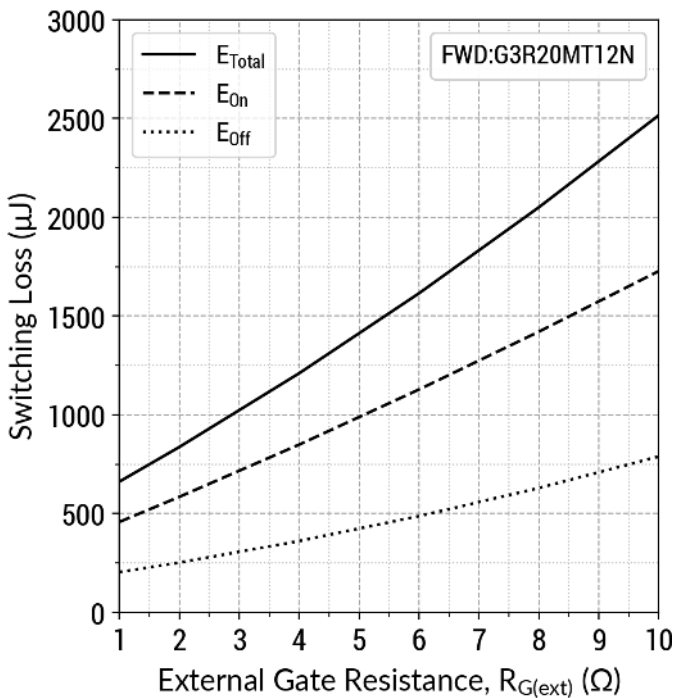
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $R_{G(ext)} = 1 \Omega$; $L = 32.0\mu H$

Figure 22: Inductive Switching Energy v/s Drain Current ($V_{DD} = 800V$)



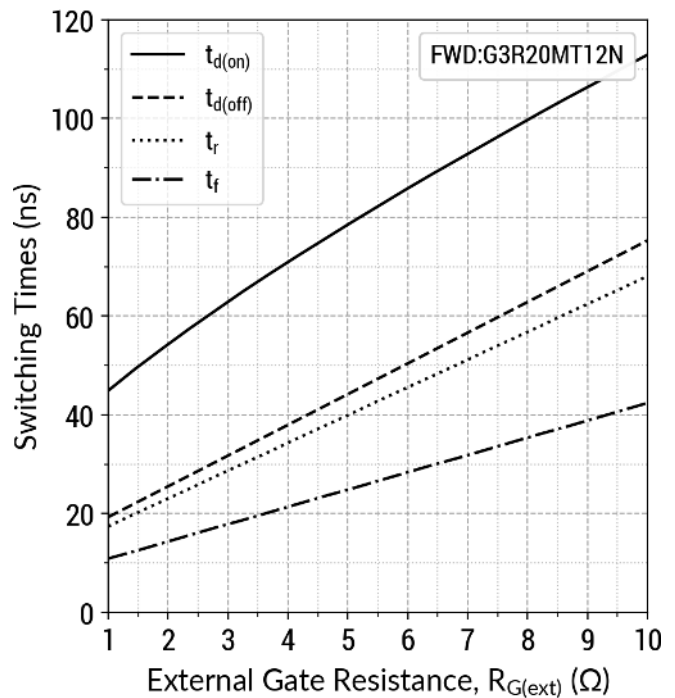
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $R_{G(ext)} = 1 \Omega$; $L = 32.0\mu H$

Figure 23: Inductive Switching Energy v/s $R_{G(ext)}$ ($V_{DD} = 800V$)



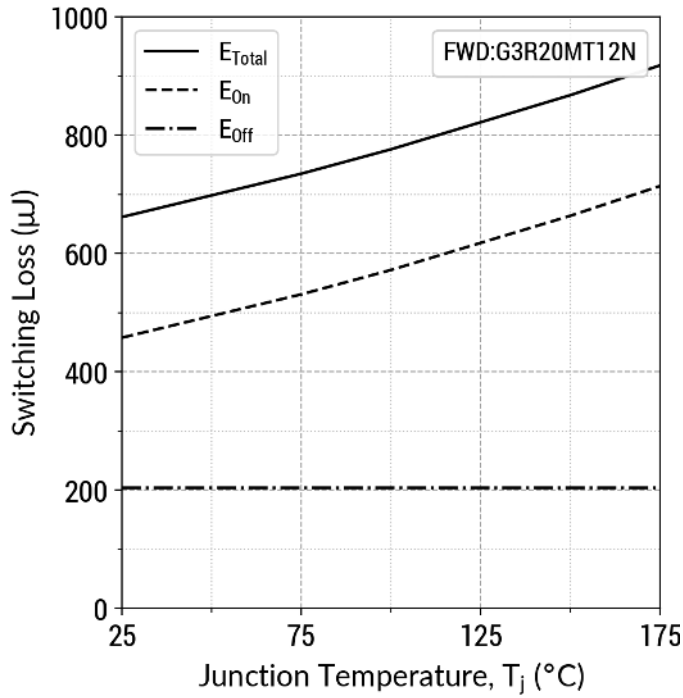
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $I_{DS} = 60 A$; $L = 32.0\mu H$

Figure 24: Switching Time v/s $R_{G(ext)}$ ($V_{DD} = 800V$)



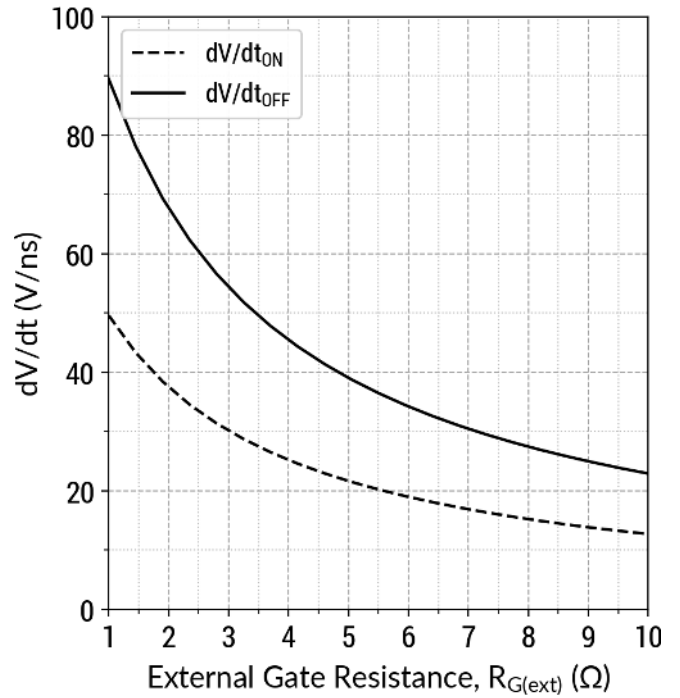
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $I_{DS} = 60 A$; $L = 32.0\mu H$

Figure 25: Inductive Switching Energy v/s Temperature
($V_{DD} = 800V$)



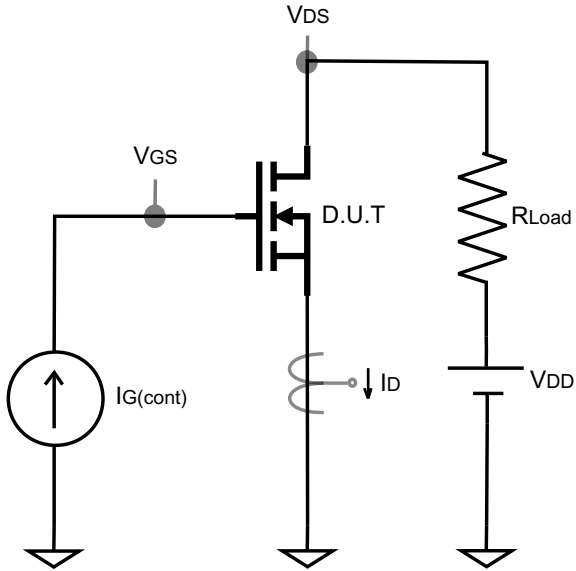
$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $R_{G(ext)} = 1 \Omega$; $I_{DS} = 60 A$; $L = 32.0\mu H$

Figure 26: dV/dt v/s $R_{G(ext)}$
($V_{DD} = 800V$)

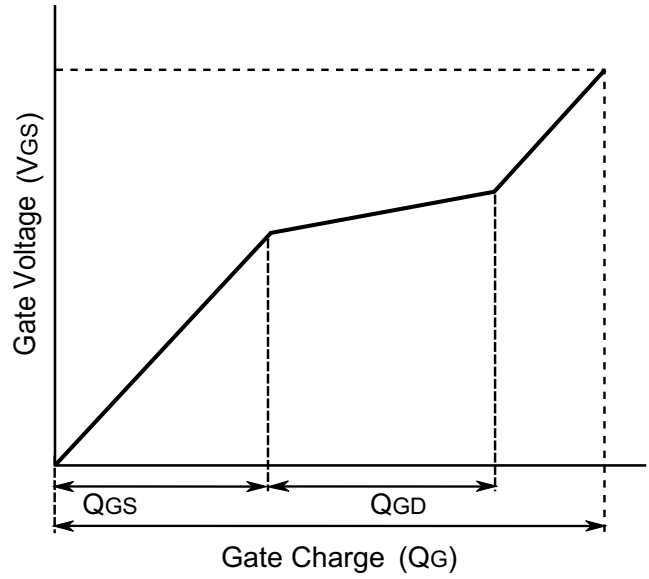


$T_j = 25^\circ C$; $V_{GS} = -5/+15V$; $I_{DS} = 60 A$; $L = 32.0\mu H$

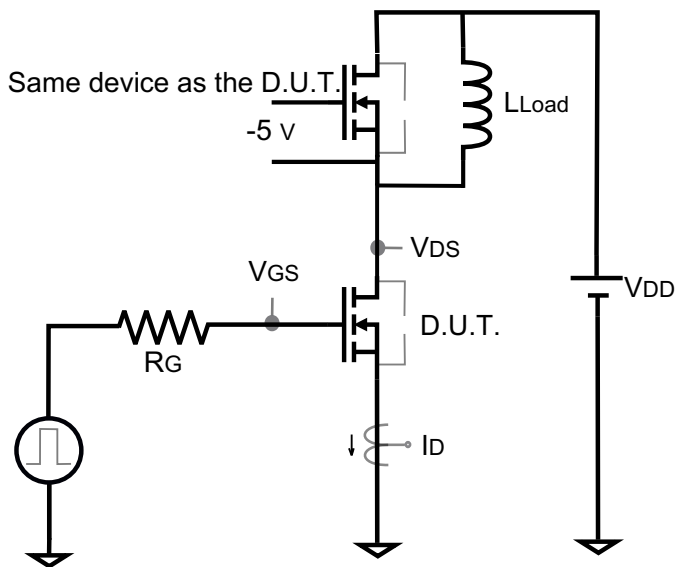
Gate Charge Circuit



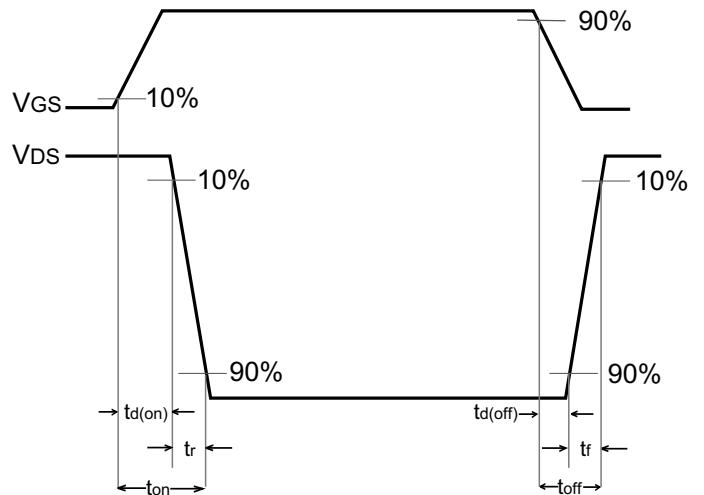
Gate Charge Waveform



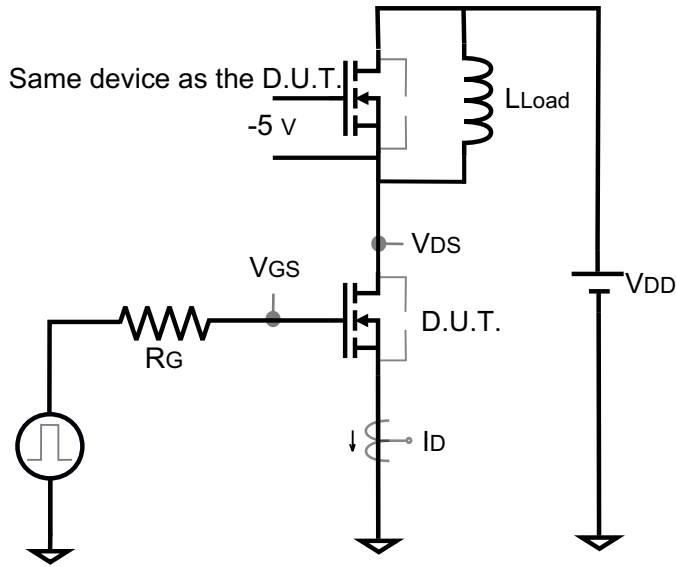
Switching Time Circuit



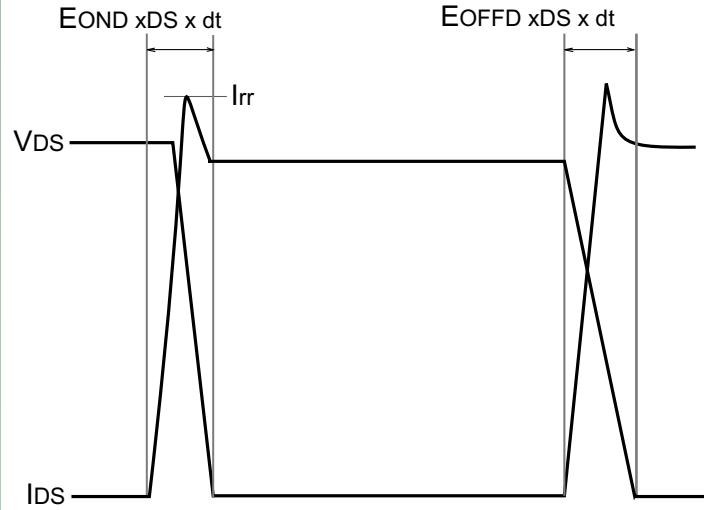
Switching Time Waveform



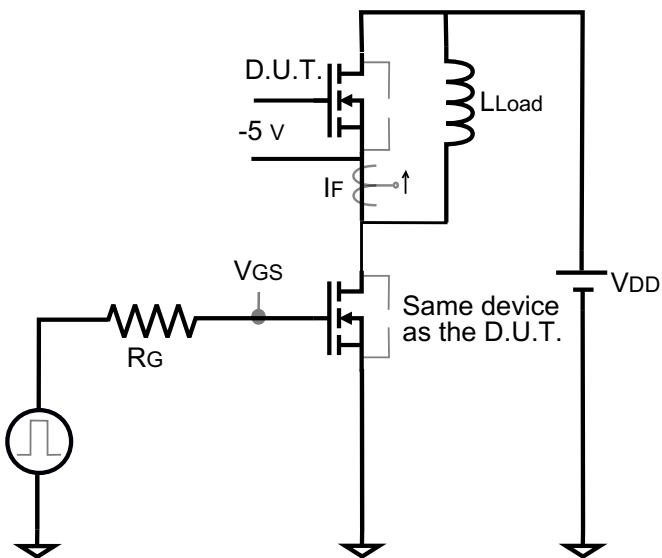
Switching Energy Circuit



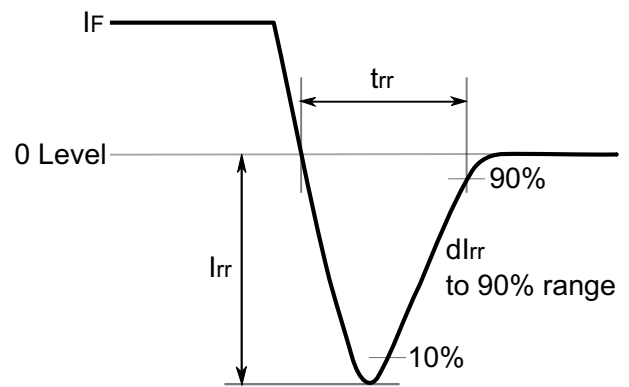
Switching Energy Waveform



Reverse Recovery Circuit

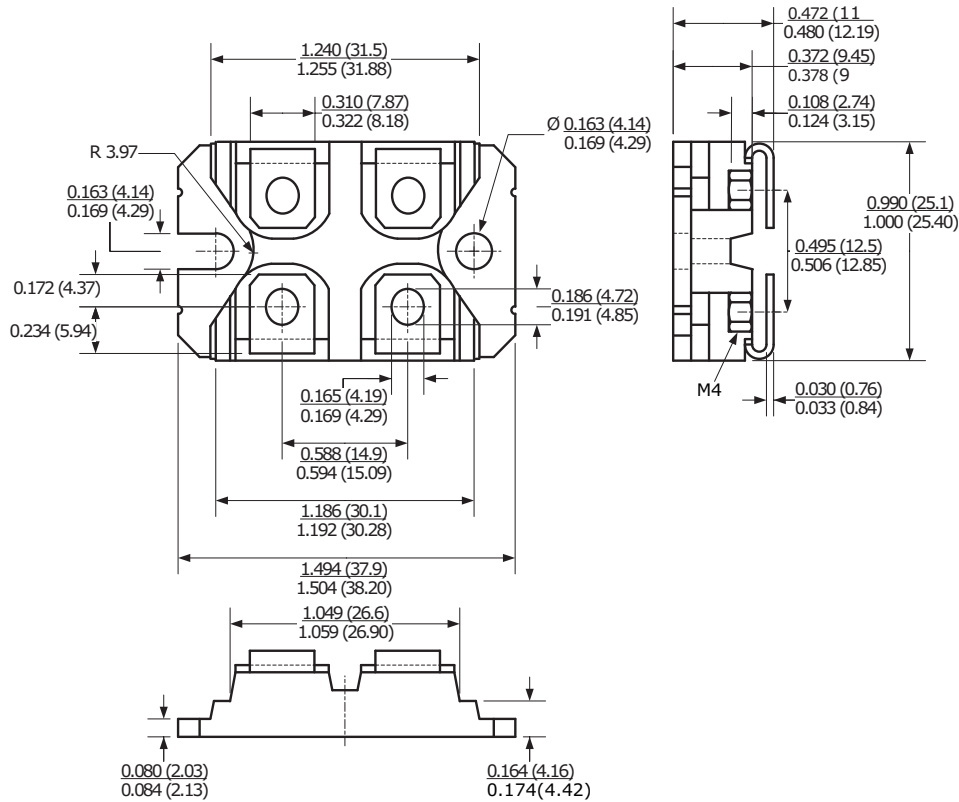


Reverse Recovery Waveform

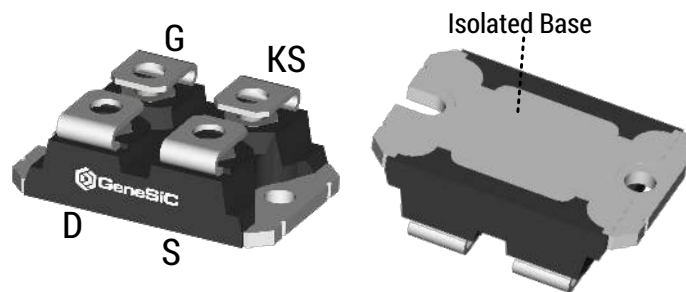


Package Dimensions

SOT-227 Package Outline



Package View



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.
3. THE SOURCE AND KELVIN-SOURCE PINS ARE NOT INTERCHANGABLE. THEIR EXCHANGE MIGHT LEAD TO MALFUNCTION.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

Disclaimer

GeneSiC Semiconductor, Inc. reserves right to make changes to the product specifications and data in this document without notice. GeneSiC disclaims all and any warranty and liability arising out of use or application of any product. No license, express or implied to any intellectual property rights is granted by this document.

Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.

Related Links

- SPICE Models: https://www.genesicsemi.com/sic-mosfet/G3R20MT12N/G3R20MT12N_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-mosfet/G3R20MT12N/G3R20MT12N_PLECS.zip
- CAD Models: https://www.genesicsemi.com/sic-mosfet/G3R20MT12N/G3R20MT12N_3D.zip
- Gate Driver Reference: <https://www.genesicsemi.com/technical-support>
- Evaluation Boards: <https://www.genesicsemi.com/technical-support>
- Reliability: <https://www.genesicsemi.com/reliability>
- Compliance: <https://www.genesicsemi.com/compliance>
- Quality Manual: <https://www.genesicsemi.com/quality>

Revision History

- Rev 23/Feb: Updated with Most Recent Data
- Supersedes: Rev 20/Jun, Rev 20/Aug, Rev 21/Jan, Rev 21/May



www.genesicsemi.com/sic-mosfet/