NJU77580/NJU77582

20MHz, Low noise, Excellent EMI Immunity, Rail-to-rail I/O, Operational Amplifiers

FEATURES

(V^+ = 5V, Typical value)

- Wide Gain Bandwidth 20MHz
- Low Noise 6nV/√Hz (f = 10kHz)
- Enhanced C-Drive ™
  - 1000pF High Capacitive Load Drive
  - Maintains GBW 20MHz under High Capacitive Load
- Input Offset Voltage Drift 0.5μV/°C
- Integrated EMI filter EMIRR = 64dB (f = 1.8GHz)
- Input Tolerant
- High Slew Rate 10V/μs
- Rail-to-Rail Input and Output
- Unity-Gain stable
- Supply Voltage 2.7V to 5.5V
- Input Offset Voltage 2.5mV max.
- Supply Current 2.3mA / ch
- Packages SOT-23-5
  SOP8, MSOP8 (VSP8)
  DFN8-U1 (ESON8-U1)

APPLICATIONS

- Sensor Signal Conditioning
- High-Speed Cable Drivers
- Multi-Pole Active Filters
- Security
- Scanners
- Photodiode Amplifier
- ADC front ends

DESCRIPTION

The NJU77580/NJU77582 are single and dual rail-to-rail input and output single supply OpAmp featuring wide bandwidth and low noise. The combination of very low noise (6nV√Hz at 10kHz), high-gain bandwidth (20MHz), and fast slew rate (10V/μs) make the devices ideal for a wide variety of applications, including signal conditioning and sensor amplification requiring high gains.

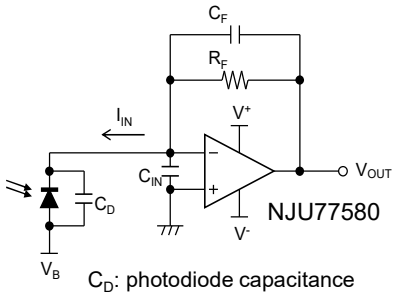
Low input bias current, low noise and low offset voltage drift of 0.5μV/°C performances are also excellent for filters, integrators, photodiode amplifiers, and high impedance sensors. The ability of rail-to-rail input and output enables the designers to buffer ADC, DAC, and other wide output swing devices in single-supply systems.

The Enhanced C-Drive ™ of NJU77580/NJU77582 can directly drive a 1000pF capacitive load, and can output an AC signal with little distortion even with a large capacitive load by suppressing the decrease in GBW. This feature is ideal for high-speed signal cable drivers and high-speed active filter circuits that are sensitive to wiring capacitance.

NJU77580/NJU77582 includes integrated EMI filter to reduce malfunctions caused by R_F noises from mobile phones and other wireless devices. And the input tolerant that allows the input voltage (Recommended: V^-+5.5V) that exceed positive supply voltage is ideal for design for robust industrial applications.

NJU77580/NJU77582 operates from supply range of 2.7V to 5.5V over the -55°C to 125°C extended industrial temperature range. The NJU77580 is available in 5-pin SOT-23-5 package. The NJU77582 is available in 8-pin SOP8, MSOP (VSP): meet JEDEC MO-187-DA type package, and DFN that is thin and 2mm square small package.

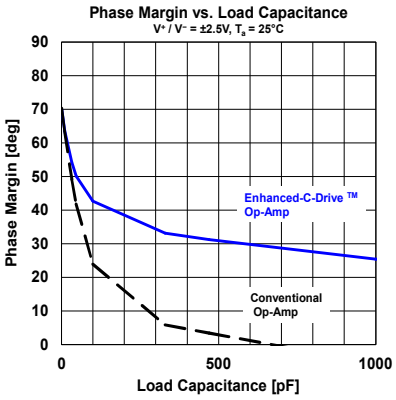
■ TYPICAL APPLICATION



C_D: photodiode capacitance
C_{IN}: OpAmp input capacitance

Transimpedance amplifier

1000pF Capacitive Load Drive



■ PRODUCT NAME INFORMATION

NJU7758X aaa (bbb)

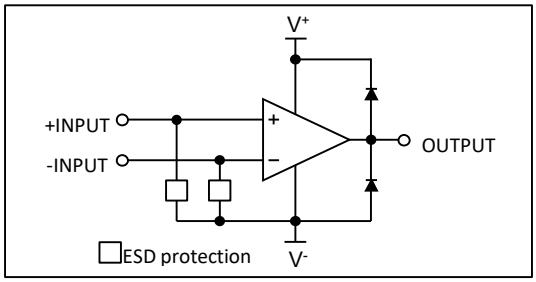
Description of configuration

Suffix	Parameter	Description
aaa	Package code	Indicates the package. Refer to the order information.
bbb	Packing	Refer to the packing specifications.

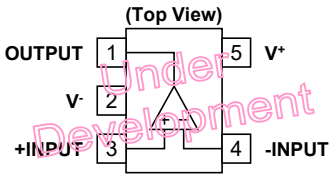
■ ORDER INFORMATION

Product Name	Package	RoHS	Halogen-Free	Terminal Finish	Marking	Weight (mg)	MOQ (pcs)
NJU77580F (TE1)	SOT-23-5	Yes	Yes	Sn2Bi	N/A	15	3000
NJU77582G (TE2)	SOP8	Yes	Yes	Pure Sn	77582	88	2500
NJU77582R (TE1)	MSOP8 (VSP8)	Yes	Yes	Sn2Bi	77582	21	2000
NJU77582KU1 (TE3)	DFN8-U1 (ESON8-U1)	Yes	Yes	Sn2Bi	77582	5.3	3000

■ BLOCK DIAGRAM

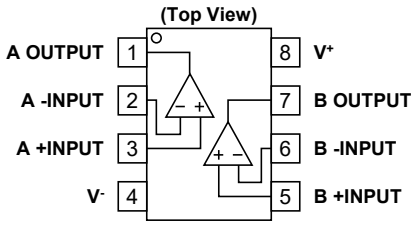


■ PIN DESCRIPTIONS (5 Pin)

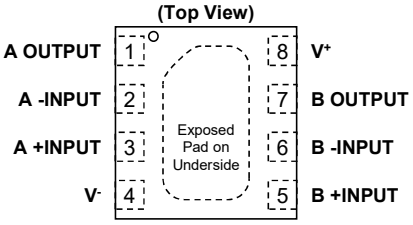


Pin No. SOT-23-5	SYMBOL	I/O	DESCRIPTION
1	A OUTPUT	O	Output channel
3	A -NPUT	I	Inverting input channel
2	A +NPUT	I	Non-inverting input channel
5	V+	-	Positive supply
2	V-	-	Negative supply or Ground (single supply)

■ PIN DESCRIPTIONS (8 Pin)



SOP8, VSP8



ESON8-U1

Pin No. SOP8	Pin No. VSP8	Pin No. ESON8-U1	SYMBOL	I/O	DESCRIPTION
1	1	1	A OUTPUT	O	Output channel A
2	2	2	A -NPUT	I	Inverting input channel A
3	3	3	A +NPUT	I	Non-inverting input channel A
7	7	7	BOUTPUT	O	Output channel B
6	6	6	B -INPUT	I	Inverting input channel B
5	5	5	B +INPUT	I	Non-inverting input channel B
8	8	8	V+	-	Positive supply
4	4	4	V-	-	Negative supply or Ground (single supply)

*Connect to exposed pad to V-

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	$V^+ - V^-$	7	V
Input Voltage *1	V_{IN}	$V^- - 0.3$ to $V^- + 7$	V
Input Current *1	I_{IN}	−10	mA
Output Terminal Input Voltage *2	V_O	$V^- - 0.3$ to $V^+ + 0.3$	V
Differential Input Voltage *3	V_{ID}	±7	V
Output Short-Circuit Duration *4		Continuous	
Storage Temperature	T_{stg}	−65 to 150	°C
Junction Temperature *5	T_j	150	°C

*1 Input voltages outside the supply voltage will be clamped by ESD protection diodes. If the input voltage exceeds the supply voltage, the current must be limited 10mA or less by μsing a restriction resistance. Input current outflow is negative.

*2 The output terminal input voltage is limited at 7V.

*3 Differential voltage is the voltage difference between +INPUT and −INPUT.

*4 Short-circuit can cause excessive heating and destructive dissipation.

*5 Calculate the power consumption of the IC from the operating conditions, and calculate the junction temperature with the thermal resistance.
Please refer to "Thermal characteristics" for the thermal resistance under our measurement board conditions.

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

■ THERMAL CHARACTERISTICS

Package	Measurement Result		Unit
	Thermal Resistance (Θja)	Thermal Characterization Parameter (ψjt)	
SOT-23-5 *1	192	58	°C/W
SOP8 *1	125	43	
MSOP8 (VSP8) *1	189	53	
DFN8-U1 (ESON8-U1) *2	104	25	

qja:Junction-to-Ambient Thermal Resistance
ψjt:Junction-to-Top Thermal Characterization Parameter

*1 Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.

*2 Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4) with exposed pad.
(Applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

■ ELECTROSTATIC DISCHARGE (ESD) PROTECTION VOLTAGE

Parameter	Conditions	Protection Voltage
HBM	C = 100 pF, R = 1.5 kΩ	±1000 V
CDM	Direct CDM	±1000 V

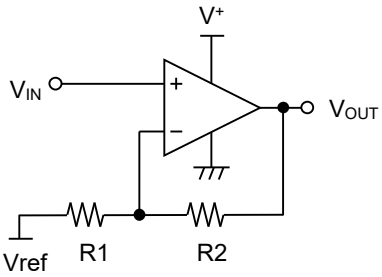
ELECTROSTATIC DISCHARGE RATINGS
The electrostatic discharge test is done based on JEITA ED-4701. In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

■ RECOMMENDED OPERATING CONDITIONS

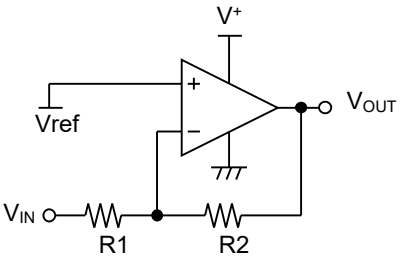
Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	$V^+ - V^-$		2.7 to 5.5	V
Input Voltage	V_{IN}	Closed-loop	$V^- - 0.3$ to $V^- + 5.5$	V
Operating Temperature	T_a		-55 to 125	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

■ TYPICAL APPLICATION CIRCUIT



Non-inverting amplifier



Inverting amplifier

■ ELECTRICAL CHARACTERISTICS

V^+ = 2.7V to 5.5V, V^- = 0V, R_L = 10kΩ to $V^+/2$, T_a = 25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS *1						
Input Offset Voltage	V_{IO}	V_{COM} = V^-	-	0.5	2.5	mV
Input Bias Current	I_B		-	1	-	pA
Input Offset Current	I_{IO}		-	1	-	pA
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	V_{COM} = 0V	-	0.5	-	μV/°C
Input Resistance	R_{IC}		-	70	-	GΩ
Input Capacitance	C_{IN}		-	5	-	pF
Open-Loop Voltage Gain	A_V	V^+ = 5.5V, R_L = 10kΩ, V_O = V^- − 0.3V to V^+ − 0.3V	80	100	-	dB
Common-Mode Rejection Ratio	CMR	V^+ = 5.5V, V_{COM} = V^- − 0.2V to V^+ − 2V	70	90	-	dB
		V^+ = 5.5V, V_{COM} = V^- − 0.2V to V^+ + 0.2V *2	60	80	-	dB
Common-Mode Input Voltage Range	V_{ICM}	Guaranteed by CMR	V^- − 0.2	-	V^+ + 0.2 *2	V
OUTPUT CHARACTERISTICS						
High-level Output Voltage	V_{OH}	V^+ = 5.5V, R_L = 10kΩ to V^+ / 2	-	V^+ − 0.005	V^+ − 0.050	V
		V^+ = 2.7V, R_L = 10kΩ to V^+ / 2	-	V^+ − 0.002	V^+ − 0.050	V
Low-level Output Voltage	V_{OL}	V^+ = 5.5V, R_L = 10kΩ to V^+ / 2	-	7	50	mV
		V^+ = 2.7V, R_L = 10kΩ to V^+ / 2	-	2	50	mV
Capacitive Load Drive	C_L	Φ_M = 45deg	-	50	-	pF
Output Impedance	Z_O	V^+ = 5V, f = 1MHz	-	90	-	Ω
Output Short-Circuit Current	I_{SC}	V^+ = 5V, Source / Sink	-	50 / 50	-	mA
POWER SUPPLY						
Supply Current per Amplifier	I_{SUPPLY}	V^+ = 5V, V_{COM} = 0V, V^+	-	2.3	3.8	mA
		V^+ = 2.7V, V_{COM} = 0V, V^+	-	2.0	3.5	mA
Supply Voltage Rejection Ratio	SVR	V^+ = 2.7 to 5.5V, V_{COM} = 0V, V^+	70	90	-	dB
AC CHARACTERISTICS (V^+ = 5V, V_{COM} = V^+ / 2)						
Slew Rate	SR	C_L = 50pF, V_{IN} = $4V_{PP}$, Gain = 1	-	10	-	V/μs
Gain Bandwidth Product	GBW	C_L = 50pF	-	20	-	MHz
Settling Time 0.1%	t_s	C_L = 50pF, V_{IN} = $4V_{PP}$, Gain = 1	-	0.7	-	μs
Phase Margin	Φ_M	C_L = 10pF	-	60	-	Deg
		C_L = 50pF	-	45	-	Deg
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, V_O = 1.5Vrms	-	0.005	-	%
Equivalent Input Noise Voltage	V_{NI}	f = 0.1Hz to 10Hz	-	1.4	-	μV_{PP}
	e_n	f = 1kHz	-	7	-	nV/√Hz
		f = 10kHz	-	6	-	nV/√Hz
Channel Separation	CS	NJU77582, f = 1kHz	-	120	-	dB

*1 Input offset voltage and drift, Input bias and offset current are positive or negative, its absolute values are listed in electrical characteristics.

*2 V^+ + 0.2V value is limited at 5.5V.

■ APPLICATION NOTE

Single and Dual Supply Voltage Operation

The NJU7758x series works with both single supply and dual supply when the voltage supplied is between V^+ and V^-. These amplifiers operate from single 2.7V to 5.5V supply and dual ±1.35V to ±2.75V supply. The power supply pin should have bypass capacitor (i.e. 0.1µF).

No Phase Reversal

The NJU7758x series are designed to prevent phase reversal at the input voltage above the supply voltage. Figure1 shows no phase reversal characteristics with the input voltage exceeding the supply voltage.

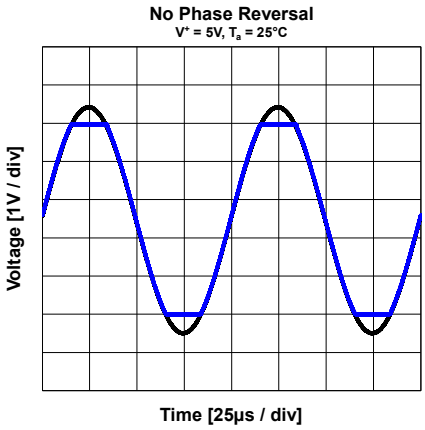


Figure1. No phase reversal

Power-on Time

The NJU7758x series typically require a power-on time of 10µs (Figure2). Power-on time depends on the supply voltage, bypass capacitor, impedance of supply source and impedance other devices. While settling time, IC is unstable, such as output voltage.

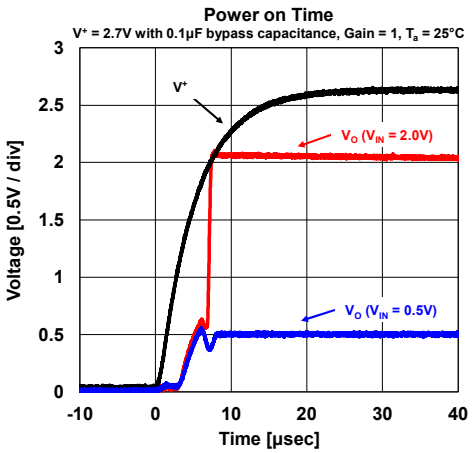


Figure2. Power on time

Rail-to-Rail Input

The input stage of NJU7758x series has two input differential pairs, PMOS and NMOS (Figure3). When the common- mode input voltage is from 200mV below the negative supply voltage to the typically (V^+) − 1.3V, the PMOS pair is active. When the common-mode input voltage close to the positive supply, typically (V^+) − 1.3V to 200mV above positive supply, the NMOS pair is active. In the transition region, the performance of offset voltage, as shown in figure4, offset voltage drift, CMR, SVR and THD is slightly degraded.

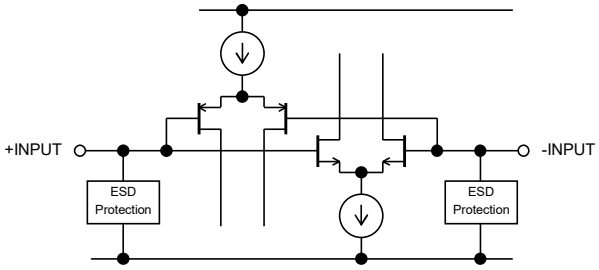


Figure3. Simplified Schematic of Input Stage

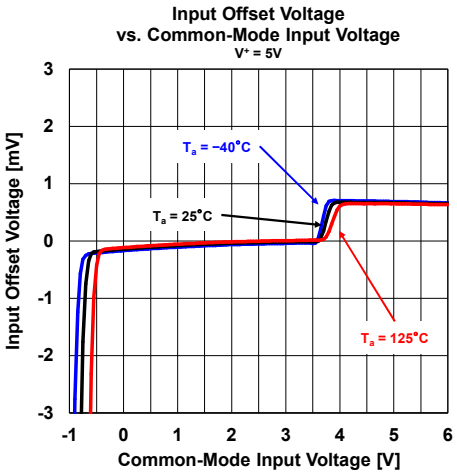


Figure4. Offset Voltage change with common-mode input voltage.

For the best performance design is inverting amplifier shown in Figure5. Inverting amplifier has a constant common-mode voltage equal to Vref. If Vref voltage is constant and is chosen to avoid transition region, output will be best linearity performance.

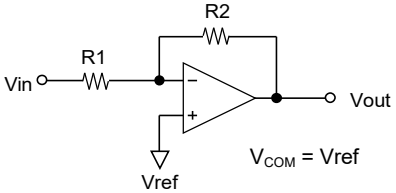


Figure5. Inverting Amplifier

■ APPLICATION NOTE

Input Tolerant

In general, common Op-Amp is protected by internal ESD diode that is connected from input pin to both the positive and negative power supply. In a buffer configuration, when input exceeds either supply voltage, ESD diode will be forward biased and current. If the current is high enough, even when input current over long periods of time or even short periods of time, can shift the electrical characteristics beyond the data sheet's guaranteed limits, or cause a permanent failure of the op amp.
The input of the NJU7758x series has an ESD protection as shown in Figure 3. The input bias current is minimized in the input voltage even in operating voltage range and exceeding the V^+ supply, and the Op-Amp is protected from overvoltage current (Figure6). The maximum input voltage is absolute maximum rating of V^- + 7V, but usually recommend design so that the input voltage is up to V^- + 5.5V.

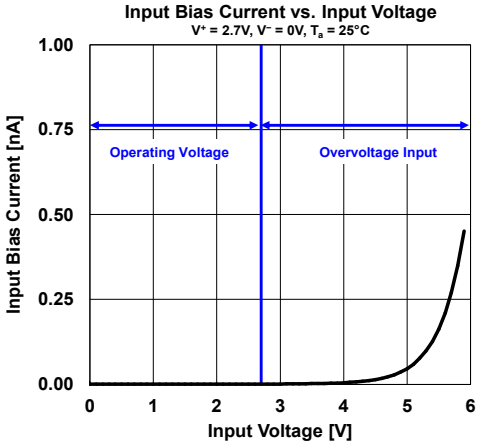
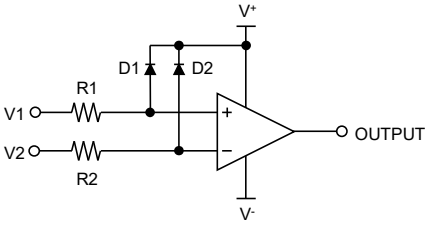


Figure6. Input bias current vs. input voltage

NJU7758x series protects the input pin from overvoltage by shunting the overvoltage current to the V^- supply rail. When the input voltage for V^- − 0.3V to V^- + 7V, the ESD protection is not activate and minimize the input bias current (Figure6).
For the input voltage 300mV below the negative supply voltage, the ESD protection operates to protect the input terminal. At this moment, the current flowing in protection element is allowed up to 10 mA.
Momentary voltages above V^- + 7V, the ESD protection also activate, and clamp inputs, but cannot protect against overvoltage excepting ESD.

In some applications, it may be necessary to prevent excessive overvoltage. Figure6 is example to protect input transistors. The external resistors R1, R2 limit the current through external diodes D1, D2.



$$(R1, R2) > \frac{V^-\text{-}(V1, V2)}{10mA}$$

$$(R1, R2) > \frac{(V1,\ V2)\text{-}V^+}{I_F}$$

I_F:Forward current of external diode.

Figure7. Example of input protection

Power Supply Protection for Overvoltage Condition

In general, many power supplies cannot sink current. If nothing within the circuit can sink the overvoltage current, if the overvoltage occurs with the supplies powered on, in the ESD diode protection Op-Amp, the supply voltage can exceed the intended operating voltage of the system.
Figure8 compares the output voltage of a conventional Op-Amp and NJU7758x series, when a signal is applied to the input terminal when the power supply voltage is OFF. In conventional Op-Amp, the output voltage is generated according to the input voltage. This output voltage will input an unexpected signal to the device connected to the subsequent stage of Op-Amp, which may cause malfunction or damage. Since NJU7758x series prevents the positive overvoltage current flowing through to power supply terminal and rising power supply voltage and keep the output voltage at 0V.

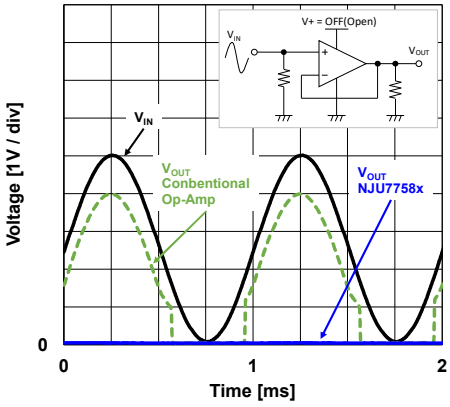


Figure8. Example of input protection

■ APPLICATION NOTE

Power Supply Protection for Overvoltage Condition (Continues)

The input tolerant function of the NJU7758x series prevents unexpected signal input to subsequent devices such as AD converters, or prevents applied voltage that can damage subsequent devices (Figure9a, Figure9b).

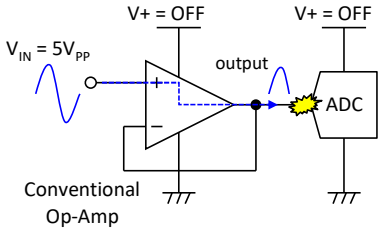


Figure9a. Conventional Op-Amp

Output voltage is generated when voltage is applied to the input terminal when the power is OFF.
In some cases, subsequent devices will be damaged.

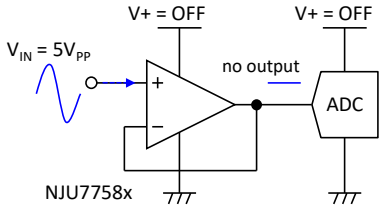


Figure9b. NJU7758x Series

The output voltage is 0V when the voltage is applied to the input terminal when the power is OFF.
Input tolerant function protects subsequent devices.

Enhanced C-Drive ™

A typical high-speed Op-Amp causes a phase lag and a decrease in gain bandwidth product (GBW) when the capacitive load increases due to pattern wiring or cable routing. The phase lag causes ringing and overshoot in the step response, and the decrease in GBW results in a decrease in the amplification factor at AC output signals.
The NJU7758x series uses *Enhanced C-Drive* ™ technology to minimize performance degradation under such capacitive loads.
Figure 10 shows a comparison of the phase margins of a typical Op-Amp and an *Enhanced C-Drive* ™ Op-Amp due to a capacitive load. A typical Op-Amp has a phase margin of less than 30 degree with a capacitive load of 100pF, whereas an *Enhanced C-Drive* ™ Op-Amp has a similar phase margin at 1000pF.

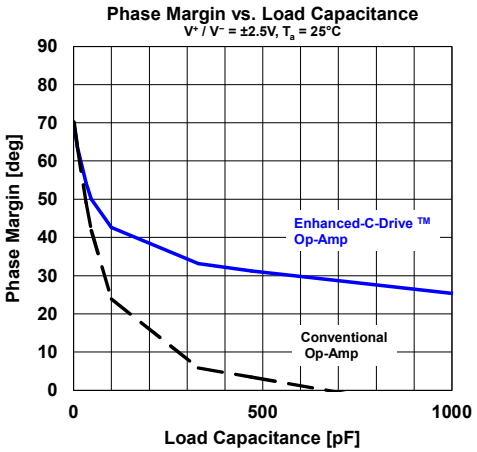


Figure10. Suppresses the decrease in phase margin due to capacitive load

Some conventional Op-Amps have a reduced GBW as increasing capacitive load, causes a decrease in amplitude and distortion of the AC output signals. As shown in Figure11, the *Enhanced C-Drive* ™ Op-Amp can output an AC signal with little distortion even with a large capacitive load by suppressing the decrease in GBW.
The NJU7758x series eliminates the necessary to consider pattern wiring and cable capacity when designing sets that requires high-speed response, making it possible to reduce the mounting area and design period.

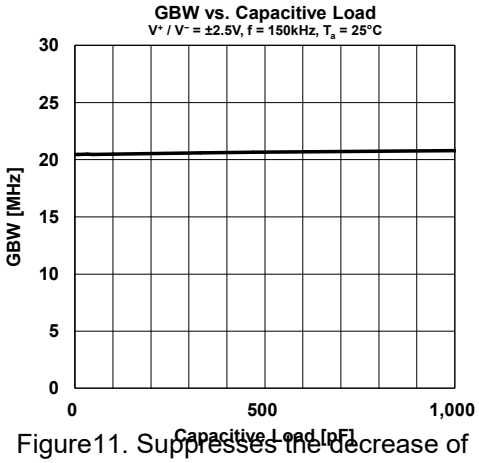


Figure11. Suppresses the decrease of GBW due to capacitive load

■ APPLICATION NOTE

Capacitive Load

The NJU7758x series can use at unity gain follower. The unity gain follower is the most sensitive configuration to capacitive load, but Enhanced C-Drive ™ technology minimizes performance degradation under capacitive loads.
The NJU7758x series is unity gain stable for capacitive loads of 1000pF. To drive heavier capacitive loads, an isolation resistor, R_{ISO} as shown Figure12, should be used. R_{ISO} improves the feedback loop's phase margin by making the output load resistive at higher frequencies. The larger the value of R_{ISO}, the more stable the output voltage will be. However, larger values of R_{ISO} result in reduced output swing, reduced output current drive and reduced frequency bandwidth (Figure13).

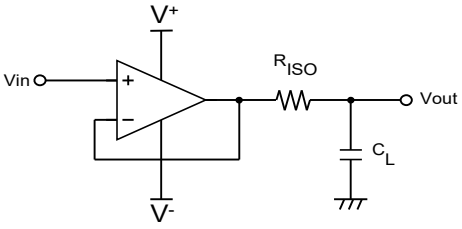


Figure12. Isolating capacitive load

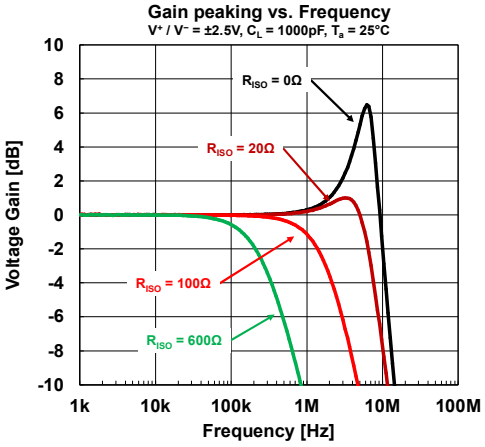
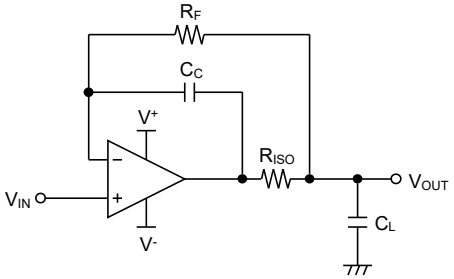


Figure13.Gain peaking with R_{ISO}

Figure14 shows the isolation circuit with R_{ISO}, R_F and C_C. Minimize the effect of voltage drop due to R_{ISO} and output current.



$$10R_{ISO}C_L < R_FC_C$$
R_{ISO} is more than 100Ω

Figure14. Isolating capacitive load with R_{ISO}, R_F and C_C

Low noise voltage and input offset voltage drift

The NJU7758x series features very low noise performance (Figure15). The equivalent input noise voltage at 10kHz is 6nV / √Hz, and the Peak-to-Peak noise of 0.1Hz to 20MHz is only 260μV_{PP}.
In addition, the change in input offset voltage due to temperature change becomes ultra-low frequency noise of 0.1Hz or less, and appears as fluctuation of output voltage. The temperature change of the input offset voltage of the NJU7758x is 0.5uV/°C (typ.) (Figure16), which means an ultra-low frequency noise of 90uV at a temperature change of -55 °C to 125 °C. The sum of these two noise voltages is 350uV for the NJU7758x series, which is equivalent to 1 / 2 LSB of a 12bit ADC. The NJU7758x series is also compatible with high-precision, high-speed AD converters.

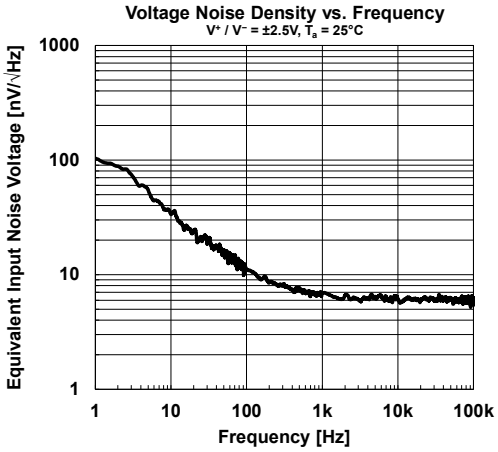


Figure15. Equivalent input noise voltage

■ APPLICATION NOTE

Low noise voltage and offset voltage drift (Continues)

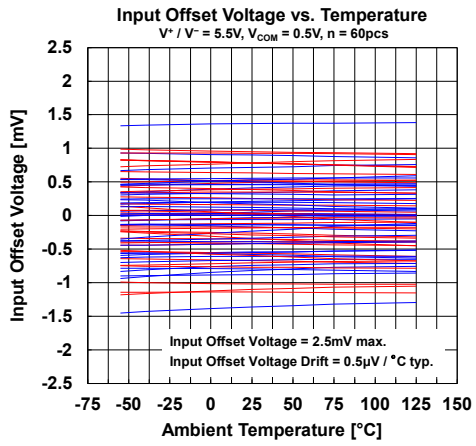


Figure16. Input offset voltage drift vs. temperature

Terminating unused Op-Amps

Figure 17 shows examples of common method of terminating uncommitted operational amplifiers with using dual or quad. Improper termination can be result increase supply current, heating and noise in Op-Amps.

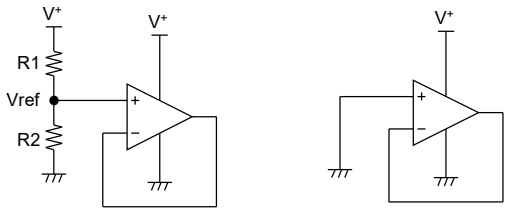
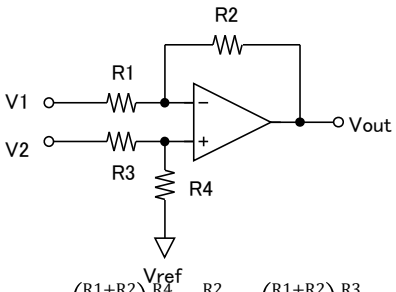


Figure17. Terminating unused Op-Amps

Differential Amplifier

Figure18 shows a one Op-Amp differential amplifier that consists of the single Op-Amp and four external resistors. Differential amplifier amplifies the difference between its two input pins, and rejects the common-mode input voltage at both input pins. This is used in variety of applications including current sensing, differential to single-end converter, isolation amplifier to remove common-mode noise.



$$Vout=\left(\frac{R1+R2}{R3+R4}\right)\frac{R4}{R1}V2-\frac{R2}{R1}V1+\left(\frac{R1+R2}{R3+R4}\right)\frac{R3}{R1}Vref$$

R1=R3, R2=R4

$$Vout=\frac{R2}{R1}(V2-V1)+Vref$$

Figure18. Differential Amplifier

The differential amplifier's common-mode rejection ratio (CMR) is primarily determined by resistor mismatches, not by the Op-Amp's CMR. Ideally, the resistors are chosen such that R2/R1 = R4/R3. The CMR due to the resistors in differential amplifier can be calculated using the below formula:

$$CMR_{R\_error} \approx 20\log\left(\frac{1+\frac{R2}{R1}}{4R_{error}}\right)$$

CMR_{R_error} = CMR due only to the resistors

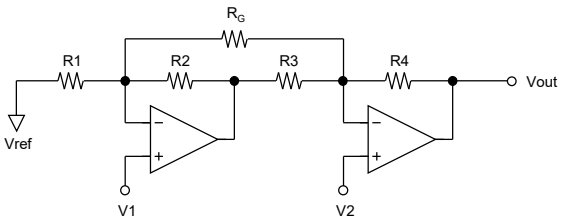
R_{error} = Resistor's tolerance

Example:
R2 / R1 = 1 and R_{error} = 0.1%, then CMR = 54dB
R2 / R1 = 1 and R_{error} = 1%, then CMR = 34dB
If using resistors with 1% tolerance and gain = 1, the CMR will only be 34dB.

■ APPLICATION NOTE

Instrumentation Amplifier

The instrumentation amplifier is suitable for requiring high input impedance and high common mode noise rejection at high gains. Figure19 and Figure20 is instrumentation amplifier using two or three Op-Amp. Supply the reference voltage (Vref) with a low impedance source to keep accuracy.

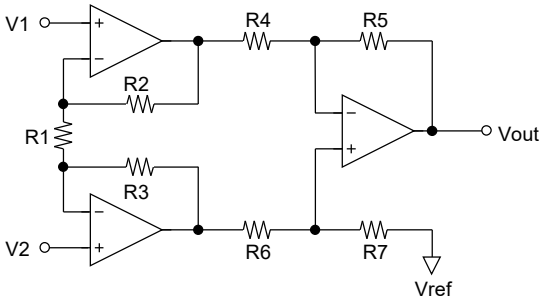


$$\text{Vout}=\left(1+\frac{R4}{R3}+\frac{2R4}{R_G}\right)(V2-V1)+Vref$$

R1=R4, R2=R3

$$CMR_{R\_error} \approx 20\log\left(\frac{1+\frac{R4}{R3}+\frac{2R4}{R_G}}{4R_{error}}\right)$$

Figure19. Instrumentation Amplifier with two Op-Amp



$$\text{Vout}=\left(1+\frac{2R2}{R1}\right)\left(\frac{R5}{R4}\right)(V_2-V_1)+Vref$$

R2=R3, R4=R6, R5=R7

$$CMR_{R\_error} \approx 20\log\left(\frac{R1+2R2}{R1}\times\frac{1+\frac{R5}{R4}}{4R_{error}}\right)$$

Figure20. Instrumentation Amplifier with three Op-Amp

Current Sensing

Current sensing applications are one such application in a wide range of electronic applications and mostly used for feedback control systems, including power metering battery life indicators and chargers, over- current protection and supervising circuit, automotive, and medical equipment. In such applications, it is desirable to use a shunt with very low resistance to minimize the series voltage drop and minimizes wasted power, and allows the measurement of high current. The NJU7758x series is ideal for these current sensing applications. Figure21 shows a high-side current sensing circuit, and Figure22 shows a low-side current sensing circuit. The NJU7758x series has rail-to-rail input and output characteristics, thus allows the both of high-side and low-side current sensing circuit.
The differential amplifier's common-mode rejection ratio (CMR) is primarily determined by resistor mismatches. For details, refer to differential amplifiers in the application note.

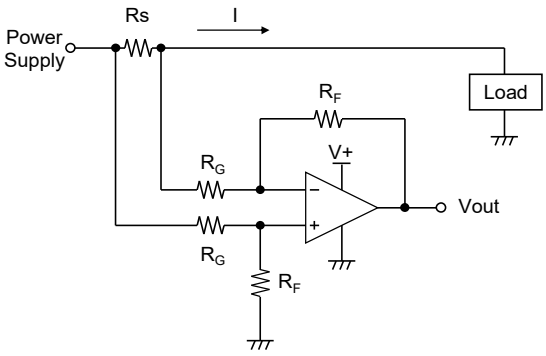


Figure21. High-Side Current Sensing

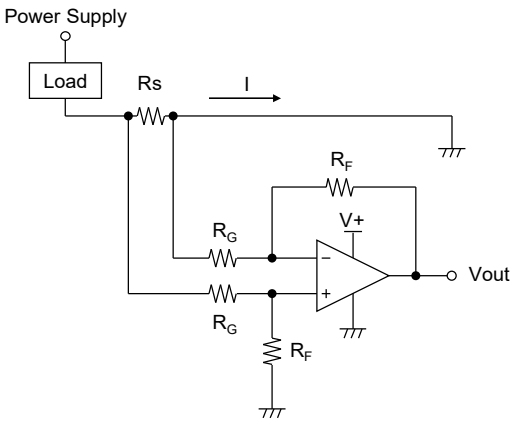
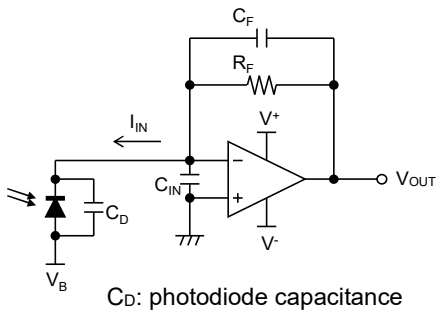


Figure22. Low-Side Current Sensing

■ APPLICATION NOTE

Transimpedance Amplifier

The features high input impedance with CMOS input and low power can be used for transimpedance amplifier applications shown in Figure23. The output voltage of amplifier is given by the equation $V_{OUT} = I_{IN} \cdot R_F$. Since the output voltage swing of amplifier is limited, R_F should be selected such that all possible values of I_{IN} can be detected.



C_D: photodiode capacitance
C_{IN}: Op-Amp input capacitance

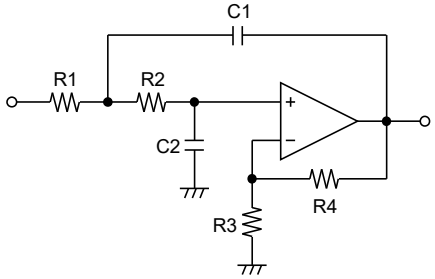
Figure23. Transimpedance amplifier

The C_D, C_{IN} and R_F generate a phase lag which causes gain-peaking and can destabilized circuit. The essential component for obtaining a maximally flat response is a feedback capacitor C_F. C_F is usually added in parallel with R_F to maintain circuit stability and to control the frequency response. To maximally flat, 2nd order response, R_F and C_F should be chosen by using below equation.

$$C_F = \sqrt{\frac{C_{IN}+C_D}{GBW \times 2\pi \times R_F}}$$

Sallen-Key 2nd-Order Active Low-Pass Filter

The Sallen-Key 2nd-order active low-pass filter is shown in Figure24. It can be used for a multiple pole filter required high attenuation.



$R = R1 = R2$, $C = C1 = C2$
Q: Quality factor , G_{DC}: DC Gain

$$f_{-3dB} = \frac{1}{2\pi RC} \text{ , } Q = \frac{1}{3-G_{DC}} \text{ , } G_{DC} = 1 + \frac{R4}{R3} = 3 - \frac{1}{Q}$$

Figure24. Sallen-Key 2nd-Order Low-Pass Filter

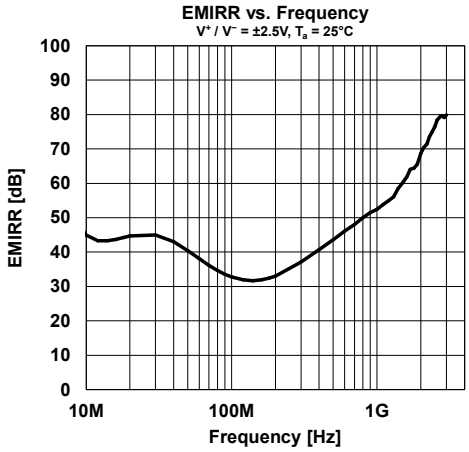
EMIRR (EMI Rejection Ratio) Definition

EMIRR is a parameter indicating the EMI robustness of an Op-Amp. The definition of EMIRR is given by the following equation1.

$$EMIRR = 20 \cdot \log\left(\frac{V_{RF\_PEAK}}{|\Delta V_{IO}|}\right) \qquad \text{--- eq.1}$$

V_{RF_PEAK}: RF Signal Amplitude [V_P]
ΔV_{IO}: Input offset voltage shift quantity [V]

The tolerance of the RF signal can be grasped by measuring an RF signal and offset voltage shift quantity. Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

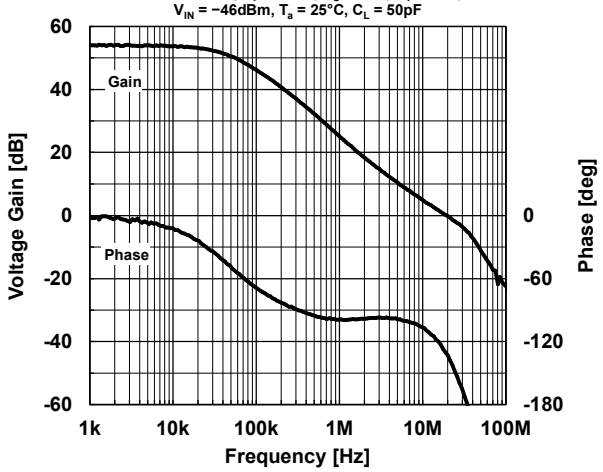


*For details, refer to “Application Note for EMI Immunity" in our HP: http://www.njr.com/

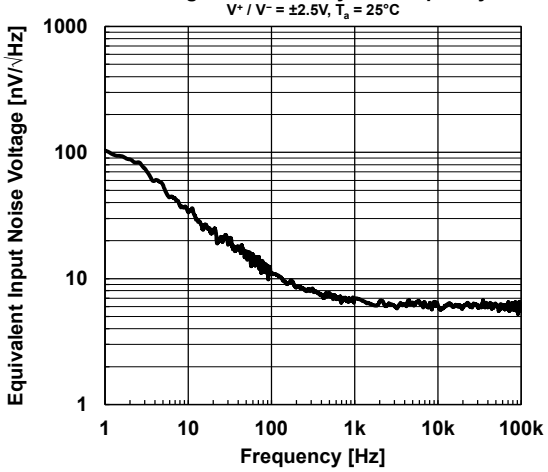
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

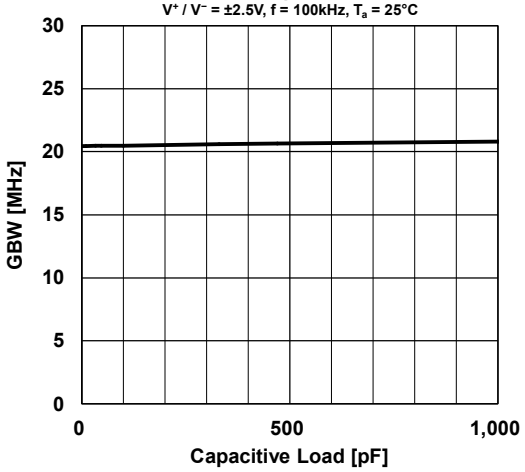
Gain / Phase vs. Frequency
V^+ / V^- = ±2.5V, R_F = 10kΩ, R_S = 20Ω, R_T = 50Ω,
V_{IN} = −46dBm, T_a = 25°C, C_L = 50pF



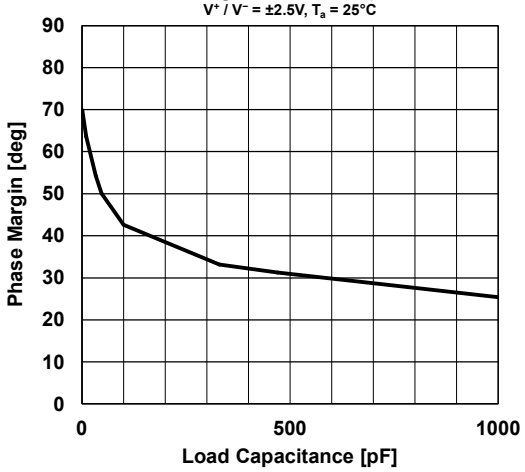
Voltage Noise Density vs. Frequency
V^+ / V^- = ±2.5V, T_a = 25°C



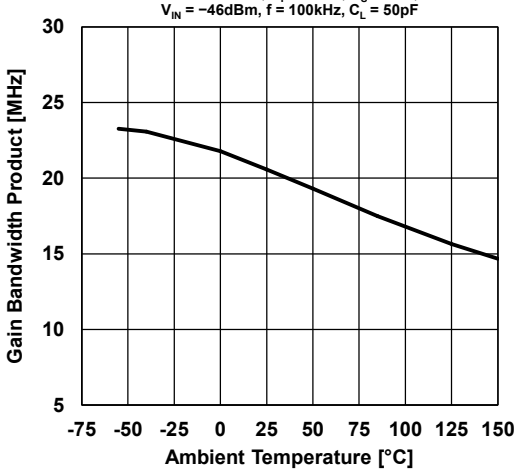
GBW vs. Capacitive Load
V^+ / V^- = ±2.5V, f = 100kHz, T_a = 25°C



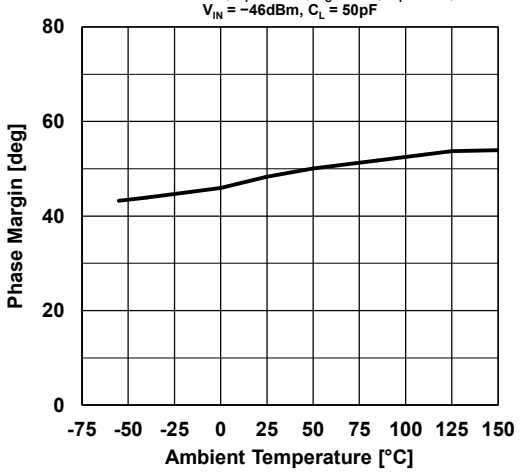
Phase Margin vs. Load Capacitance
V^+ / V^- = ±2.5V, T_a = 25°C



GBW vs. Temperature
V^+ / V^- = ±2.5V, R_F = 10kΩ, R_S = 20Ω,
V_{IN} = −46dBm, f = 100kHz, C_L = 50pF



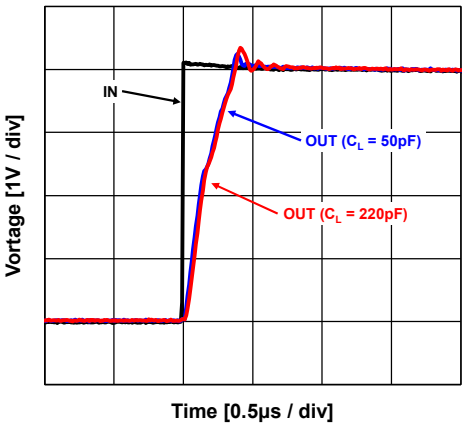
Phase Margin vs. Temperature
V^+ / V^- = ±2.5V, R_F = 10kΩ, R_S = 20Ω, R_T = 50Ω,
V_{IN} = −46dBm, C_L = 50pF



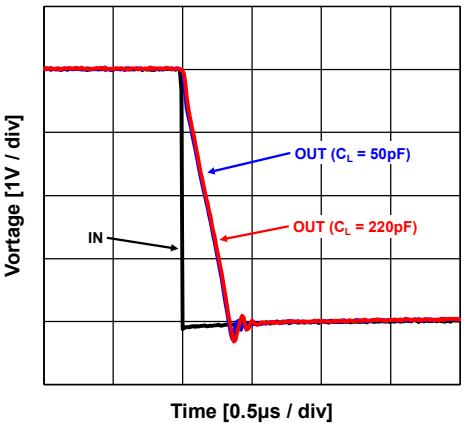
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

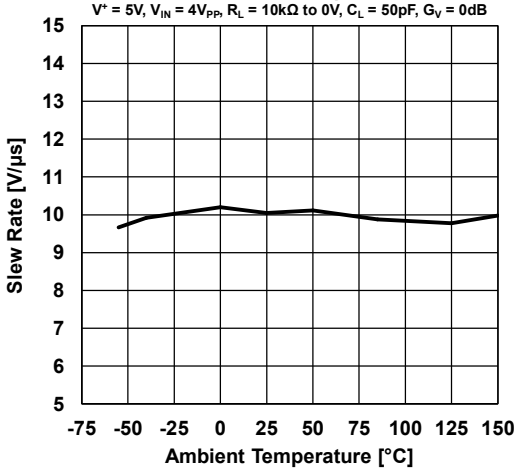
Pulse Response
V^+ = 5V, V_{IN} = 4V_{PP}, R_L = 10kΩ to 0V, G_V = 0dB, T_a = 25°C



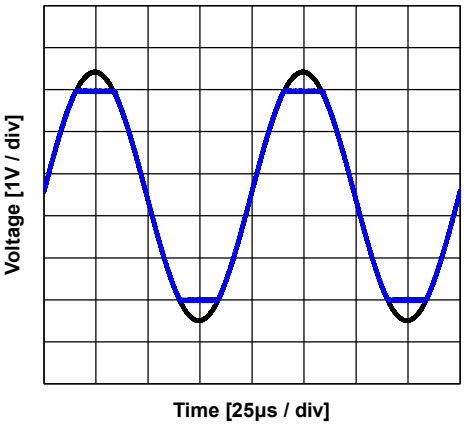
Pulse Response
V^+ = 5V, V_{IN} = 4V_{PP}, R_L = 10kΩ to 0V, G_V = 0dB, T_a = 25°C



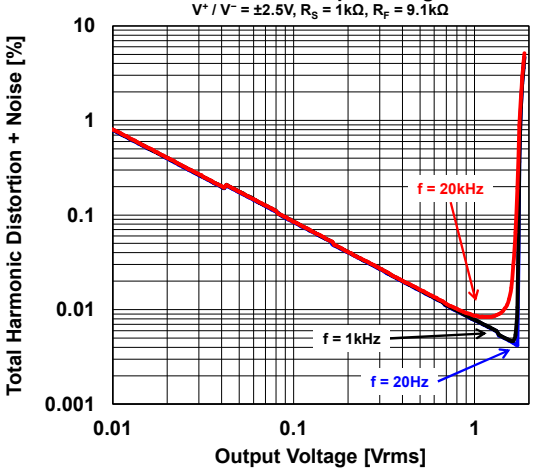
Slew Rate vs Temperature
V^+ = 5V, V_{IN} = 4V_{PP}, R_L = 10kΩ to 0V, C_L = 50pF, G_V = 0dB



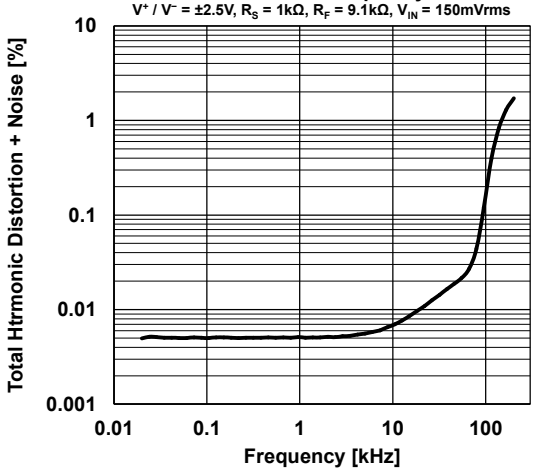
No Phase Reversal
V^+ = 5V, T_a = 25°C



THD+N vs. Output Voltage
V^+ / V^- = ±2.5V, R_S = 1kΩ, R_F = 9.1kΩ



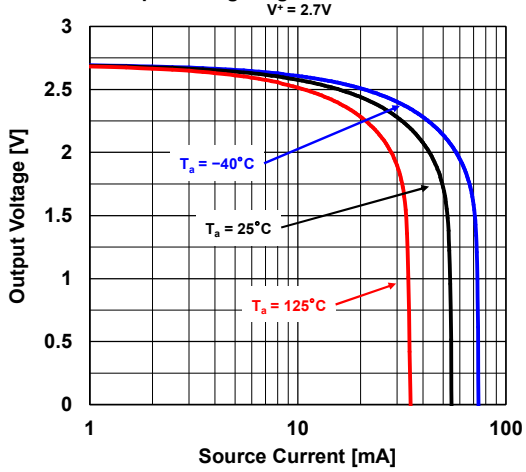
THD+N vs. Frequency
V^+ / V^- = ±2.5V, R_S = 1kΩ, R_F = 9.1kΩ, V_{IN} = 150mVrms



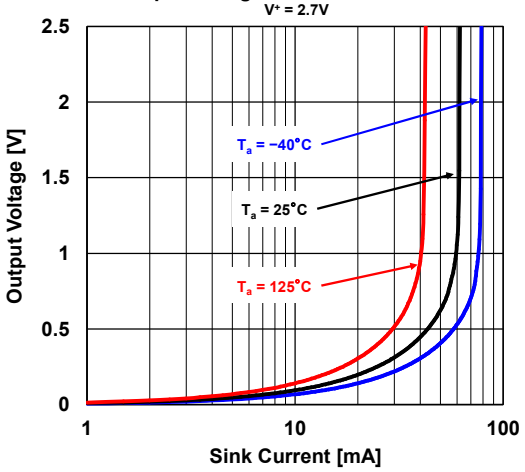
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

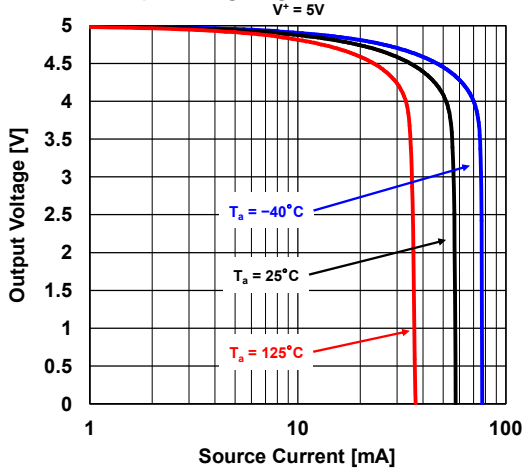
Output Voltage High vs. Source Current
V⁺ = 2.7V



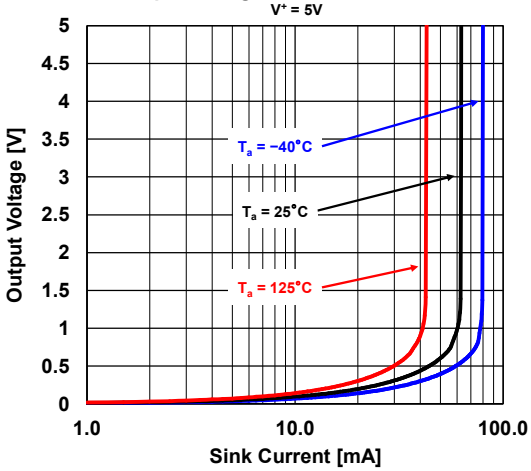
Output Voltage Low vs. Sink Current
V⁺ = 2.7V



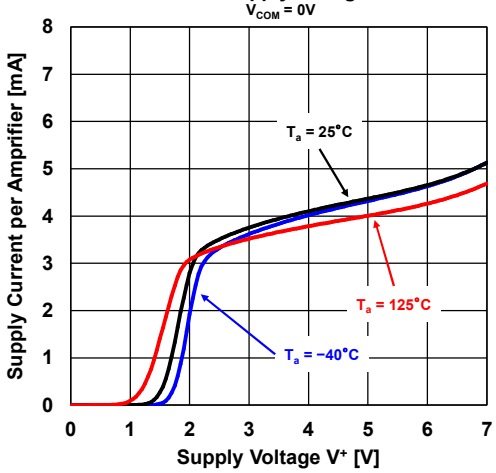
Output Voltage High vs. Source Current
V⁺ = 5V



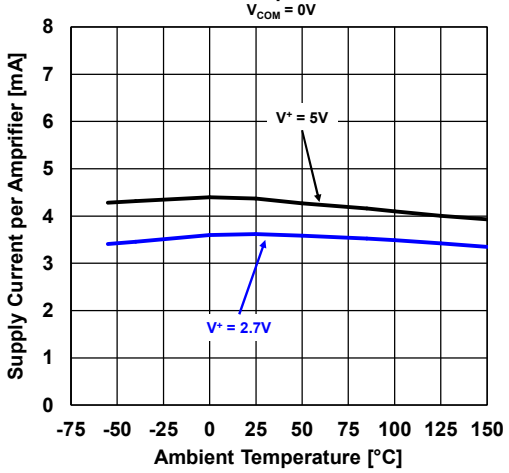
Output Voltage Low vs. Sink Current
V⁺ = 5V



Supply Current per Amprifier vs. Supply Voltage
V_{COM} = 0V



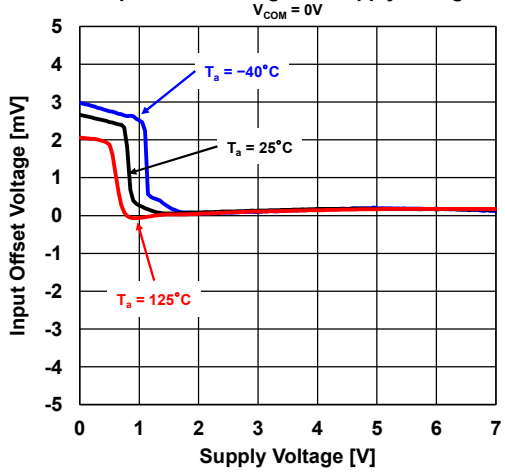
Supply Current per Ampreifier vs. Temperature
V_{COM} = 0V



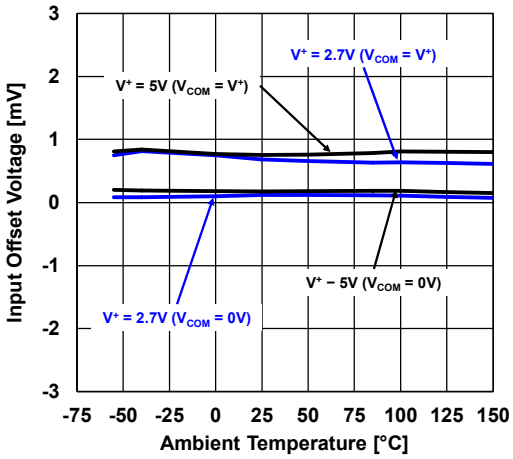
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

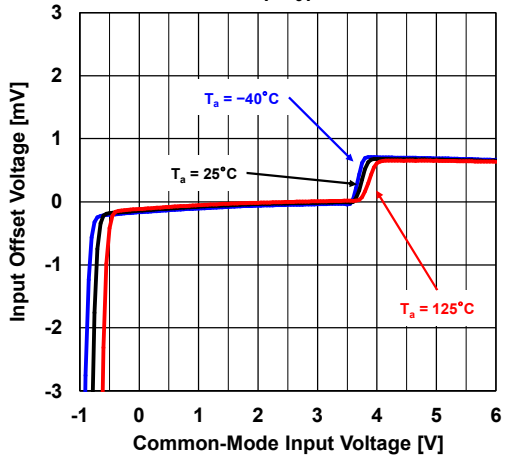
Input Offset Voltage vs. Supply Voltage
V_{COM} = 0V



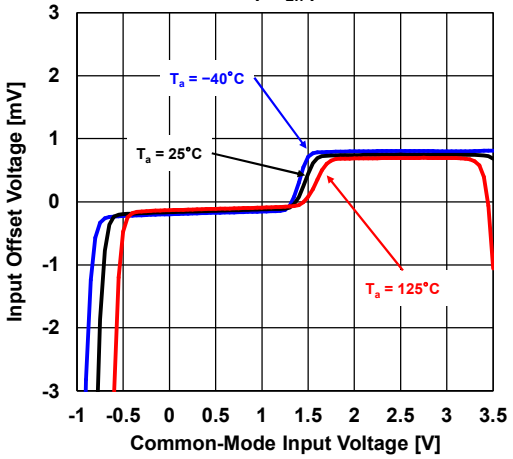
Input Offset Voltage vs. Temperature



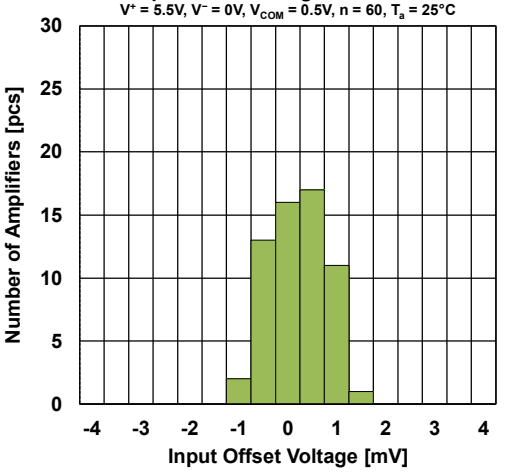
Input Offset Voltage
vs. Common-Mode Input Voltage
V+ = 5V



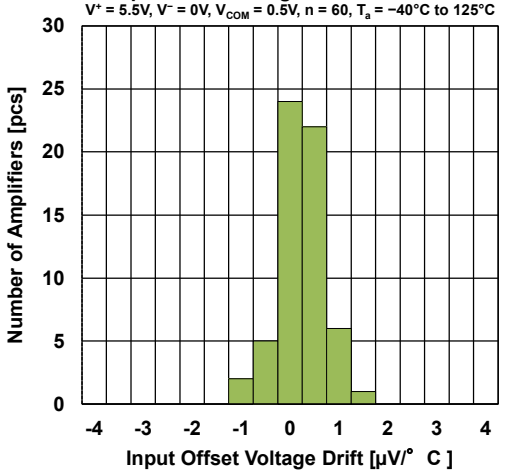
Input Offset Voltage
vs. Common-Mode Input Voltage
V+ = 2.7V



Input Offset Voltage Distribution
V+ = 5.5V, V− = 0V, V_{COM} = 0.5V, n = 60, T_a = 25°C



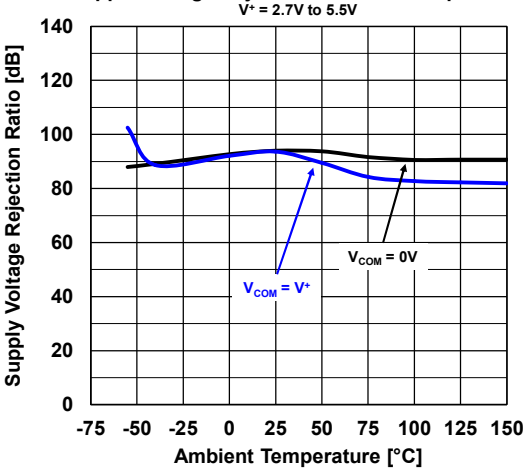
Input Offset Voltage Drift Distribution
V+ = 5.5V, V− = 0V, V_{COM} = 0.5V, n = 60, T_a = −40°C to 125°C



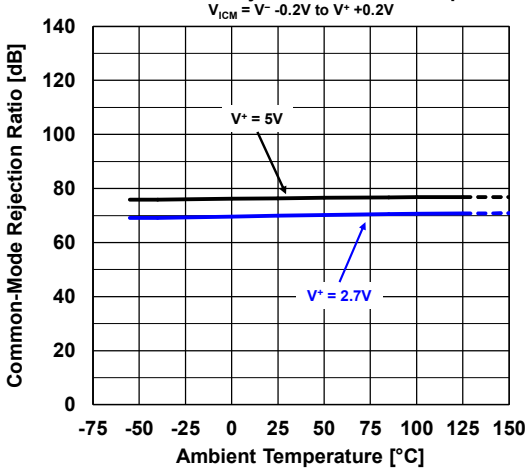
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

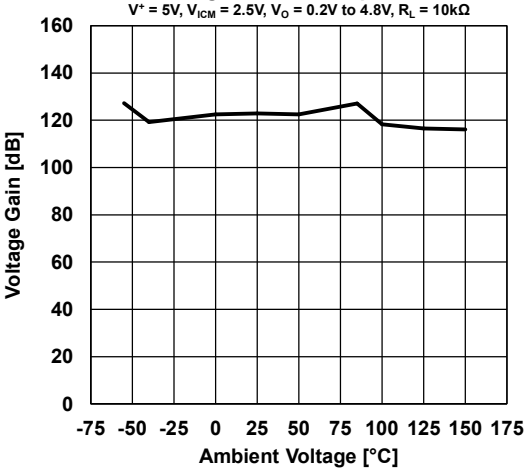
Supplu Voltage Rejection Ratio vs. Temperature
V^+ = 2.7V to 5.5V



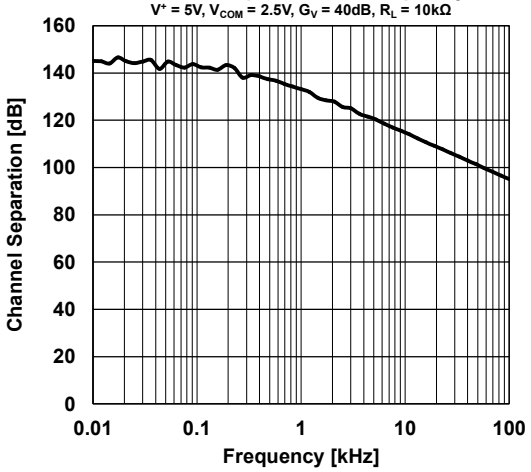
Common-Mode Rejection Ratio vs. Temperature
V_{ICM} = V^- -0.2V to V^+ +0.2V



Voltage Gain vs. Temperature
V^+ = 5V, V_{ICM} = 2.5V, V_O = 0.2V to 4.8V, R_L = 10kΩ



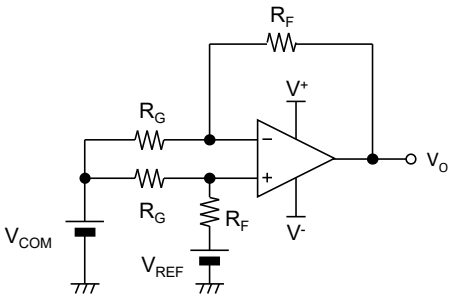
Channel Separation vs. Frequency
V^+ = 5V, V_{COM} = 2.5V, G_V = 40dB, R_L = 10kΩ



■ TEST CIRCUITS

● I_{SUPPLY}, V_{IO}, CMR, SVR

R_G = 50Ω, R_F = 50kΩ



$$V_{IO}=\frac{R_G}{(R_G+R_F)}\times(V_O-V_{REF})$$

$$CMR=20\log\frac{\Delta V_{COM}\left(1+\frac{R_F}{R_G}\right)}{\Delta V_O}$$

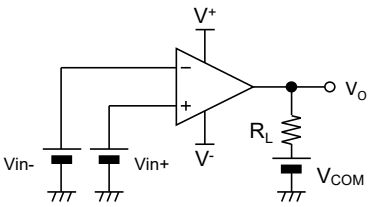
$$SVR=20\log\frac{\Delta V_S\left(1+\frac{R_F}{R_G}\right)}{\Delta V_O}$$

$V_S=V^+ - V^-$

$V_{REF}=V_S / 2$

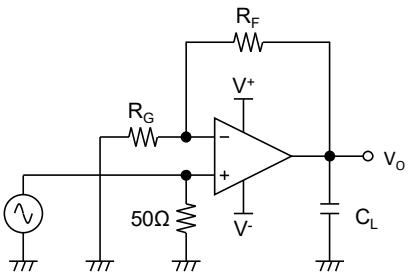
● V_{OH}, V_{OL}

$V_S = (V^+ - V^-) / 2$
V_{OH}; Vin+ = 1V, Vin- = 0V, $V_{COM} = V_S / 2$
V_{OL}; Vin+ = 0V, Vin- = 1V, $V_{COM} = V_S / 2$, V-



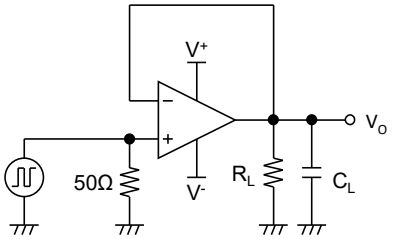
● GBW

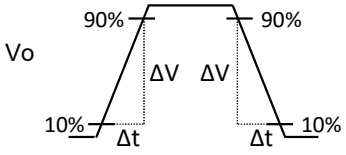
R_G = 1kΩ, R_F = 100kΩ



● SR

R_L = 100kΩ





$$SR=\frac{\Delta V}{\Delta t}$$

■ REVISION HISTORY

Date	Revision	Changes
May 30, 2019	Ver.1.0	Initial release
March 30, 2020	Ver.1.1	Collected condition of input voltage in RECOMMENDED OPERATING CONDITIONS.
May 24, 2022	Ver.1.2	Updated Data sheet format.

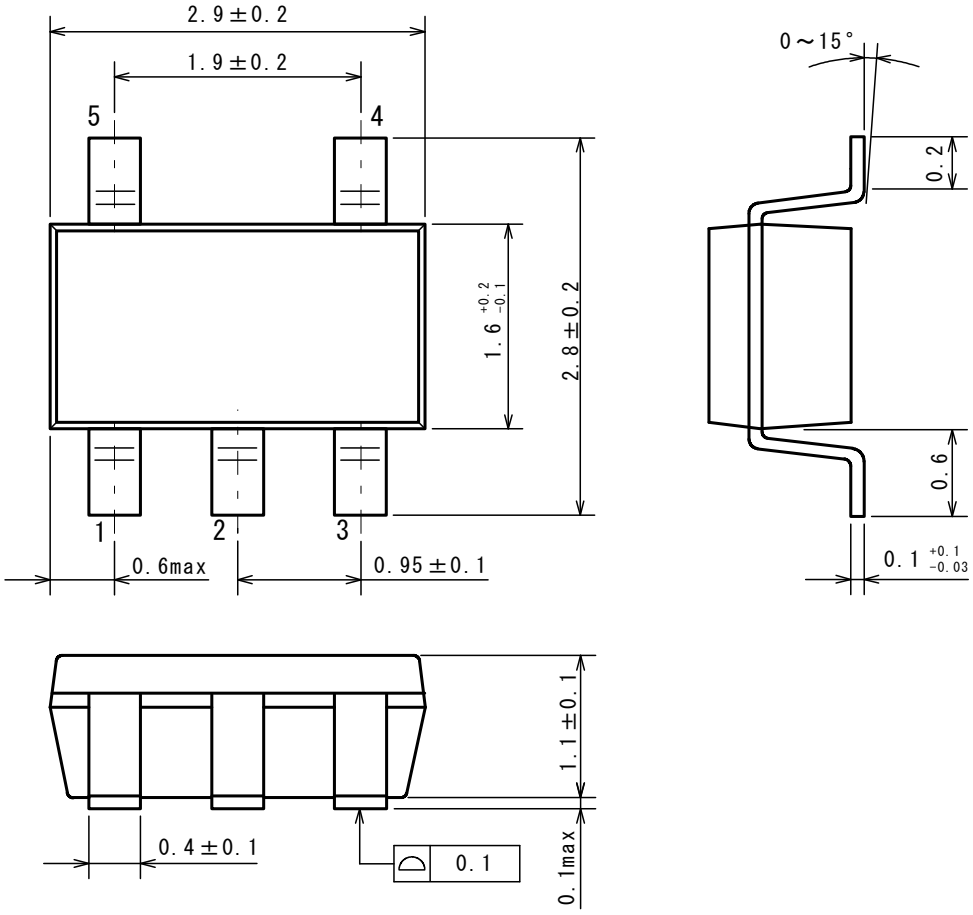
Nisshinbo Micro Devices Inc.

SOT-23-5

PI-SOT-23-5-E-A

■ PACKAGE DIMENSIONS

UNIT: mm



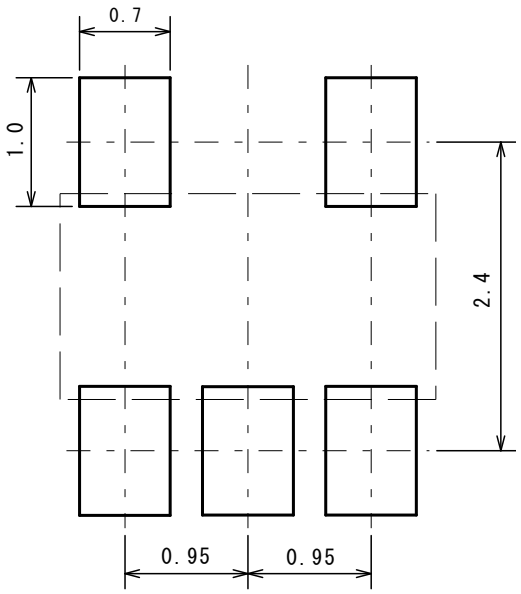
Nisshinbo Micro Devices Inc.

SOT-23-5

PI-SOT-23-5-E-A

■ EXAMPLE OF SOLDER PADS DIMENSIONS

UNIT: mm



Nisshinbo Micro Devices Inc.

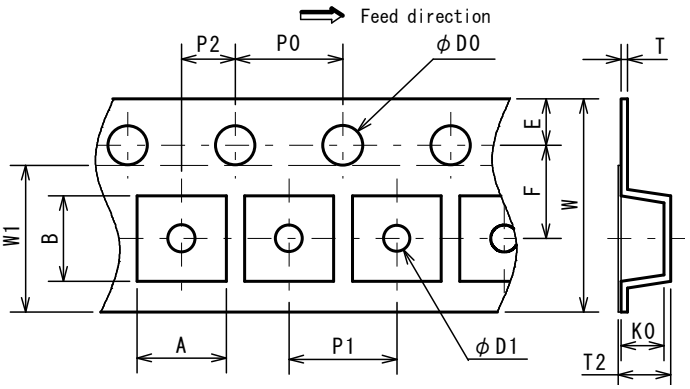
SOT-23-5

PI-SOT-23-5-E-A

■ PACKING SPEC

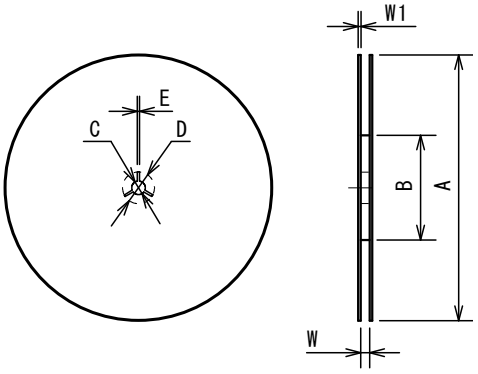
UNIT: mm

TAPING DIMENSIONS



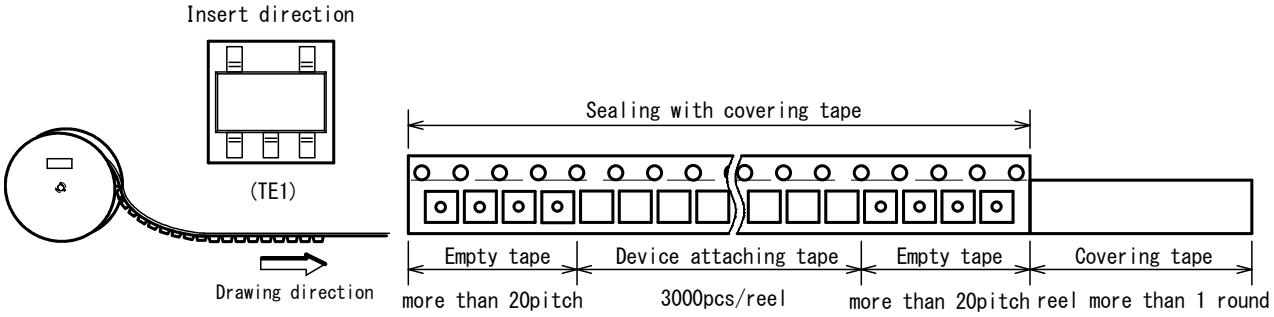
SYMBOL	DIMENSION	REMARKS
A	3.3±0.1	BOTTOM DIMENSION
B	3.2±0.1	BOTTOM DIMENSION
D0	1.55	
D1	1.05	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.82	
K0	1.5±0.1	
W	8.0±0.3	
W1	5.5	THICKNESS 0.1MAX

REEL DIMENSIONS

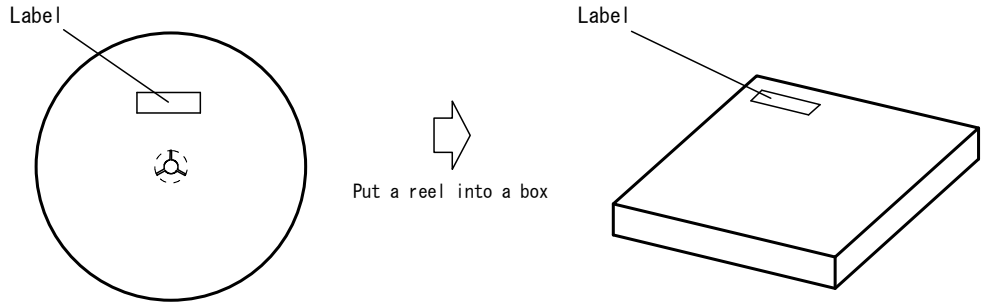


SYMBOL	DIMENSION
A	φ180±1
B	φ 60±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9±0.5
W1	1.2±0.2

TAPING STATE



PACKING STATE



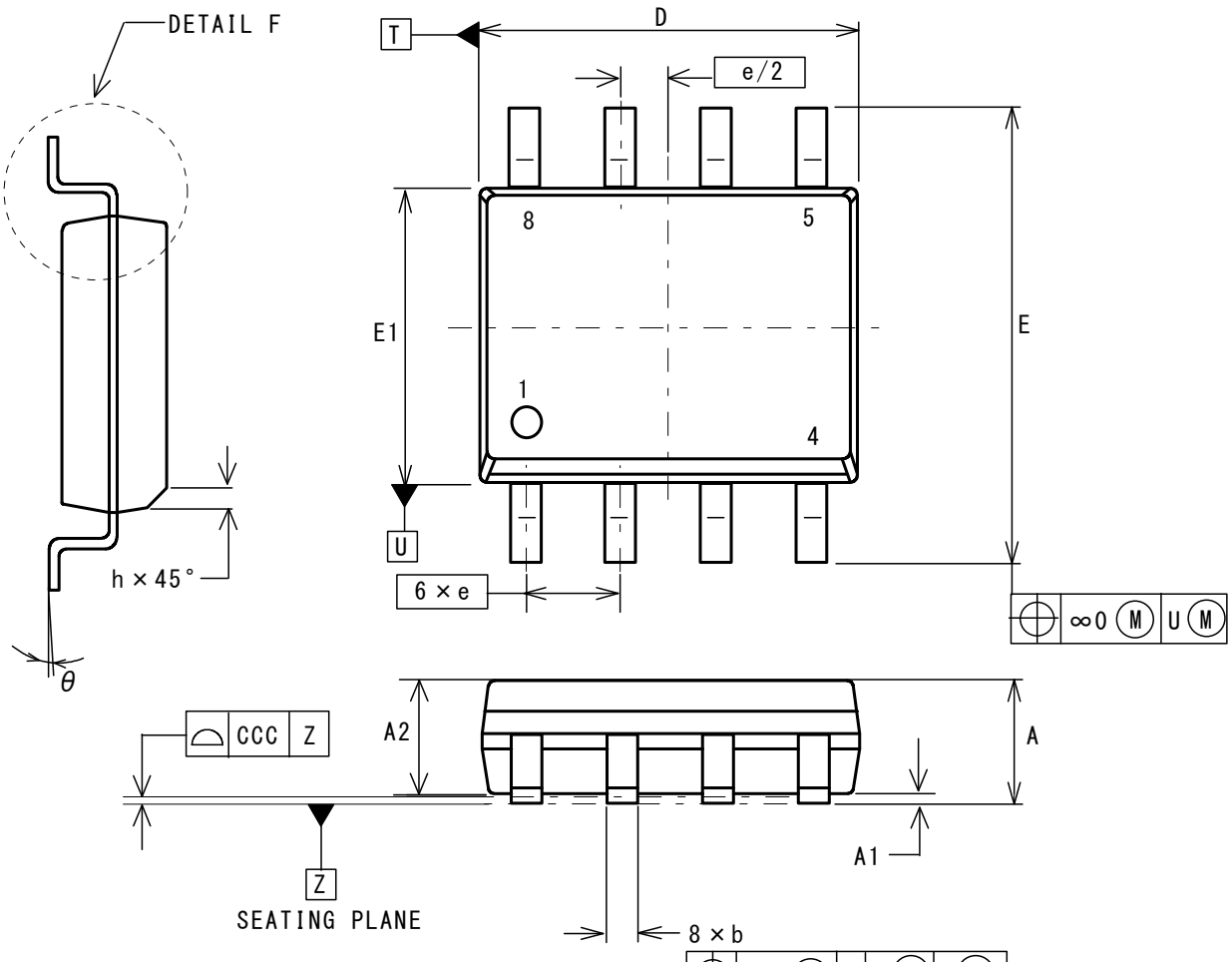
Nisshinbo Micro Devices Inc.

SOP8

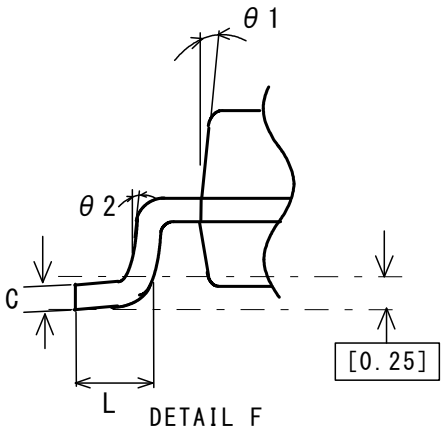
PI-SOP8-E-A

■ PACKAGE DIMENSIONS

UNIT: mm



DESCRIPTION	SYMBOL	INCH			MILLIMETER		
		MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.053		.069	1.35		1.75
STAND OFF	A_1	.004		.010	0.10		0.25
MOLD THICKNESS	A_2	.049		–	1.25		–
LEAD WIDTH	b	.014		.019	0.35		0.49
L/F THICKNESS	C	.007		.010	0.19		0.25
BODY SIZE	D	.189		.197	4.80		5.00
	E_1	.150		.157	3.80		4.00
LEAD PITCH	E	.228		.244	5.80		6.20
	e	.050 BSC			1.27 BSC		
	L	.015		.049	0.40		1.25
	h	.010		.020	0.25		0.50
	θ	0°		8°	0°		7°
	θ_1	5°		15°	5°		15°
	θ_2	2°	7°	12°	2°	7°	12°
LEAD EDGE OFFSET	∞0	.010			0.25		
LEAD OFFSET	bbb	.010			0.25		
COPLANARITY	CCC	.004			0.10		

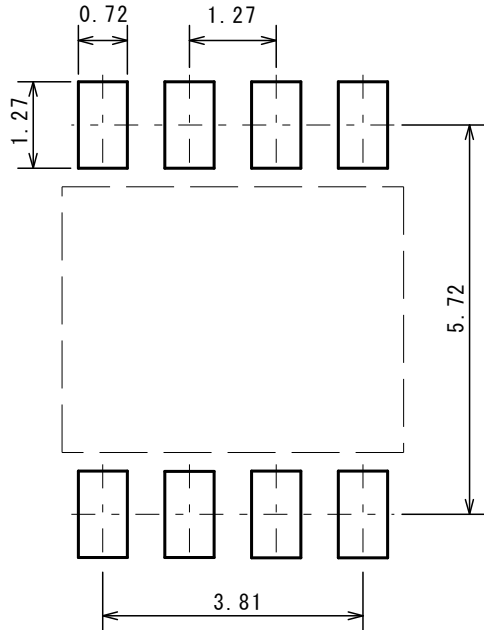


SOP8

PI-SOP8-E-A

■ **EXAMPLE OF SOLDER PADS DIMENSIONS**

UNIT: mm



Nisshinbo Micro Devices Inc.

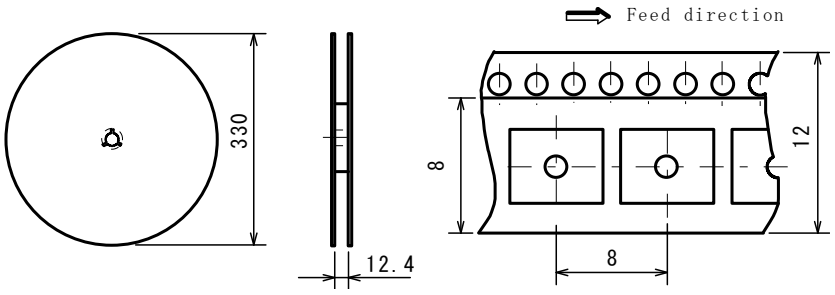
SOP8

PI-SOP8-E-A

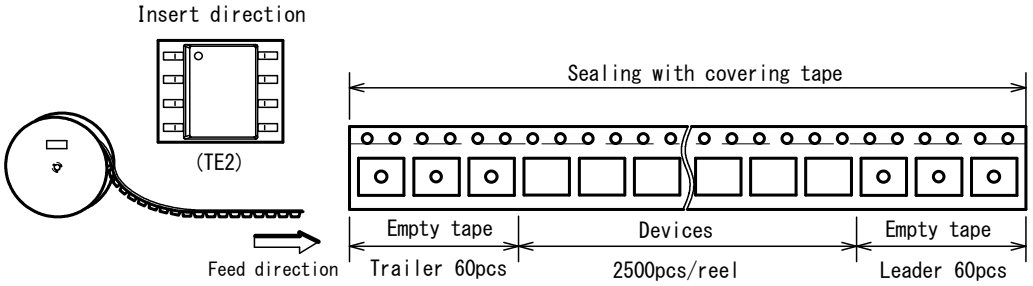
■ PACKING SPEC

UNIT: mm

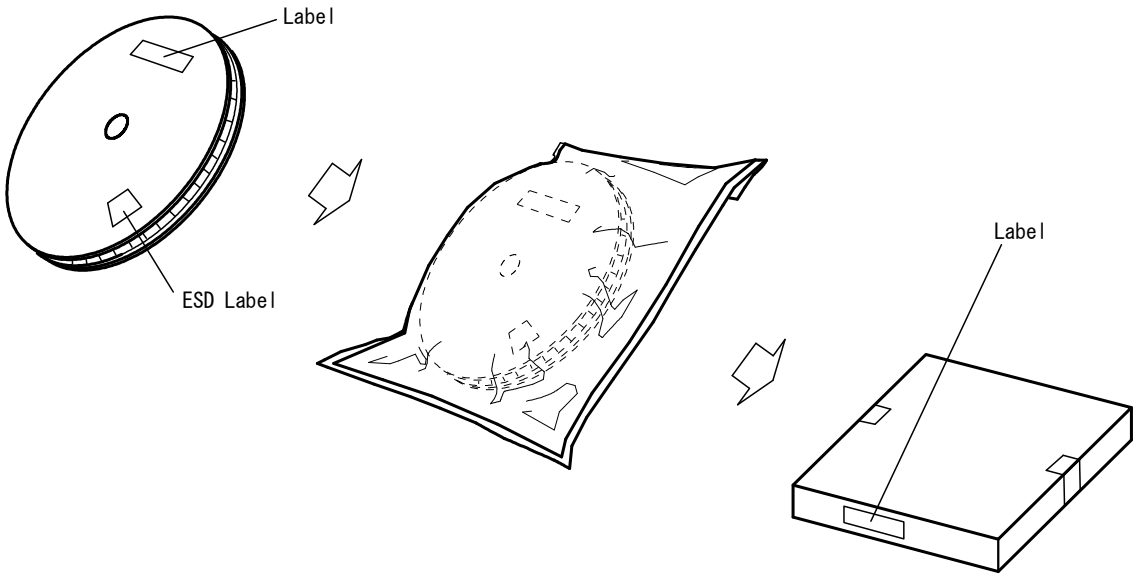
REEL DIMENSIONS / TAPING DIMENSIONS



TAPING STATE



PACKING STATE



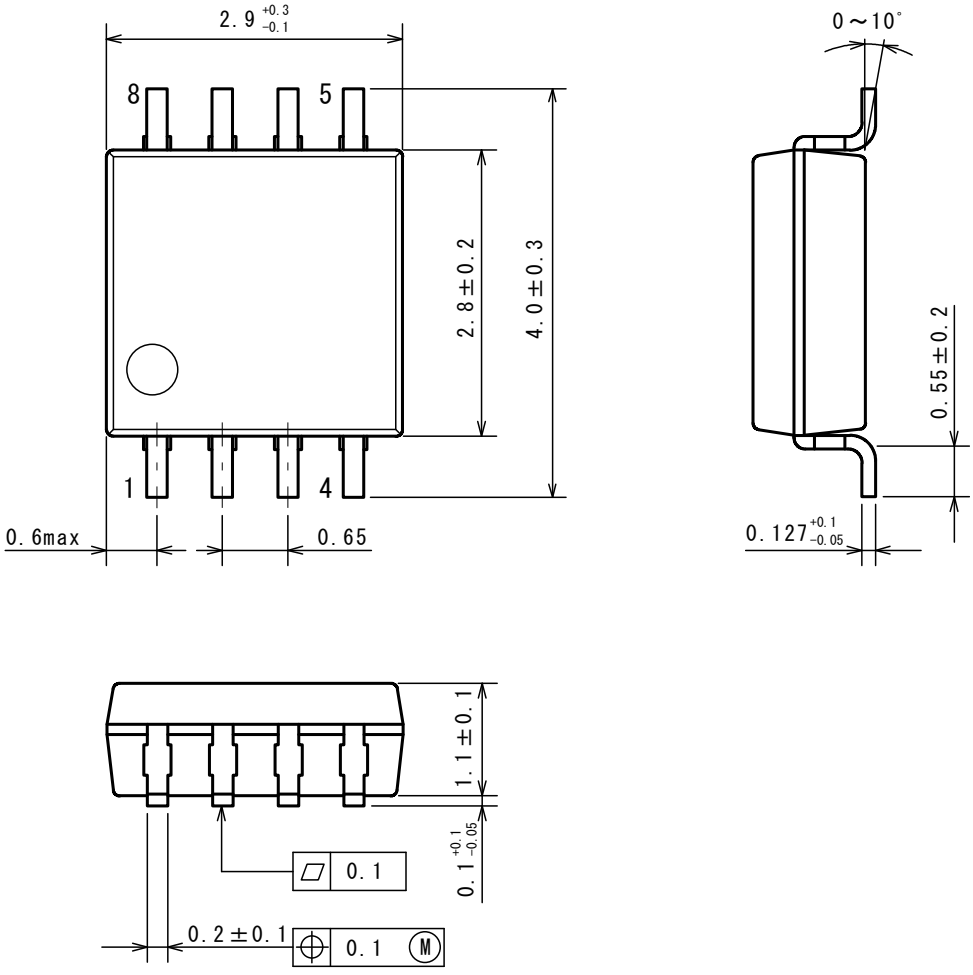
Nisshinbo Micro Devices Inc.

MSOP8 MEET JEDEC MO-187-DA (VSP8)

PI-MSOP8-E-A

■ PACKAGE DIMENSIONS

UNIT: mm



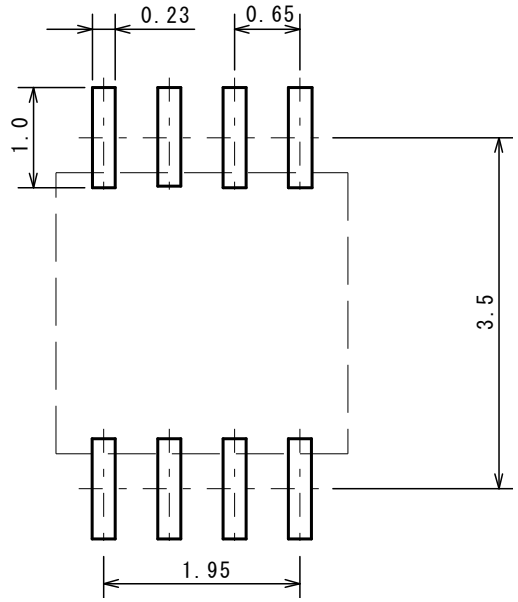
Nisshinbo Micro Devices Inc.

MSOP8 MEET JEDEC MO-187-DA (VSP8)

PI-MSOP8-E-A

■ **EXAMPLE OF SOLDER PADS DIMENSIONS**

UNIT: mm



Nisshinbo Micro Devices Inc.

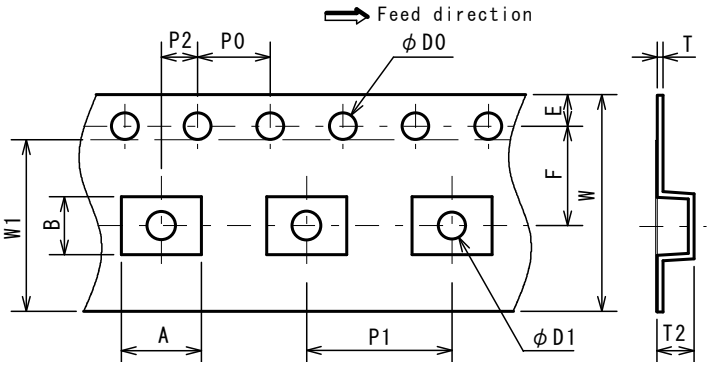
MSOP8 MEET JEDEC MO-187-DA (VSP8)

PI-MSOP8-E-A

■ PACKING SPEC

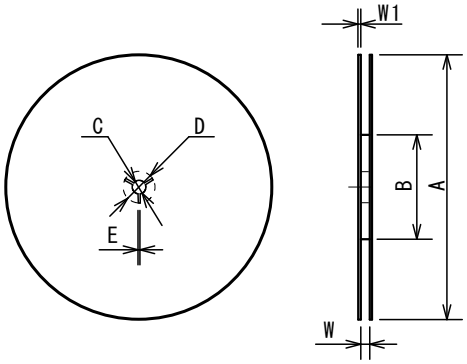
UNIT: mm

TAPING DIMENSIONS



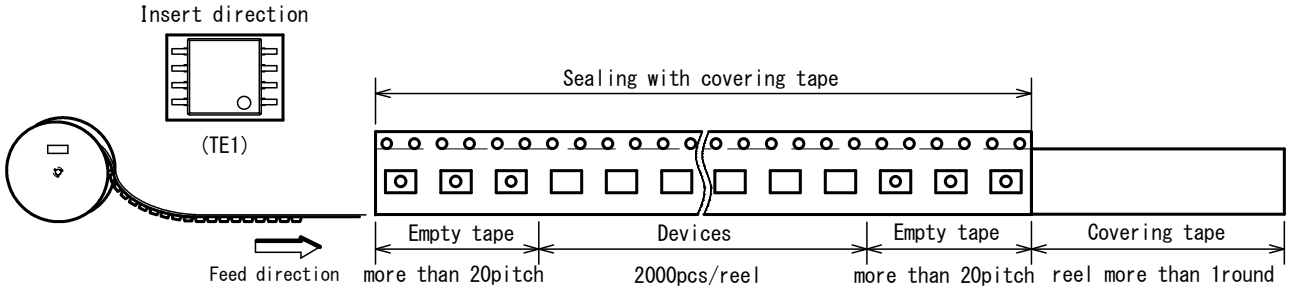
SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
B	3.2	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.30±0.05	
T2	2.0 (MAX.)	
W	12.0±0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

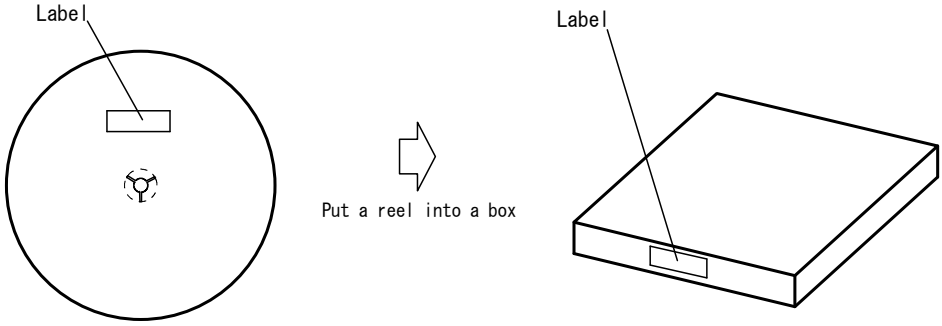


SYMBOL	DIMENSION
A	φ254±2
B	φ100±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	2.0±0.2

TAPING STATE



PACKING STATE



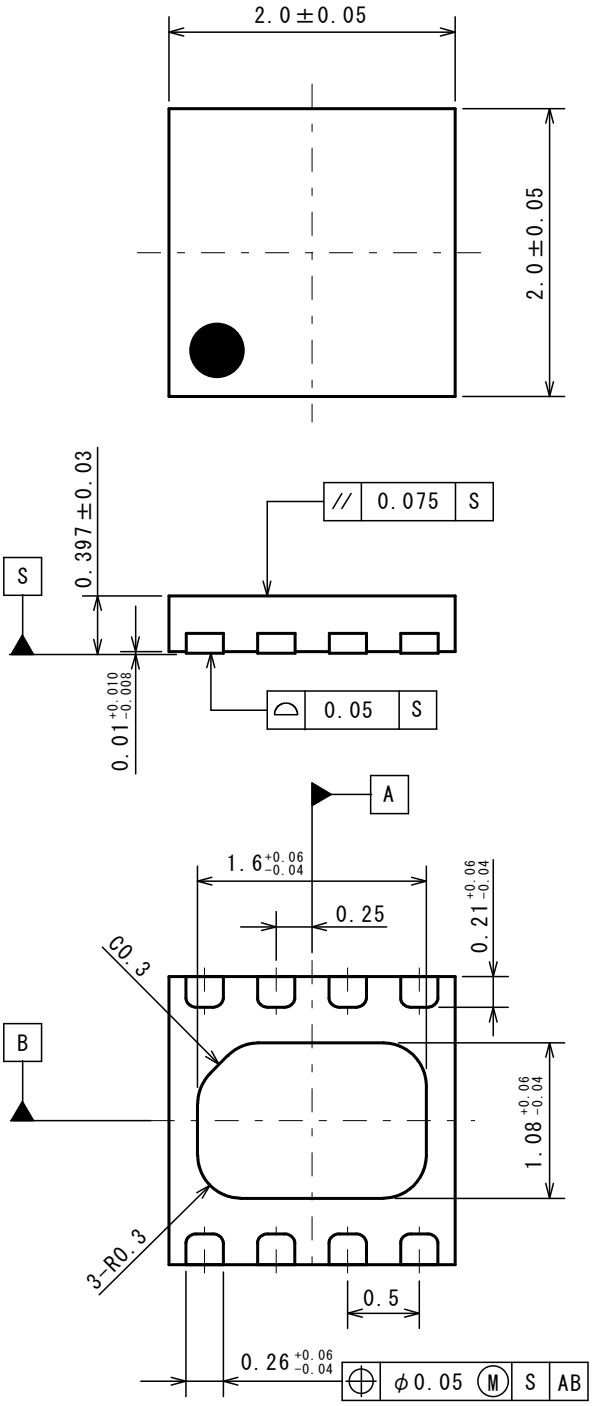
Nisshinbo Micro Devices Inc.

DFN8-U1 (ESON8-U1)

PI-DFN8-U1-E-A

■ PACKAGE DIMENSIONS

UNIT: mm



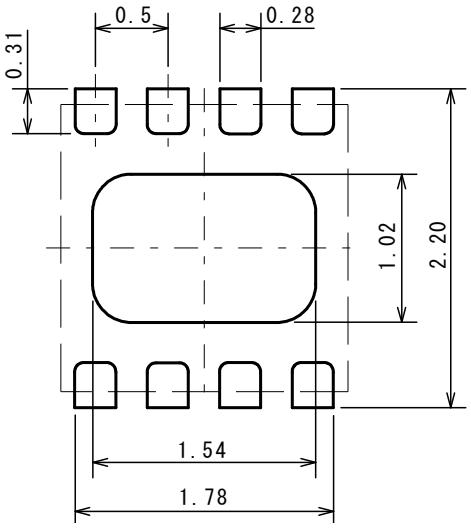
Nisshinbo Micro Devices Inc.

DFN8-U1 (ESON8-U1)

PI-DFN8-U1-E-A

■ EXAMPLE OF SOLDER PADS DIMENSIONS

UNIT: mm



Nisshinbo Micro Devices Inc.

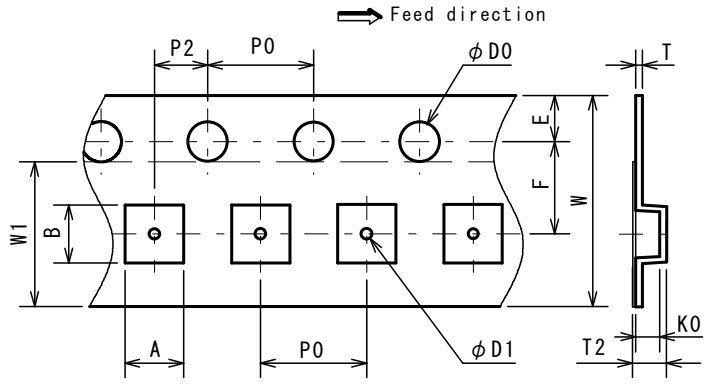
DFN8-U1 (ESON8-U1)

PI-DFN8-U1-E-A

■ PACKING SPEC

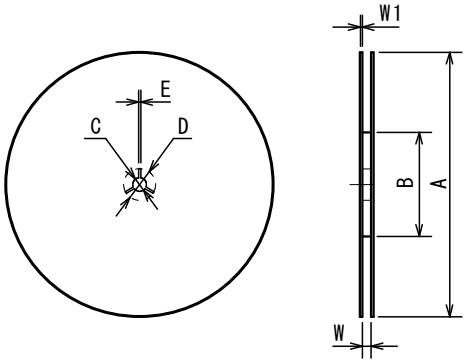
UNIT: mm

TAPING DIMENSIONS



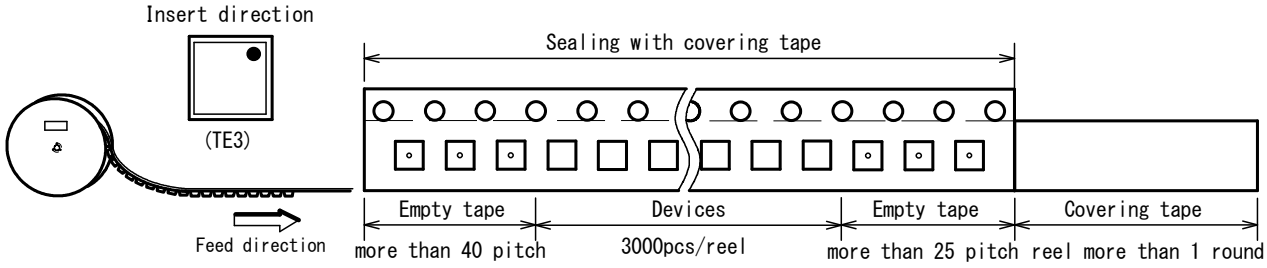
SYMBOL	DIMENSION	REMARKS
A	2.25±0.05	BOTTOM DIMENSION
B	2.25±0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	0.5±0.1	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.00±0.07	
K0	0.65±0.05	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

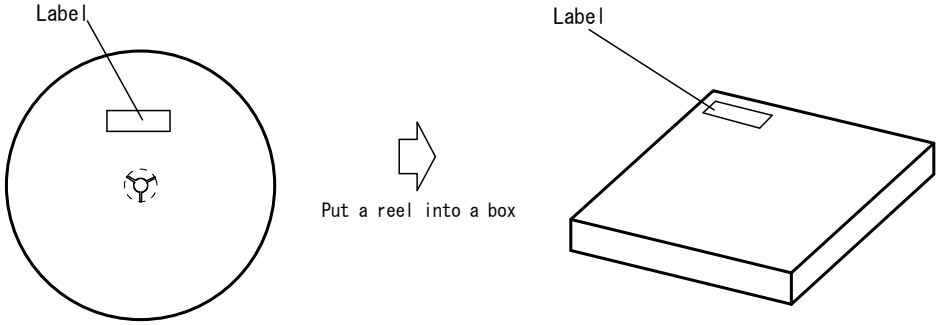


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-1.5}$
B	$\phi 60^{+1}_{0}$
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	$9^{+0.3}_{0}$
W1	1.2

TAPING STATE



PACKING STATE



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    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
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    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

    In case your company desires to use this product for any applications other than general electronic equipment mentioned above, make sure to contact our company in advance. Note that the important requirements mentioned in this section are not applicable to cases where operation requirements such as application conditions are confirmed by our company in writing after consultation with your company.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty
    8-1. Quality Warranty Period
    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

NISSHINBO

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