

PHB23NQ10LT

N-channel TrenchMOS logic level FET

Rev. 01 — 11 July 2006

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level threshold
- Fast switching
- TrenchMOS technology

1.3 Applications

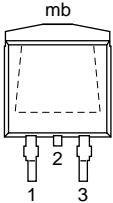
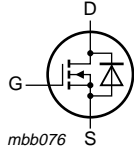
- DC-to-DC converters
- Switched-mode power supplies
- General purpose switching

1.4 Quick reference data

- $V_{DS} \leq 100$ V
- $R_{DSon} \leq 72$ m Ω
- $I_D \leq 23$ A
- $Q_{GD} = 9.3$ nC (typ)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D) [1]		
3	source (S)		
mb	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 2. Ordering information

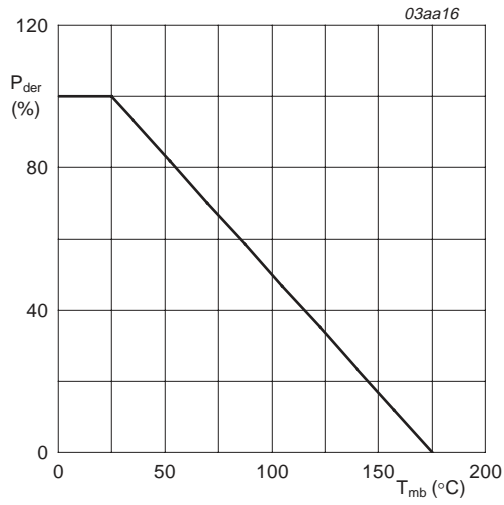
Type number	Package		Version
	Name	Description	
PHB23NQ10LT	D2PAK	plastic single-ended surface-mounted package; 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 3. Limiting values

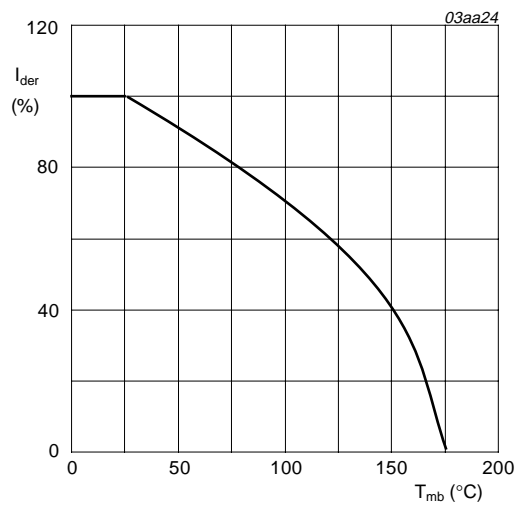
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-	± 15	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	23	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	16	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	91	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 1	-	98	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	23	A
I_{SM}	peak source current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	92	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 14.2\text{ A}$; $V_{DS} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; starting at $T_j = 25\text{ °C}$	-	100	mJ



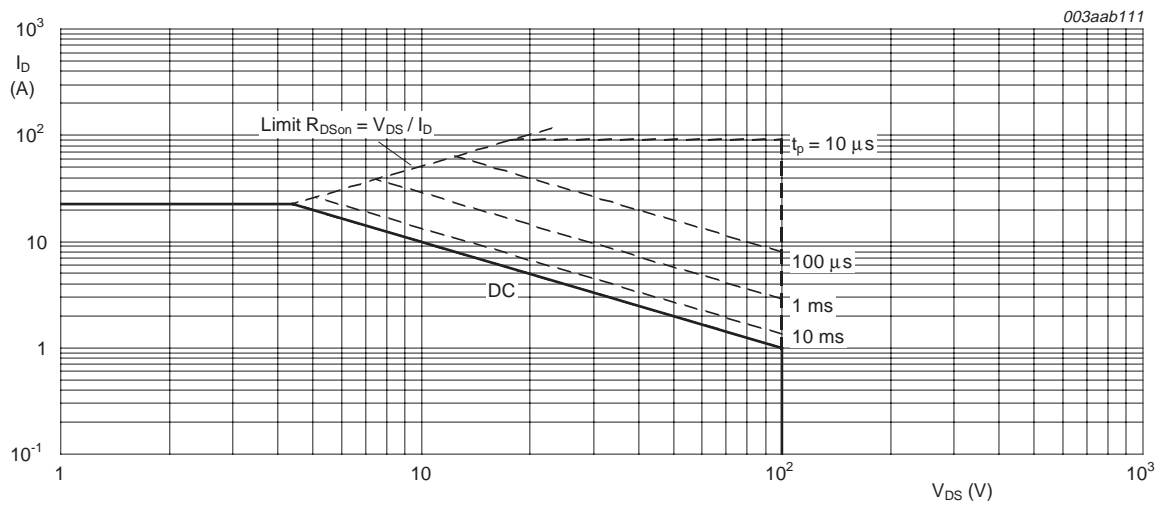
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



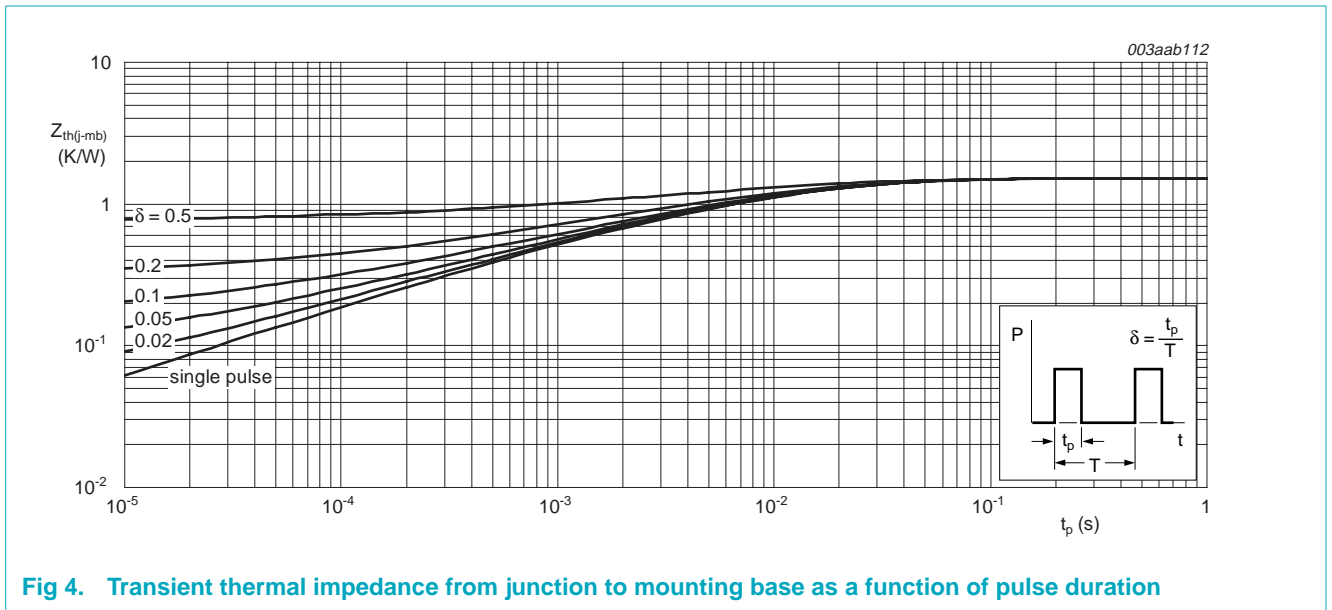
T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

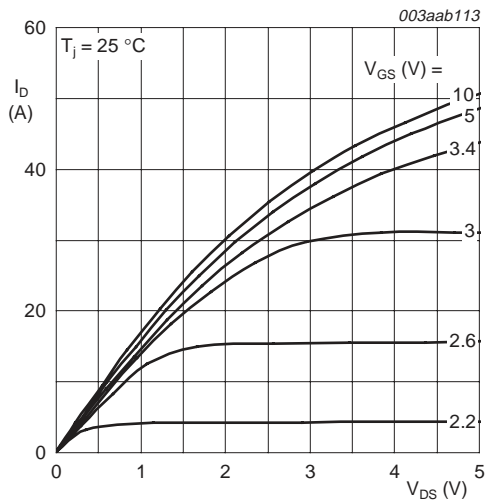
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint, FR4 board	-	50	-	K/W



6. Characteristics

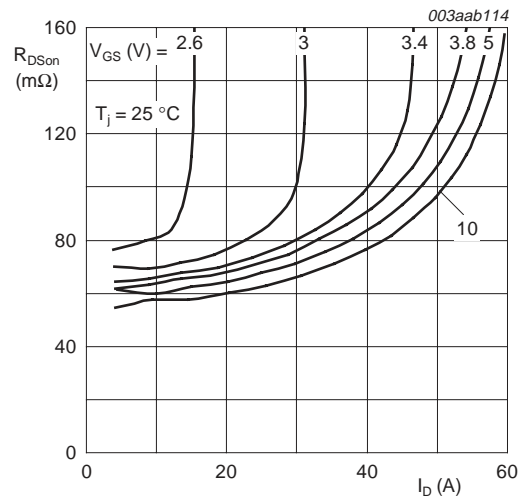
Table 5. Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C	100	-	-	V
		T _j = -55 °C	89	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; see Figure 9 and 10 T _j = 25 °C	1	1.5	2	V
		T _j = 175 °C	0.5	-	-	V
		T _j = -55 °C	-	-	2.3	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V T _j = 25 °C	-	0.05	10	μA
		T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	-	2	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 10 A; see Figure 6 and 8 T _j = 25 °C	-	60	75	mΩ
		T _j = 175 °C	-	-	203	mΩ
		V _{GS} = 10 V; I _D = 10 A; see Figure 6 and 8	-	55	72	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 44 V; V _{GS} = 10 V; see Figure 11 and 12	-	49	-	nC
Q _{GS}	gate-source charge		-	3.7	-	nC
Q _{GD}	gate-drain charge		-	9.3	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	1278	1704	pF
C _{oss}	output capacitance		-	129	155	pF
C _{rss}	reverse transfer capacitance		-	88	120	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _G = 10 Ω	-	13	20	ns
t _r	rise time		-	120	168	ns
t _{d(off)}	turn-off delay time		-	58	87	ns
t _f	fall time		-	57	86	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; see Figure 13 I _S = 23 A; V _{GS} = 0 V	-	0.85	1.2	V
			-	1.1	-	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;	-	6.3	-	ns
Q _r	recovered charge	V _R = 30 V	-	0.22	-	μC



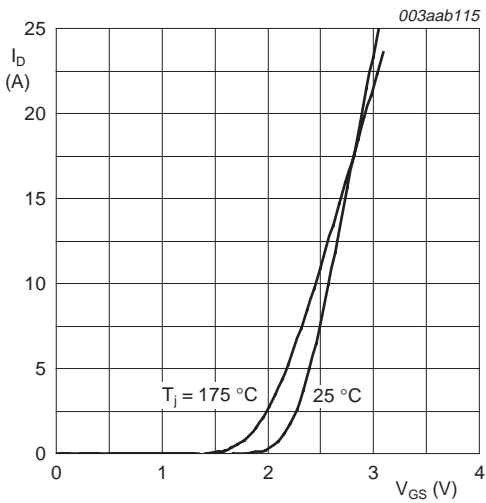
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



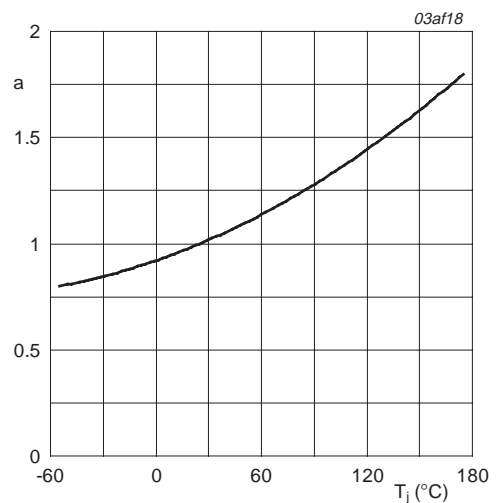
$T_j = 25\text{ °C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



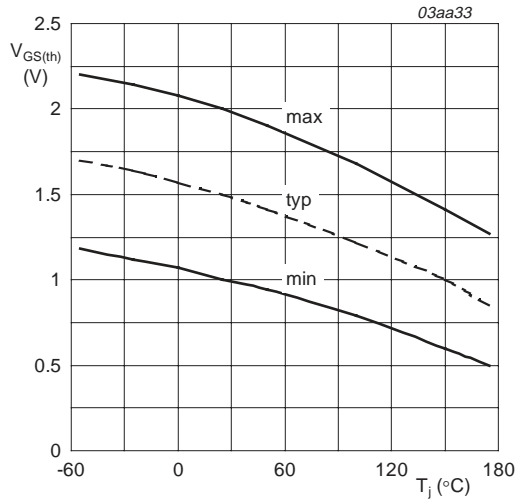
$T_j = 25\text{ °C and }175\text{ °C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



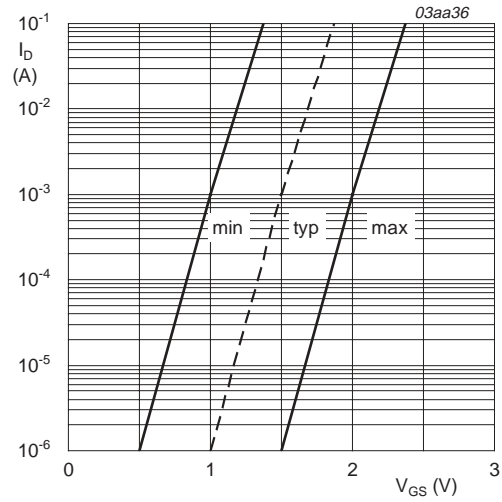
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



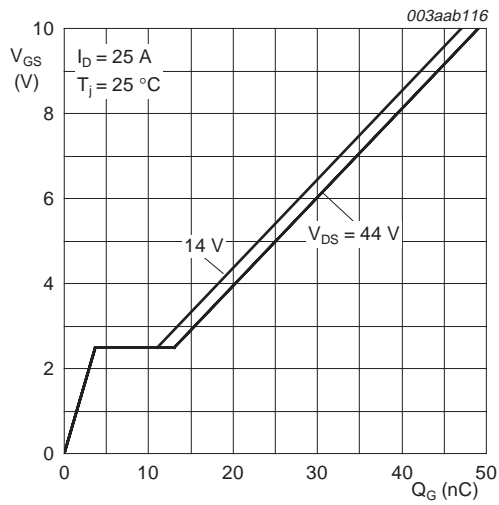
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 25 \text{ A}; V_{DS} = 14 \text{ V and } 44 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

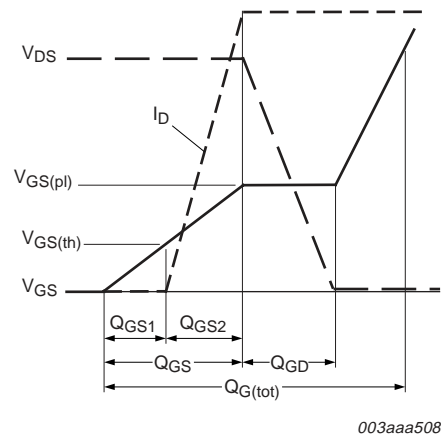
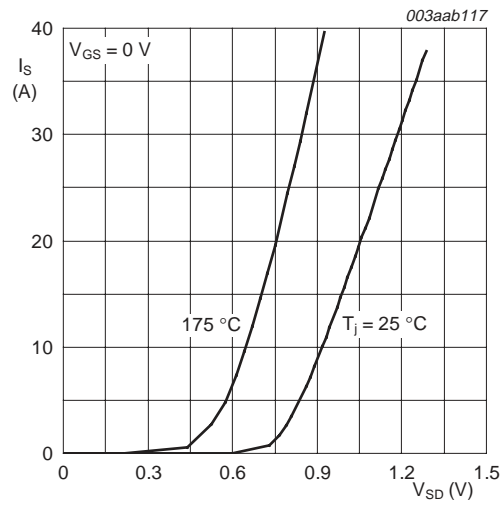


Fig 12. Gate charge waveform definitions



$T_j = 25 \text{ °C}$ and 175 °C ; $V_{GS} = 0 \text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

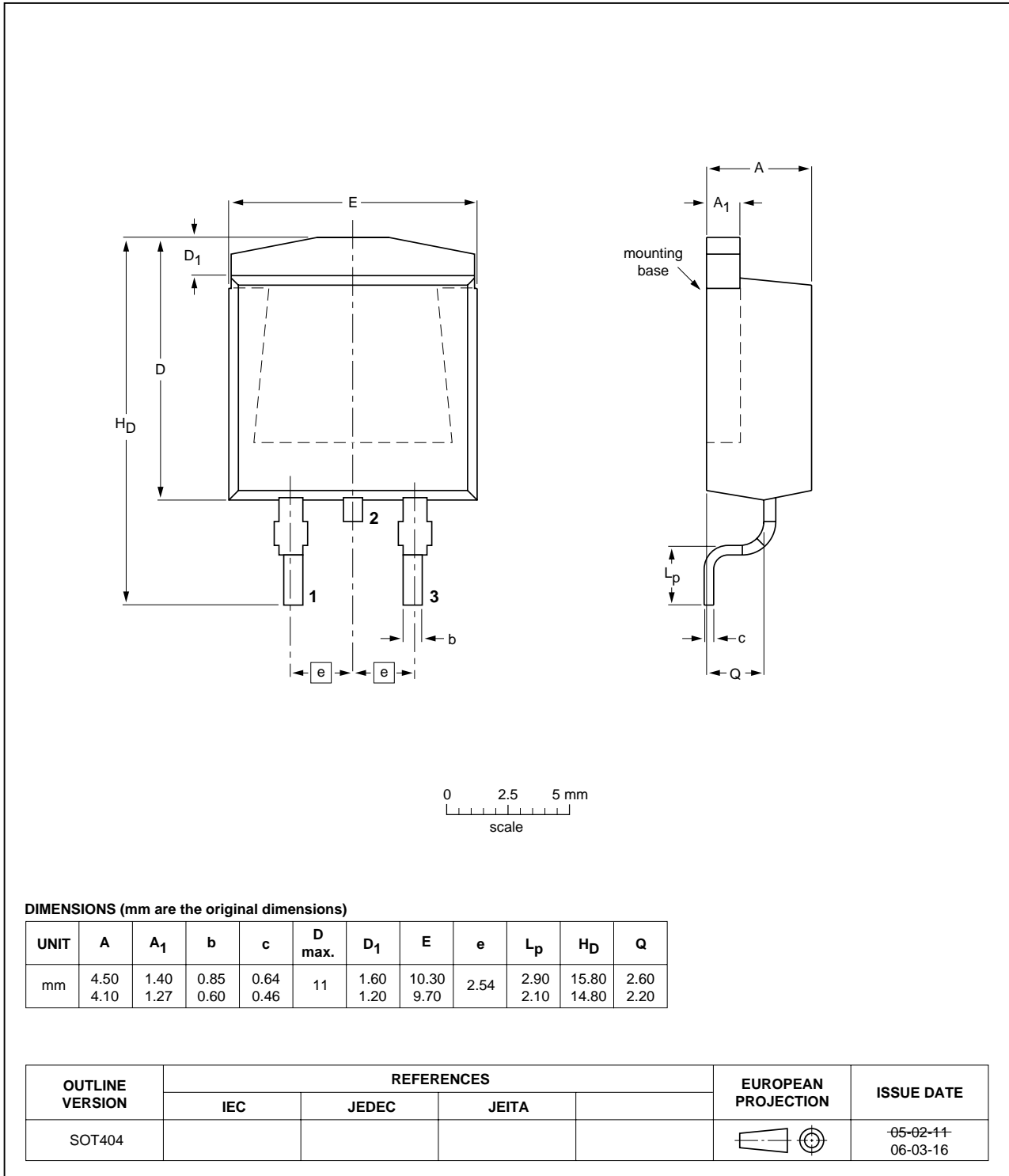


Fig 14. Package outline SOT404 (D2PAK)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHB23NQ10LT_1	20060711	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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