ADC1207S080

Single 12 bits ADC, up to 80 MHz with direct/ultra high IF sampling

Rev. 03 — 2 July 2012 Product data sheet

1. General description

The ADC1207S080 is a 12-bit Analog-to-Digital Converter (ADC) optimized for direct Input Frequency (IF) sampling and supporting the most demanding use conditions in ultra high IF radio transceivers for cellular infrastructure and other applications such as wireless infrastructure, optical networking and fixed telecommunication. Due to its broadband input capabilities, the ADC1207S080 is ideal for single and multiple carriers data conversion.

Operating at a maximum sampling rate of 80 MHz, analog input signals are converted into 12-bit binary coded digital words. All static digital inputs are CMOS compatible. All output signals are Low-Voltage Complementary Metal-Oxide Semiconductor (LVCMOS) compatible. The ADC1207S080 offers the most flexible acquisition control system because of its programmable Complete Conversion Signal (CCS) that allows to adjust the delay of the acquisition clock.

The ADC1207S080 offers the lowest input capacitance (< 1 pF) and therefore the highest flexibility in front-end aliasing filter strategy because of its internal front-end buffer.

2. Features

- 12-bit resolution
- Differential input with 375 MHz bandwidth
- 90 dB SFDR; 71 dB S/N (f_i = 225 MHz; f_{clk} = 80 MHz; B = 5 MHz)
- 74 dB SFDR; 66.5 dB S/N (f_i = 175 MHz; f_{clk} = 80 MHz; B = Nyquist)
- High speed sampling rate up to 80 MHz
- Internal front-end buffer (input capacitance < 1 pF)
- Programmable acquisition output clock (complete conversion signal)
- Full-scale controllable from 1.5 V to 2 V (p-p); continuous scale
- Single 5 V power supply
- 3.3 V LVCMOS compatible digital outputs
- Binary or two’s-complement LVCMOS outputs
- CMOS compatible static digital inputs
- Only 2 clock cycles latency
- Industrial temperature range from −40 °C to +85 °C
- HTQFP48 package

3. Applications

High speed analog to digital conversion for:

- Radio transceivers
- Wireless infrastructure
- Cable modem
- Digital storage scope
- Fixed telecommunication,
- Optical networking
- Wireless Local Area Network (WLAN) infrastructure.
- General purpose applications

4. Ordering information

Table 1. Ordering information

Type number	Package			Sampling frequency (MHz)
	Name	Description	Version	
ADC1207S080HW	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body 7 × 7 × 1 mm; exposed die pad	SOT545-2	80

5. Block diagram

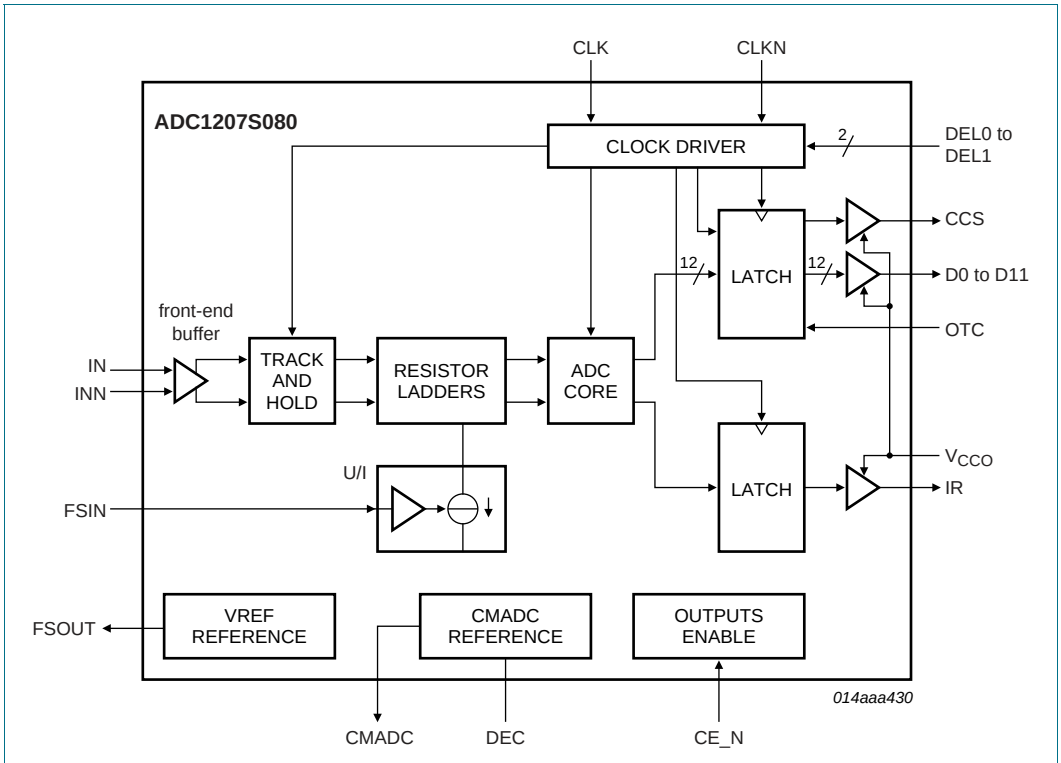


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

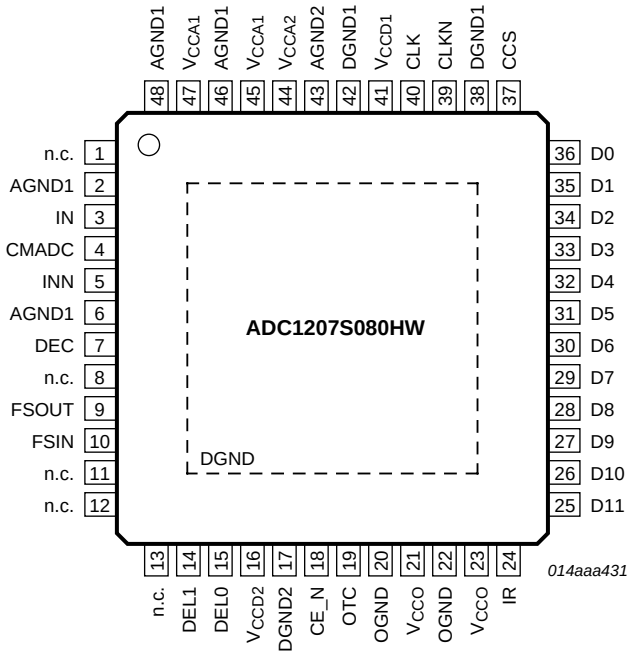


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type [1]	Description
n.c.	1	-	not connected
AGND1	2	G	analog ground 1
IN	3	I	analog input voltage
CMADC	4	O	regulator common mode ADC output
INN	5	I	complementary analog input voltage
AGND1	6	G	analog ground 1
DEC	7	I/O	decoupling node
n.c.	8	-	not connected
FSOUT	9	O	full-scale reference voltage output
FSIN	10	I	full-scale reference voltage input
n.c.	11	-	not connected
n.c.	12	-	not connected
n.c.	13	-	not connected
DEL1	14	I	complete conversion signal delay input 1
DEL0	15	I	complete conversion signal delay input 0
V_{CCD2}	16	P	digital supply voltage 2 (5.0 V)

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
DGND2	17	G	digital ground 2
CE_N	18	I	chip enable input (CMOS level; active LOW)
OTC	19	I	control input for two's complement output (active HIGH)
OGND	20	G	data output ground
V_{CCO}	21	P	data output supply voltage (3.3 V)
OGND	22	G	data output ground
V_{CCO}	23	P	data output supply voltage (3.3 V)
IR	24	O	in-range output
D11	25	O	data output bit 11 (Most Significant Bit (MSB))
D10	26	O	data output bit 10
D9	27	O	data output bit 9
D8	28	O	data output bit 8
D7	29	O	data output bit 7
D6	30	O	data output bit 6
D5	31	O	data output bit 5
D4	32	O	data output bit 4
D3	33	O	data output bit 3
D2	34	O	data output bit 2
D1	35	O	data output bit 1
D0	36	O	data output bit 0 (Least Significant Bit (LSB))
CCS	37	O	complete conversion signal output
DGND1	38	G	digital ground 1
CLKN	39	I	complementary clock input
CLK	40	I	clock input
V_{CCD1}	41	P	digital supply voltage 1 (5.0 V)
DGND1	42	G	digital ground 1
AGND2	43	G	analog ground 2
V_{CCA2}	44	P	analog supply voltage 2 (5.0 V)
V_{CCA1}	45	P	analog supply voltage 1 (5.0 V)
AGND1	46	G	analog ground 1
V_{CCA1}	47	P	analog supply voltage 1 (5.0 V)
AGND1	48	G	analog ground 1
DGND	exposed die pad	G	digital ground

[1] P: power supply; G: ground; I: input; O: output.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage		[1]	−0.5	+7.0	V
V_{CCD}	digital supply voltage		[1]	−0.5	+7.0	V
V_{CCO}	output supply voltage		[2]	−0.5	+5.0	V
ΔV_{CC}	supply voltage difference	$V_{CCA} - V_{CCD}$		−1.0	+1.0	V
		$V_{CCD} - V_{CCO}$		−1.0	+4.0	V
		$V_{CCA} - V_{CCO}$		−1.0	+4.0	V
$V_{i(IN)}$	input voltage on pin IN	referenced to AGND		0	V_{CCA} + 1	V
$V_{i(INN)}$	input voltage on pin INN	referenced to AGND		0	V_{CCA} + 1	V
$V_{i(CLK)}$	input voltage on pin CLK	referenced to DGND		0	V_{CCD} + 1	V
$V_{i(CLKN)}$	input voltage on pin CLKN	referenced to DGND		0	V_{CCD} + 1	V
I_O	output current			-	10	mA
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
T_j	junction temperature			-	150	°C

[1] The supply voltages V_{CCA} and V_{CCD} may have any value between −0.5 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

[2] The supply voltage V_{CCO} may have any value between −0.5 V and +5.0 V provided that the supply voltage differences ΔV_{CC} are respected.

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	36.2	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	14.3	K/W

[1] In compliance with JEDEC test board, in free air.

9. Characteristics

Table 5. Characteristics

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; V_{CCO} = 2.7 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = −0.5 dBFS; $V_{ref(fs)} = V_{CCA} - 1.87$ V; $V_{I(cm)} = V_{CCA} - 1.95$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V, V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{CCA}	analog supply voltage			4.75	5.0	5.25	V
V_{CCD}	digital supply voltage			4.75	5.0	5.25	V
V_{CCO}	output supply voltage			2.7	3.3	3.6	V
I_{CCA}	analog supply current			-	120	135	mA
I_{CCD}	digital supply current			-	50	65	mA
I_{CCO}	output supply current	f_{clk} = 80 MHz; f_i = 93 MHz		-	10	15	mA
P_{tot}	total power dissipation	f_{clk} = 80 MHz; DC input		-	840	990	mW
Clock inputs: pins CLK and CLKN[1]							
V_{IL}	LOW-level input voltage	referenced to DGND; V_{CCD} = 5 V					
		Positive Emitter-Coupled Logic (PECL) mode		3.19	-	3.52	V
		Transistor-Transistor Logic (TTL) mode		DGND	-	0.8	V
V_{IH}	HIGH-level input voltage	referenced to DGND; V_{CCD} = 5 V					
		PECL mode		3.83	-	4.12	V
		TTL mode		2.0	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} or V_{CLKN} = 3.52 V	[2]	-	-	28	µA
		V_{CLK} or V_{CLKN} = 0.80 V		1	-	-	nA
I_{IH}	HIGH-level input current	V_{CLK} or V_{CLKN} = 3.83 V		-	-	30	µA
		V_{CLK} or V_{CLKN} = 2.00 V		2	-	-	nA
$V_{i(clk)dif}$	differential clock input voltage	$V_{CLK} - V_{CLKN}$; AC mode; DC voltage level is 2.5 V		1.3	1.5	1.7	V
R_i	input resistance	f_{clk} = 80 MHz	[2]	-	6.3	-	kΩ
C_i	input capacitance	f_{clk} = 80 MHz	[2]	-	1.1	-	fF
Analog inputs: pins IN and INN							
I_{IL}	LOW-level input current	$V_{ref(fs)} = V_{CCA} - 1.75$ V		-	5	-	µA
I_{IH}	HIGH-level input current	$V_{ref(fs)} = V_{CCA} - 1.75$ V		-	5	-	µA
R_i	input resistance		[2]	6.3	-	-	MΩ
C_i	input capacitance		[2]	-	-	700	fF
$V_{I(cm)}$	common-mode input voltage	$V_{i(IN)} = V_{i(INN)}$; output code = 2047		$V_{CCA} - 2$	$V_{CCA} - 1.8$	$V_{CCA} - 1.6$	V
Digital inputs: pins OTC and CE_N							
V_{IL}	LOW-level input voltage			DGND	-	$0.3 \times V_{CCD}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{CCD}$	-	V_{CCD}	V

Table 5. Characteristics *...continued*

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; V_{CCO} = 2.7 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = −0.5 dBFS; $V_{ref(fs)} = V_{CCA} - 1.87$ V; $V_{I(cm)} = V_{CCA} - 1.95$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V, V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	-	1	-	µA
I_{IH}	HIGH-level input current	V_{IH} = 2.0 V	-	1	-	µA
Digital inputs: pins DEL0 and DEL1						
V_{IL}	LOW-level input voltage		DGND	-	$0.3 \times V_{CCD}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{CCD}$	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	-	8	-	µA
I_{IH}	HIGH-level input current	V_{IH} = 2.0 V	-	20	-	µA
Voltage controlled regulator output: pin CMADC						
$V_{O(cm)}$	common-mode output voltage	I_L = 0 mA	-	$V_{CCA} - 1.88$	-	V
		I_L = 2 mA	-	$V_{CCA} - 1.95$	-	V
Reference voltage input: pin FSIN[3]						
$V_{ref(fs)}$	full-scale reference voltage		-	$V_{CCA} - 1.80$	-	V
$I_{ref(fs)}$	full-scale reference current		-	0.1	-	µA
$V_{i(a)(p-p)}$	peak-to-peak analog input voltage	see Figure 5; $V_i = V_{i(IN)} - V_{i(INN)}$; $V_{I(cm)} = V_{CCA} - 1.95$ V	-	1.85	-	V
Full-scale voltage controlled regulator output: pin FSOUT						
$V_{O(ref)}$	reference output voltage	$I_L = I_{ref(fs)}$	-	$V_{CCA} - 1.80$	-	V
		I_L = 2 mA	-	$V_{CCA} - 1.82$	-	V
Digital outputs: pins D11 to D0, IR and CCS						
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	DGND	-	DGND + 0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = −0.4 mA	$V_{CCO} - 0.5$	-	V_{CCO}	V
I_{OZ}	OFF-state output current	output level between 0.5 V and V_{CCO}	−0.1	0	+0.1	µA
Timing[4]						
$t_{d(s)}$	sampling delay time	C_L = 10 pF	-	0.1	0.24	ns
$t_{h(o)}$	output hold time	C_L = 10 pF	2.6	3.8	-	ns
$t_{d(o)}$	output delay time	C_L = 10 pF	-	4.7	7.8	ns
3-state output delay						
t_{dZH}	float to active HIGH delay time		-	3.6	-	ns
t_{dZL}	float to active LOW delay time		-	3.9	-	ns
t_{dHZ}	active HIGH to float delay time		-	9.2	-	ns
t_{dLZ}	active LOW to float delay time		-	7.2	-	ns

Table 5. Characteristics *…continued*

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; V_{CCO} = 2.7 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = −0.5 dBFS; $V_{ref(fs)} = V_{CCA} - 1.87$ V; $V_{I(cm)} = V_{CCA} - 1.95$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V, V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock timing inputs: pins CLK and CLKN							
δ	duty cycle	f_{clk} = 80 MHz; f_i = 175 MHz		45	-	55	%
$f_{clk(min)}$	minimum clock frequency			-	-	9.5	MHz
$f_{clk(max)}$	maximum clock frequency	δ = 45 % to 55 %		80	-	-	MHz
Timing complete conversion signal: pin CCS; see Figure 6							
$t_{d(CCS)}$	CCS delay time	C_L = 10 pF; DEL0 = HIGH; DEL1 = LOW		-	0.3	-	ns
		C_L = 10 pF; DEL0 = LOW; DEL1 = HIGH		-	1.3	-	ns
		C_L = 10 pF; DEL0 = HIGH; DEL1 = HIGH		-	2.3	-	ns
Analog signal processing (clock duty cycle 50 %)							
INL	integral non-linearity	f_{clk} = 20 MHz; f_i = 21.4 MHz		-	±2.0	-	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; f_i = 21.4 MHz; no missing code guaranteed		-	±0.6	-	LSB
E_{offset}	offset error	$V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.3 V; T_{amb} = 25 °C; output code = 2047		−4	+8	+24	mV
E_G	gain error	$V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.3 V; T_{amb} = 25 °C		-	2.5	-	%FS
B	bandwidth	f_{clk} = 80 MHz; −3 dB; full-scale input	[5]	320	375	-	MHz
α_{2H}	second harmonic level	f_i = 21.4 MHz		-	−79	-	dBc
		f_i = 93 MHz		-	−78	-	dBc
		f_i = 175 MHz		-	−74	-	dBc
α_{3H}	third harmonic level	f_i = 21.4 MHz		-	−84	-	dBc
		f_i = 93 MHz		-	−80	-	dBc
		f_i = 175 MHz		-	−76	-	dBc
THD	total harmonic distortion	f_i = 21.4 MHz	[6]	-	−75	-	dBc
		f_i = 93 MHz		-	−73	-	dBc
		f_i = 175 MHz		-	−68	-	dBc
$N_{th(RMS)}$	RMS thermal noise	$V_{i(IN)} = V_{i(INN)}$; f_{clk} = 80 MHz		-	0.45	-	LSB

Table 5. Characteristics *…continued*

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; V_{CCO} = 2.7 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = −0.5 dBFS; $V_{ref(fs)} = V_{CCA} - 1.87$ V; $V_{I(cm)} = V_{CCA} - 1.95$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V, V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
S/N	signal-to-noise ratio	f_i = 21.4 MHz	[7]	-	67.4	-	dBc
		f_i = 93 MHz		63	67.2	-	dBc
		f_i = 175 MHz		-	66.5	-	dBc
SFDR	spurious free dynamic range	f_i = 21.4 MHz		-	76	-	dBc
		f_i = 93 MHz		68	78	-	dBc
		f_i = 175 MHz		-	74	-	dBc
ACPR	adjacent channel power ratio	f_i = 93 MHz; 5 MHz channel spacing; B = 3.84 MHz		-	70	-	dB
IMD2	second-order intermodulation distortion	f_i 1 = 21 MHz; f_i 2 = 22 MHz	[8]	-	−89	-	dBFS
		f_i 1 = 91.5 MHz; f_i 2 = 94.5 MHz		-	−86	-	dBFS
		f_i 1 = 174 MHz; f_i 2 = 176 MHz		-	−83	-	dBFS
IMD3	third-order intermodulation distortion	f_i 1 = 21 MHz; f_i 2 = 22 MHz	[8]	-	−88	-	dBFS
		f_i 1 = 91.5 MHz; f_i 2 = 93.5 MHz		-	−82	-	dBFS
		f_i 1 = 174 MHz; f_i 2 = 176 MHz		-	−83	-	dBFS

[1] The circuit has two clock inputs: CLK and CLKN. There are 5 modes of operation:

a) PECL mode 1: (DC levels vary 1:1 with V_{CCD}) CLK and CLKN inputs are at differential PECL levels.

b) PECL mode 2: (DC levels vary 1:1 with V_{CCD}) CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on CLKN decoupled to GND via a 100 nF capacitor.

c) PECL mode 3: (DC levels vary 1:1 with V_{CCD}) CLKN input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.

d) Differential AC driving mode 4: When driving the CLK input directly and with any AC signal of minimum 1 V (p-p) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal. When driving the CLKN input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the CLKN or CLK input to DGND via a 100 nF capacitor.

e) TTL mode 5: CLK input is at TTL level and sampling is taken on the falling edge of the clock input signal. In that case CLKN pin has to be connected to the ground.

[2] Guaranteed by design.

[3] The ADC input range can be adjusted with an external reference connected to pin FSIN. This voltage has to be referenced to V_{CCA}.

[4] Output data acquisition: the output data is available after the maximum delay of $t_{d(o)}$.

[5] The −3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.

[6] The total harmonic distortion is obtained with the addition of the first five harmonics.

[7] The signal-to-noise ratio takes into account all harmonics above five and noise up to Nyquist frequency.

[8] Intermodulation measured relative to either tone with analog input frequencies f_i 1 and f_i 2. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (−6 dB below full-scale for each input signal). IMD3 is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product; IMD2 is the ratio of the RMS value of either input tone to the RMS value of the worst case second order intermodulation product.

10. Additional information relating to Table 5

Table 6. Output coding with differential inputs

$V_{i(IN)} - V_{i(INN)}$ = 1.9 V; $V_{ref(fs)} = V_{CCA1} - 1.87$ V; typical values to AGND.

Code	$V_{i(IN)}$ (V)	$V_{i(INN)}$ (V)	IR	Binary outputs (D11 to D0)	Two's complement outputs (D11 to D0)
Underflow	< 2.675	> 3.625	0	0000 0000 0000	1000 0000 0000
0	2.675	3.625	1	0000 0000 0000	1000 0000 0000
1	-	-	1	0000 0000 0001	1000 0000 0001
↓	↓	↓	↓	↓	↓
2047	3.15	3.15	1	0111 1111 1111	1111 1111 1111
↓	↓	↓	↓	↓	↓
4094	-	-	1	1111 1111 1110	0111 1111 1110
4095	3.625	2.675	1	1111 1111 1111	0111 1111 1111
Overflow	> 3.625	< 2.675	0	1111 1111 1111	0111 1111 1111

Table 7. Mode selection

Two's complement output (OTC)	Chip enable input (CE_N)	Data output (D0 to D11; IR)
0	0	binary; active
1	0	two's complement; active
X[1]	1	high-impedance

[1] X = don't care.

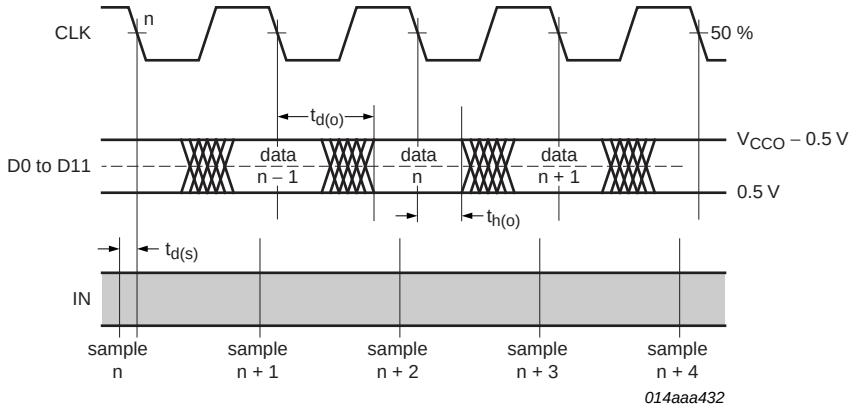
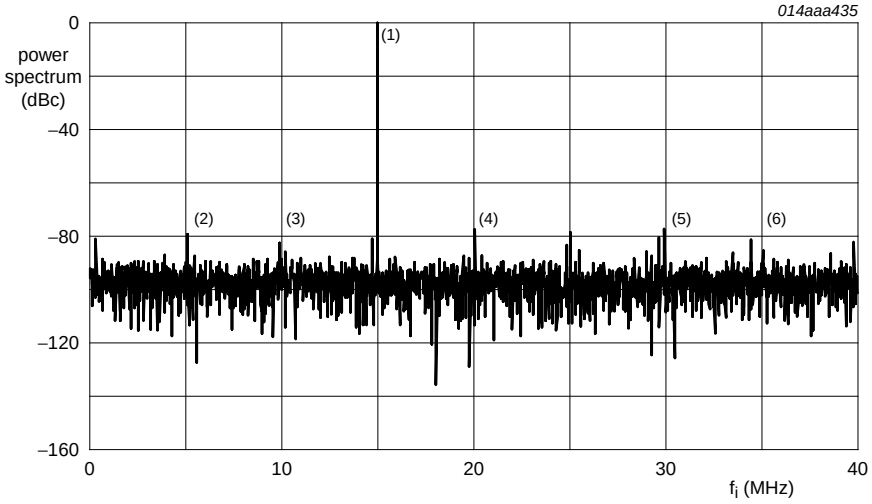


Fig 3. Output timing diagram



(1) f_i 1H = 15 MHz; 0 dBc
(2) f_i 2H = 5.1 MHz; −79.6 dBc
(3) f_i 3H = 9.88 MHz; −82.1 dBc
(4) f_i 4H = 20.1 MHz; −80.6 dBc
(5) f_i 5H = 30 MHz; −74.7 dBc
(6) f_i 6H = 35.1 MHz; −93.9 dBc
THD (5H): −72.2 dBc
SFDR: 74.7 dBc

Fig 4. Single tone; f_i = 175 MHz; f_{CLK} = 80 MHz

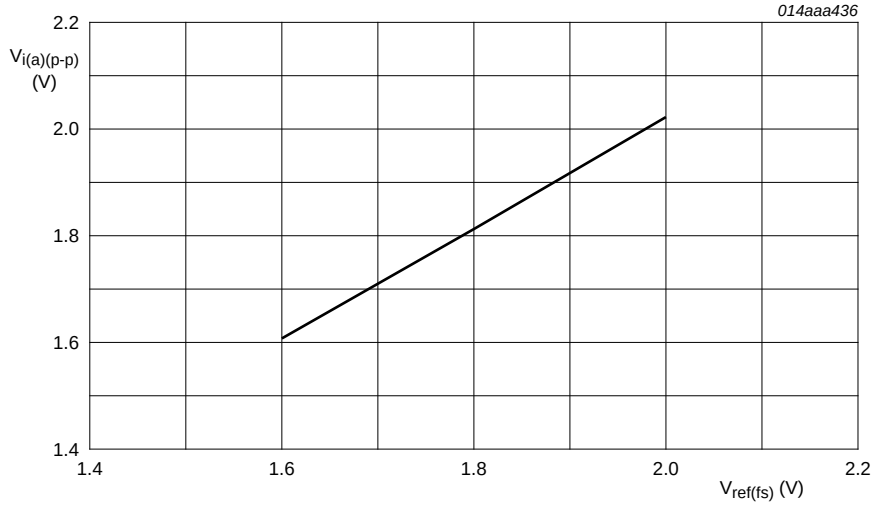


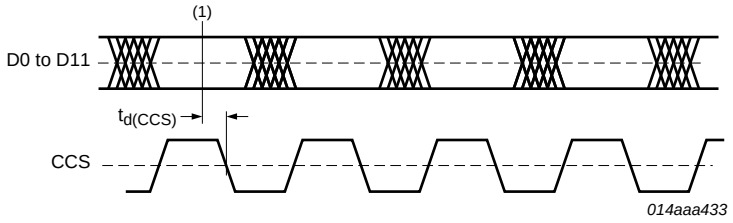
Fig 5. ADC full-scale; $V_{i(a)(p-p)}$ as a function of $V_{ref(fs)}$

The ADC1207S080 allows modifying the ADC full-scale. This could be done with FSIN (full-scale input) according to Figure 5.

The ADC1207S080 generates an adjustable clock output called Complete Conversion Signal (CCS), which can be used to control the acquisition of converted output data by the digital circuit connected to the ADC1207S080 output data bus. Two logic inputs, DEL0 and DEL1 pins, allow adjusting the delay of the edge of the CCS signal to achieve an optimal position in the stable, usable zone of the data.

Table 8. Complete conversion signal selection

DEL1	DEL0	CCS output
0	0	high-impedance
0	1	active, typical delay 0.3 ns
1	0	active, typical delay 1.3 ns
1	1	active, typical delay 2.3 ns



(1) $t_{d(CSS)}$ is referenced to the middle of the active data.

Fig 6. Complete conversion signal timing diagram

11. Definitions

11.1 Static parameters

11.1.1 Integral Non-Linearity (INL)

It is defined as the deviation of the transfer function from a best fit straight line (linear regression computation). The INL of the code i is obtained from the equation:

$$INL(i) = \frac{V_i(i) - V_i(ideal)}{S}$$

where: S corresponds to the slope of the ideal straight line (code width); i corresponds to the code value; V_i is the input voltage.

11.1.2 Differential Non-Linearity (DNL)

It is the deviation in code width from the value of 1 LSB.

$$DNL(i) = \frac{V_i(i+1) - V_i(i)}{S}$$

where: V_i is the input voltage; i from 0 to $(2^n - 2)$.

11.2 Dynamic parameters

Figure 7 shows the spectrum of a single tone full-scale input sine wave with frequency f, conforming to coherent sampling (f/f_s = M/N, with M number of cycles and N number of samples, M and N being relatively prime), and digitized by the ADC under test.

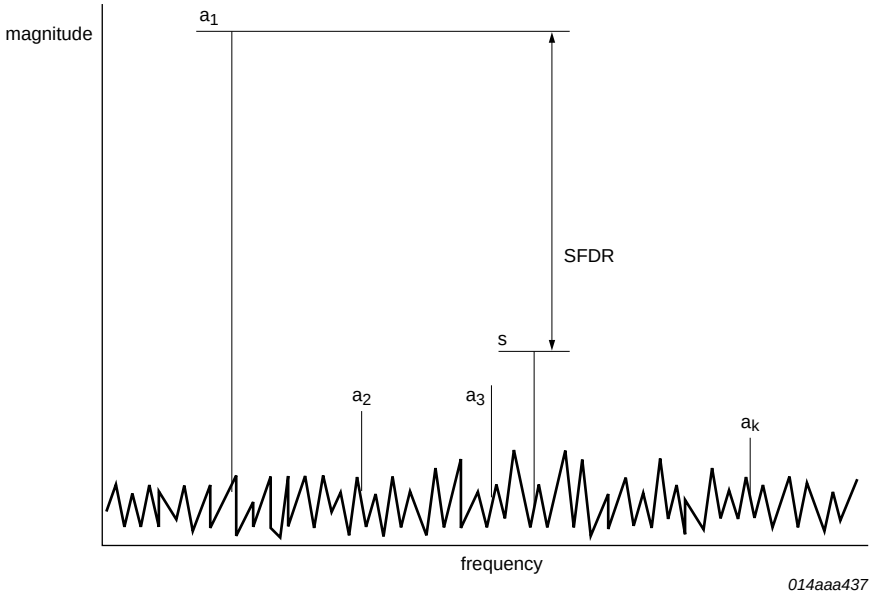


Fig 7. Single tone spectrum of full-scale input sine wave with frequency f_t

Remark: In the following equations, P_{noise} is the power of the terms which include the effects of random noise, non-linearities, sampling time errors, and 'quantization noise'.

11.2.1 SIgnal-to-Noise And Distortion (SINAD)

The ratio of the output signal power to the noise plus distortion power for a given sample rate and input frequency, excluding the DC component:

$$SINAD[dB] = 10log_{10}\left(\frac{P_{signal}}{P_{noise+distortion}}\right)$$

11.2.2 Effective Number Of Bits (ENOB)

It is derived from SINAD and gives the theoretical resolution an ideal ADC would require to obtain the same SINAD measured on the real ADC. A good approximation gives:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

11.2.3 Total Harmonic Distortion (THD)

The ratio of the power of the harmonics to the power of the fundamental. For k − 1 harmonics the THD is:

$$THD[dB] = 10log_{10}\left(\frac{P_{harmonics}}{P_{signal}}\right)$$

where:

$$P_{harmonics} = \alpha_2^2 + \alpha_3^2 + \ldots + \alpha_k^2$$

$$P_{signal} = \alpha_1^2$$

The value of k is usually 6 (i.e. calculation of THD is done on the first 5 harmonics).

11.2.4 Signal-to-Noise ratio (S/N)

The ratio of the output signal power to the noise power, excluding the harmonics and the DC component is:

$$S/N[dB] = 10log_{10}\left(\frac{P_{signal}}{P_{noise}}\right)$$

11.2.5 Spurious Free Dynamic Range (SFDR)

The number SFDR specifies available signal range as the spectral distance between the amplitude of the fundamental and the amplitude of the largest spurious harmonic and non-harmonic, excluding DC component:

$$SFDR[dB] = 20log_{10}\left(\frac{\alpha_1}{max(S)}\right)$$

11.2.6 IMD2 (IMD3)

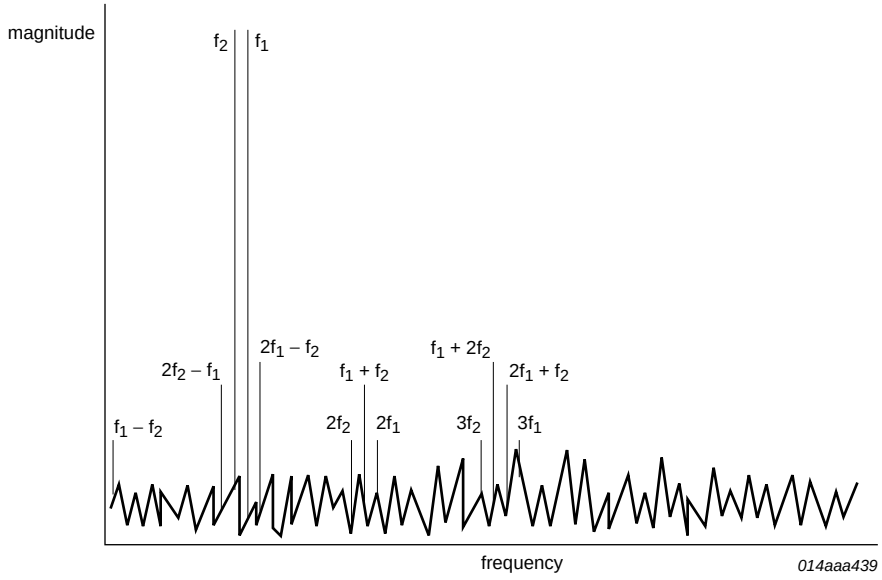


Fig 8. Spectral of dual tone input sine wave with frequency

From a dual tone input sinusoid (f_{t1} and f_{t2}, these frequencies being chosen according to the coherence criterion), the intermodulation distortion products IMD2 and IMD3 (respectively, 2nd and 3rd order components) are defined, as follows.

The ratio of the RMS value of either tone to the RMS value of the worst second (third) order intermodulation product.

The total InterModulation Distortion (IMD) is given by:

$$IMD[dB] = 10log_{10}\left(\frac{P_{intermod}}{P_{signal}}\right)$$

where:

$$P_{intermod} = \alpha^2_{im(f_{t1}-f_{t2})} - \alpha^2_{im(f_{t1}+f_{t2})} + \alpha^2_{im(f_{t1}-2f_{t2})} + \alpha^2_{im(f_{t1}+2f_{t2})} + \ldots$$
$$\ldots + \alpha^2_{im(2f_{t1}-f_{t2})} + \alpha^2_{im(2f_{t1}+f_{t2})}$$

with $\alpha^2_{im(f_{t1})}$ corresponding to the power in the intermodulation component at frequency f_t.

$$P_{signal} = \alpha^2_{f_{t1}} + \alpha^2_{f_{t2}}$$

12. Application information

12.1 ADC1207S080 in 3G radio receivers

The ADC1207S080 has been proven in many 3G radio receivers with various operating conditions regarding Input Frequency (IF), signal IF bandwidth and sampling frequency. The ADC1207S080 is provided with a maximum analog input signal frequency of 400 MHz. It allows a significant cost-down of the RF front-end, from two mixers to only one, even in multi-carriers architecture.

Table 9 describes some possible applications with the ADC1207S080 in high IF sampling mode.

Table 9. Examples of possible f_i, f_{clk}, IF BW combinations supported

f_i (MHz)	f_{clk} (MHz)	IF BW (MHz) [1]	SNR (dB)	SFDR (dBc)
350	80	5.00	65	71
243.95	9.60	0.25	71	80
96	76.80	1.60	72	76
96	76.80	4.80	71	77
96	76.80	20.00	68	76
80	61.44	10.00	70	85
78.4	44.80	3.50	71	76
70	40.00	1.25	72	79

[1] IF bandwidth corresponds to the observed area on the ADC output spectrum.

For a dual carrier Wideband-Code-Division-Multiple-Access (W-CDMA) receiver, the most important parameters are sensitivity and Adjacent Channel Selectivity (ACS). The sensitivity is defined as the lowest detectable signal level. In W-CDMA, it can be far below the noise floor. This difference, between the sensitivity and the noise floor, is defined by the Sensitivity-to-Noise Ratio (SENR). Its value is negative due to the gain processing. The Adjacent Channel Power Ratio (ACPR) is the difference between the full-scale −3 dB peak and the noise floor. It represents the ratio of the adjacent-channel power and the average power level of the channel. The ACS is defined by the sum of SENR and ACPR.

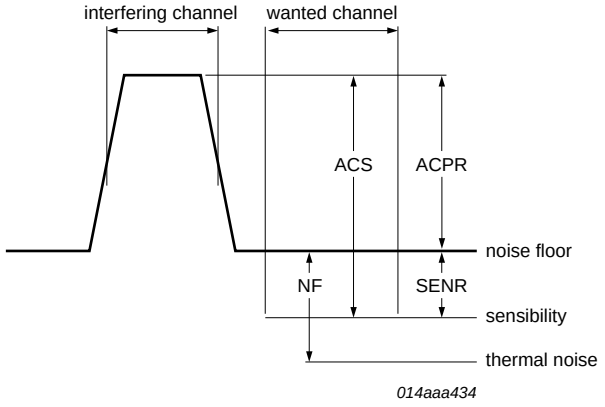


Fig 9. Adjacent channel sensitivity and ADC sensibility

12.2 Application diagram

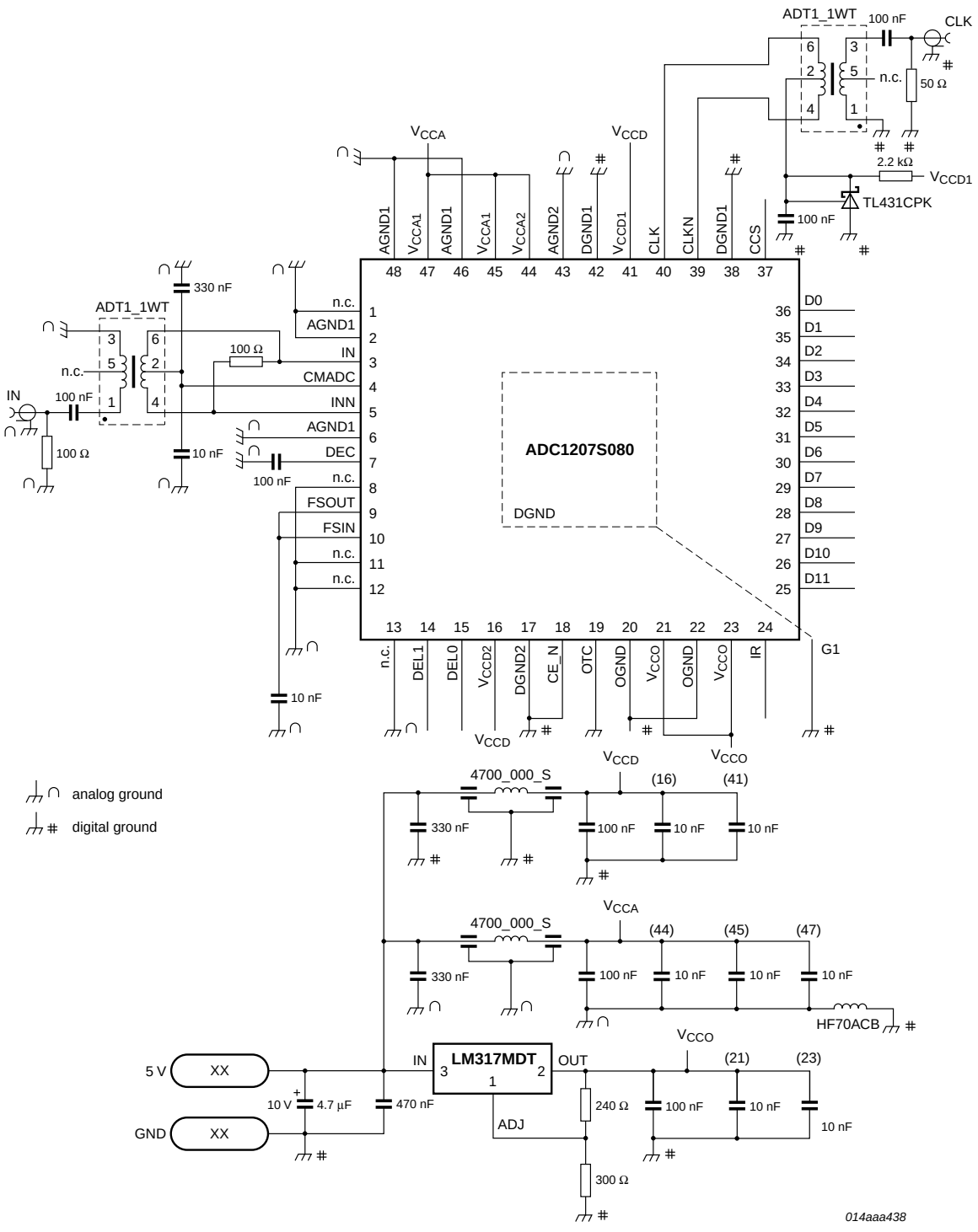
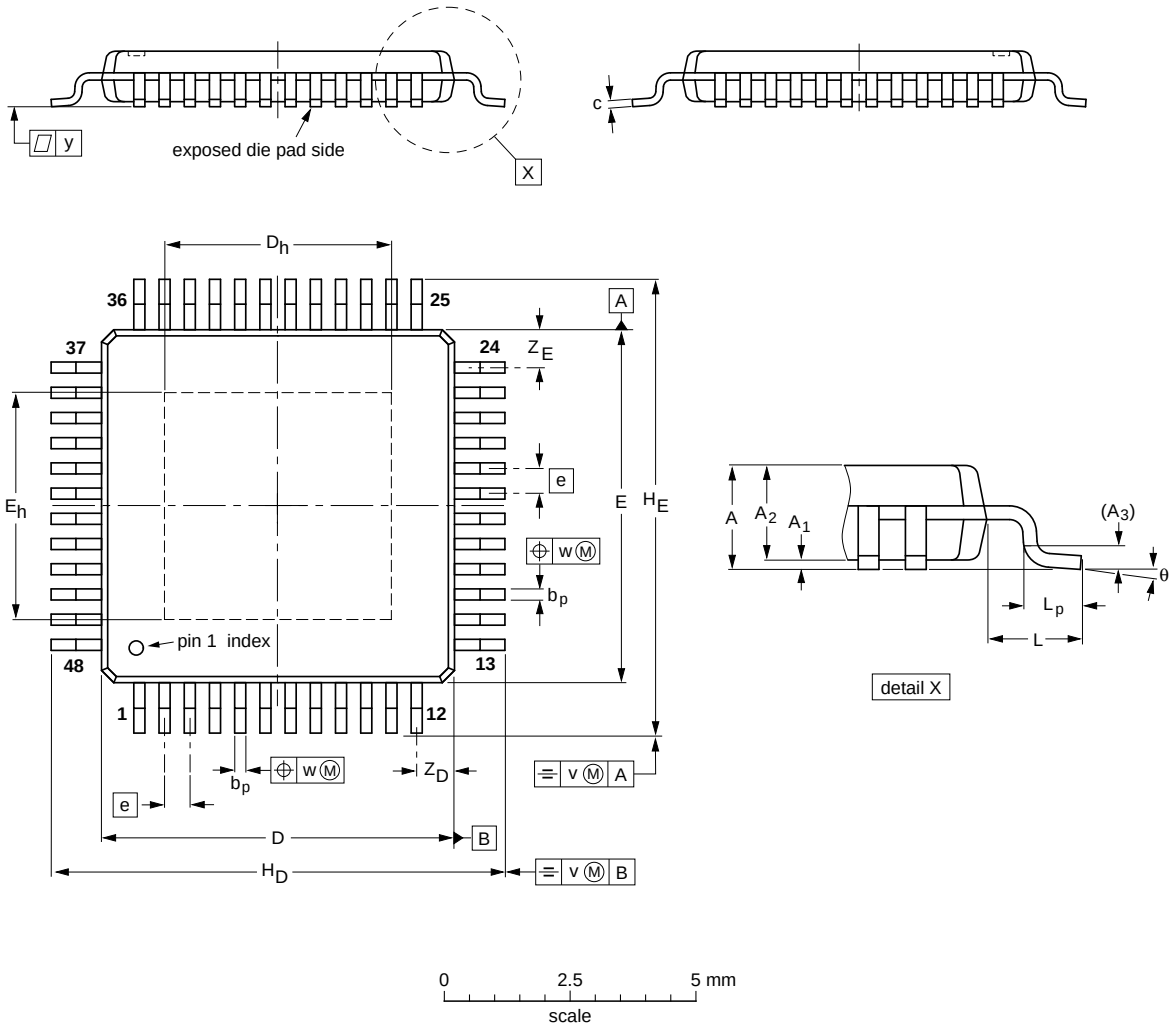


Fig 10. Application diagram

13. Package outline

HTQFP48: plastic thermal enhanced thin quad flat package; 48 leads; body 7 x 7 x 1 mm; exposed die pad

SOT545-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	7.1 6.9	4.6 4.4	7.1 6.9	4.6 4.4	0.5	9.1 8.9	9.1 8.9	1	0.75 0.45	0.2	0.08	0.08	0.9 0.6	0.9 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT545-2		MS-026				~~03-04-07~~ 04-01-29

Fig 11. Package outline SOT545-2 (HTQFP48)

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1207S080_3	20120702	Product data sheet	-	ADC1207S080_2
ADC1207S080_2	20080807	Product data sheet	-	ADC1207S080_1
Modifications:	• Corrections made to version number in Table 1. • Corrections made to several entries in Table 5. • Corrections made to alignment in Figure 10. • Corrections made to Figure 11.			
ADC1207S080_1	20080611	Product data sheet	-	-

15. Contact information

For more information or sales office addresses, please visit: http://www.idt.com

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