Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTER (3-STATE)

IDT54/74FCT16374T/AT/CT/ET
IDT54/74FCT162374T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16374T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162374T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

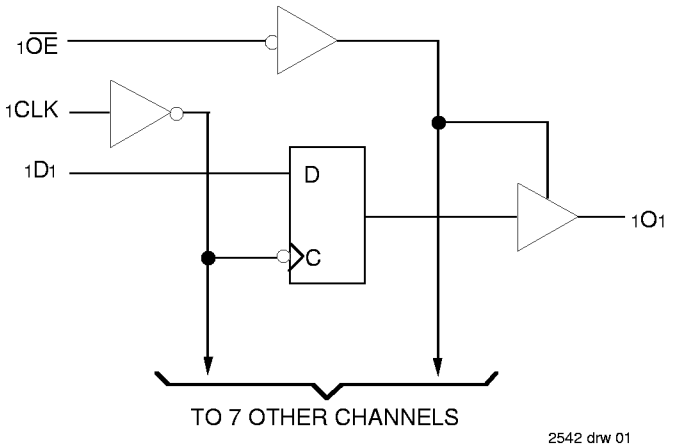
DESCRIPTION:

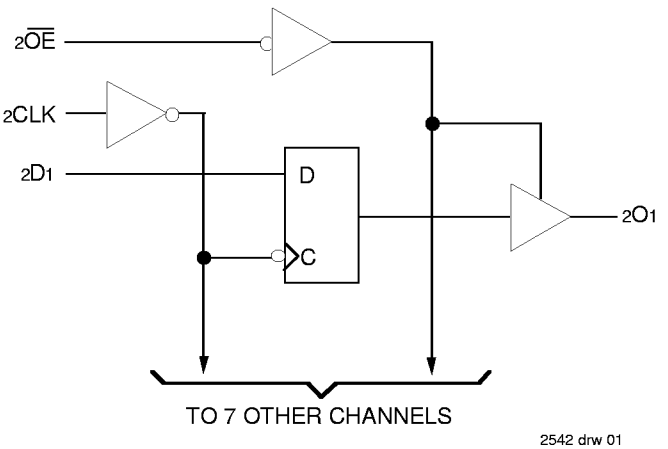
The FCT16374T/AT/CT/ET and FCT162374T/AT/CT/ET 16-bit edge-triggered D-type registers are built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable ($x\overline{OE}$) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16374T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

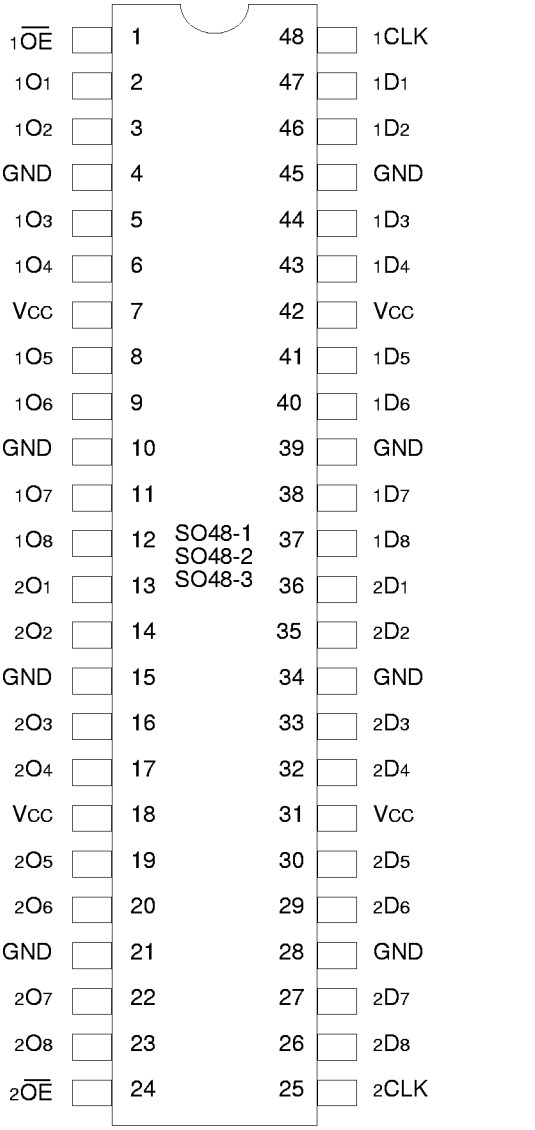
The FCT162374T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times– reducing the need for external series terminating resistors. The FCT162374T/AT/CT/ET are plug-in replacements for the FCT16374T/AT/CT/ET and ABT16374 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATIONS



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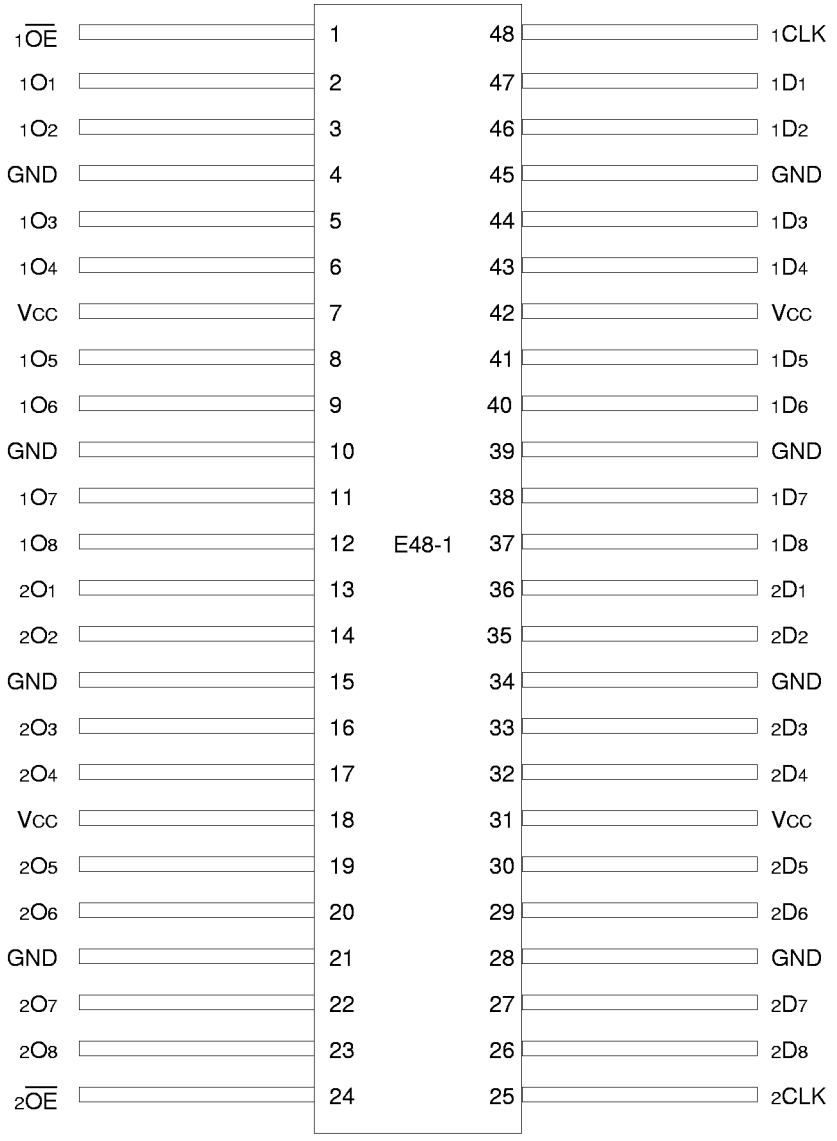
SSOP/ TSSOP/TVSOP TOP VIEW



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CERPACK TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xOx	3-State Outputs.
$x\overline{OE}$	3-State Output Enable Input (Active LOW)

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FUNCTION TABLE(1)

Function	Inputs			Outputs
	xDx	xCLK	$x\overline{OE}$	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE: 2542 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES: 2542 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2542 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT16374T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT162374T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.1	3.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	7.5	19.0[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16374T/162374T				FCT16374AT/162374AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xOx	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition[1]	FCT16374CT/162374CT				FCT16374ET/162374ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xOx	C_L = 50pF R_L = 500Ω	2.0	5.2	2.0	6.2	1.5	3.7	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.5	1.5	6.2	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.0	1.5	5.7	1.5	3.6	—	—	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	0.0	—	—	—	ns
t_W	xCLK Pulse Width HIGH or LOW		5.0	—	6.0	—	3.0[4]	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

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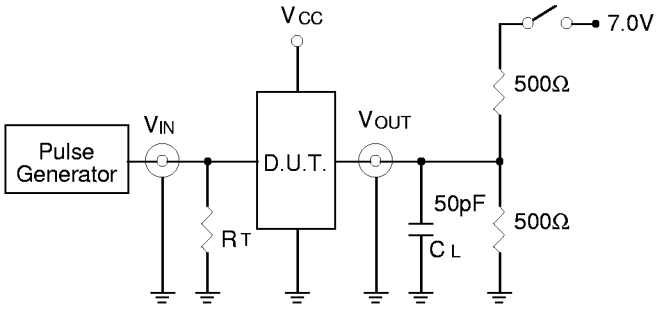
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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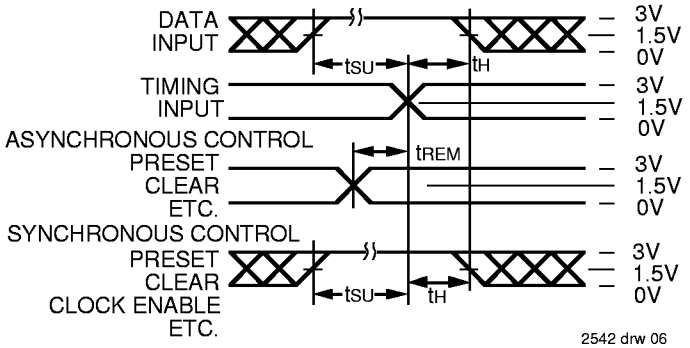
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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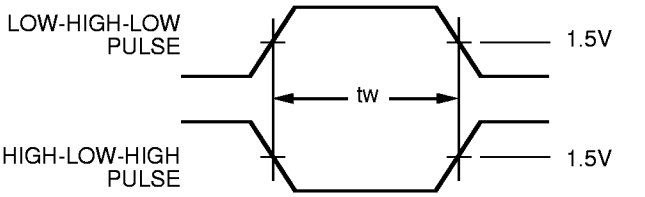
PULSE WIDTH



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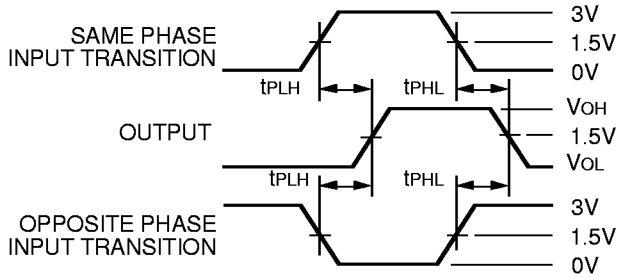
PROPAGATION DELAY



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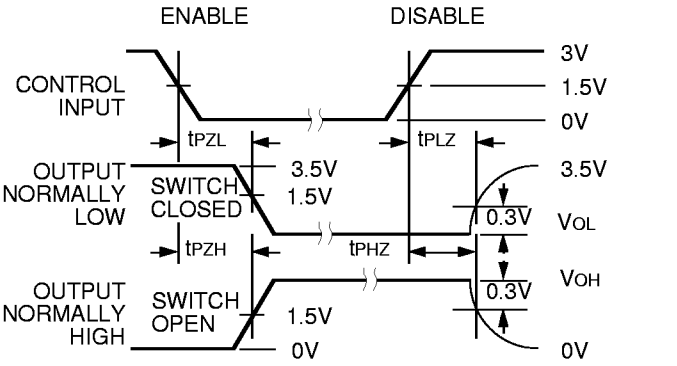
ENABLE AND DISABLE TIMES



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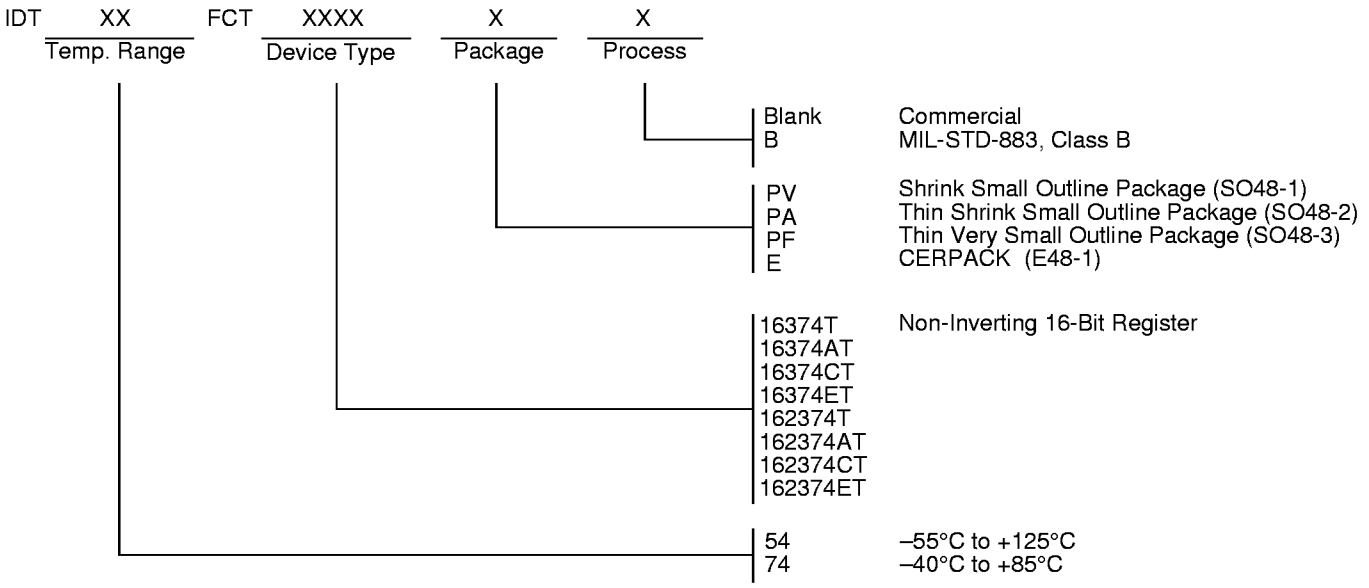
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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