L6910G

ADJUSTABLE STEP DOWN CONTROLLER WITH SYNCHRONOUS RECTIFICATION

1 FEATURES

- OPERATING SUPPLY VOLTAGE FROM 5V TO 12V BUSES
- UP TO 1.3A GATE CURRENT CAPABILITY
- ADJUSTABLE OUTPUT VOLTAGE
- N-INVERTING E/A INPUT AVAILABLE
- 0.9V ±1.5% VOLTAGE REFERENCE
- VOLTAGE MODE PWM CONTROL
- VERY FAST LOAD TRANSIENT RESPONSE
- 0% TO 100% DUTY CYCLE
- POWER GOOD OUTPUT
- OVERVOLTAGE PROTECTION
- HICCUP OVERCURRENT PROTECTION
- 200kHz INTERNAL OSCILLATOR
- OSCILLATOR EXTERNALLY ADJUSTABLE FROM 50kHz TO 1MHz
- SOFT START AND INHIBIT
- PACKAGE: SO-16

2 APPLICATIONS

- SUPPLY FOR MEMORIES AND TERMINATIONS
- COMPUTER ADD-ON CARDS
- LOW VOLTAGE DISTRIBUTED DC-DC
- MAG-AMP REPLACEMENT

3 DESCRIPTION

The device is a pwm controller for high performance dc-dc conversion from 3.3V, 5V and 12V buses.

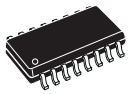
The output voltage is adjustable down to 0.9V; higher voltages can be obtained with an external voltage divider.

High peak current gate drivers provide for fast switching to the external power section, and the output current can be in excess of 20A.

The device assures protections against load overcurrent and overvoltage.

An internal crowbar is also provided turning on the low side mosfet as long as the over-voltage is detected. In case of over-current detection, the soft start capacitor is discharged and the system works in HICCUP mode.

Figure 1. Packages



SO-16 (Narrow)

Table 1. Order Codes

Part Number	Package
L6910G	SO-16
L6910GTR	SO-16 in Tape & Reel

Figure 2. Block Diagram

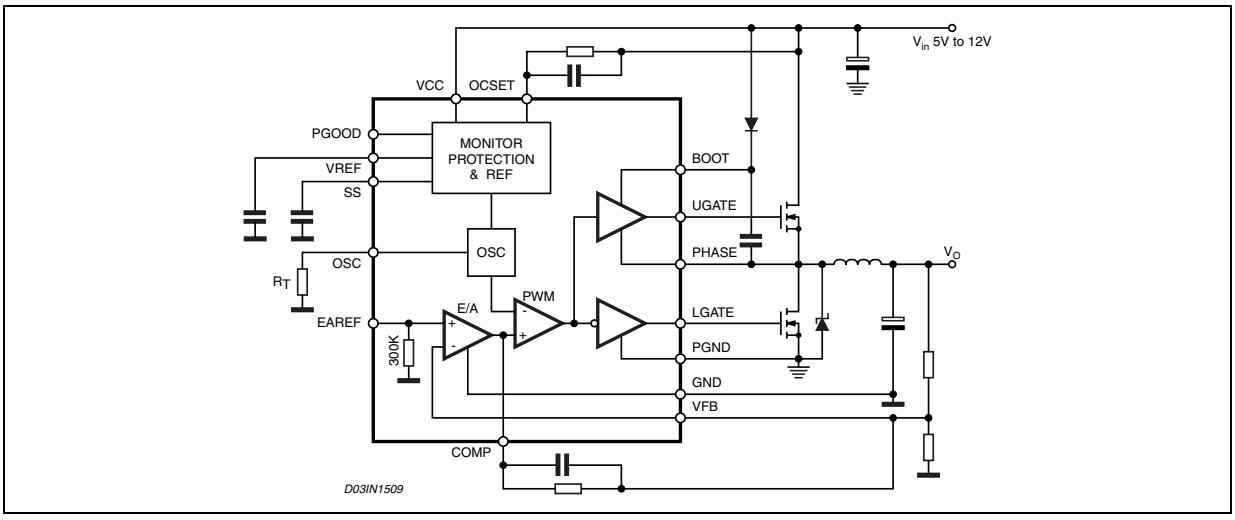


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Vcc	Vcc to GND, PGND	15	V
V_{BOOT}-V_{PHASE}	Boot Voltage	15	V
V_{HGATE}-V_{PHASE}		15	V
	OCSET, LGATE, PHASE	-0.3 to Vcc+0.3	V
	SS, FB, PGOOD, VREF, EAREF, RT	7	V
	COMP	6.5	V
T_j	Junction Temperature Range	-40 to 150	°C
T_{stg}	Storage temperature range	-40 to 150	°C
P_{tot}	Maximum power dissipation at Tamb = 25°C	1	W
OCSET PIN	Maximum Withstanding Voltage Range Test Condition: CDF-AEC-Q100-002"Human Body Model" Acceptance Criteria: "Normal Performance"	±1000	V
OTHER PINS		±2000	V

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	120	°C/W

(*) Device soldered on 1 S2P PC board

Figure 3. Pins Connection (Top view)

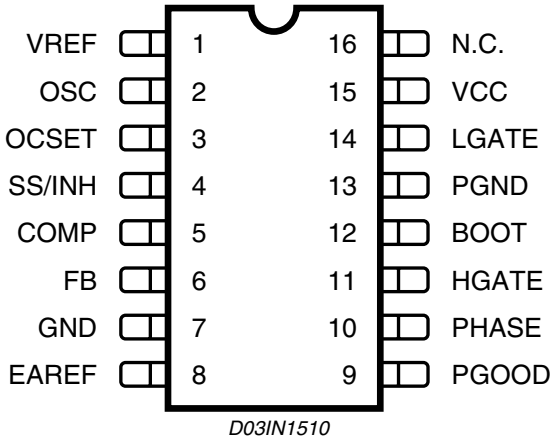


Table 4. Pins Function

Pin	Name	Description
1	VREF	Internal 0.9V ±1.5% reference is available for external regulators or for the internal error amplifier (connecting this pin to EAREF) if external reference is not available. A minimum 1nF capacitor is required. If the pin is forced to a voltage lower than 70%, the device enters the hiccup mode.
2	OSC	Oscillator switching frequency pin. Connecting an external resistor (R_T) from this pin to GND, the external frequency is increased according to the equation: $f_{OSC,RT} = 200KHz + \frac{4.94 \cdot 10^6}{R_T(K\Omega)}$ Connecting a resistor (R_T) from this pin to Vcc (12V), the switching frequency is reduced according to the equation: $f_{OSC,RT} = 200KHz - \frac{4.306 \cdot 10^7}{R_T(K\Omega)}$ If the pin is not connected, the switching frequency is 200KHz. The voltage at this pin is fixed at 1.23V. Forcing a 50µA current into this pin, the built in oscillator stops to switch. In Over Voltage condition this pin goes over 3V until that conditon is removed.
3	OCSET	A resistor connected from this pin and the upper Mos Drain sets the current limit protection. The internal 200µA current generator sinks a constant current through the external resistor. The Over-Current threshold is due to the following equation: $I_P = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DSon}}$
4	SS/INH	The soft start time is programmed connecting an external capacitor from this pin and GND. The internal current generator forces through the capacitor 10µA. This pin can be used to disable the device forcing a voltage lower than 0.4V
5	COMP	This pin is connected to the error amplifier output and is used to compensate the voltage control feedback loop.
6	FB	This pin is connected to the error amplifier inverting input and is used to compensate the voltage control feedback loop. Connected to the output resistor divider, if used, or directly to Vout, it manages also over-voltage conditions and the PGOOD signal
7	GND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
8	EAREF	Error amplifier non-inverting input. Connect to this pin an external reference (from 0.9V to 3V) for the PWM regulation or short it to VREF pin to use the internal reference. If this pin goes under 650mV (typ), the device shuts down.
9	PGOOD	This pin is an open collector output and it is pulled low if the output voltage is not within the above specified thresholds. If not used it may be left floating.
10	PHASE	This pin is connected to the source of the upper mosfet and provides the return path for the high side driver. This pin monitors the drop across the upper mosfet for the current limit together with OCSET.
11	HGATE	High side gate driver output.
12	BOOT	Bootstrap capacitor pin. Through this pin is supplied the high side driver and the upper mosfet. Connect through a capacitor to the PHASE pin and through a diode to Vcc (cathode vs. boot). **VBOOT limited to VOCSET -10V(typ.) when all other pins are connected to GND.**
13	PGND	Power ground pin. This pin has to be connected closely to the low side mosfet source in order to reduce the noise injection into the device
14	LGATE	This pin is the lower mosfet gate driver output
15	VCC	Device supply voltage. The operative supply voltage ranges is from 5V to 12V. DO NOT CONNECT V_{IN} TO A VOLTAGE GREATER THAN V_{CC}.
16	N.C.	This pin is not internally bonded. It may be left floating or connected to GND.

Table 5. Electrical Characteristics (V_{cc} = 12V, T_J =25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{cc} SUPPLY CURRENT						
Icc	Vcc Supply current	OSC = open; SS to GND	4	7	9	mA
POWER-ON						
	Turn-On Vcc threshold	VOCSET = 4V	4.0	4.3	4.6	V
	Turn-Off Vcc threshold	VOCSET = 4V	3.8	4.1	4.4	V
	Rising V_{OCSET} threshold			1.24	1.4	V
	Turn On EAREF threshold	VOCSET = 4V		650	750	mV
SOFT START AND INHIBIT						
Iss	Soft start Current S.S. current in INH condition	SS = 2V SS = 0 to 0.4V	6	10 35	14 60	µA µA
OSCILLATOR						
f_{OSC}	Initial Accuracy	OSC = OPEN OSC = OPEN; T_j = 0° to 125°	180 170	200	220 230	KHz kHz
$f_{OSC,RT}$	Total Accuracy	16 KΩ < R_T to GND < 200 KΩ	-15		15	%
ΔVosc	Ramp amplitude			1.9		V
REFERENCE						
V_{OUT}	Output Voltage Accuracy	V_{OUT} = V_{FB}; V_{EAREF} = V_{REF}	0.886	0.900	0.913	V
V_{REF}	Reference Voltage	C_{REF} = 1nF; I_{REF} = 0 to 100µA	0.886	0.900	0.913	V
V_{REF}	Reference Voltage	C_{REF} = 1nF; T_J = 0 to 125°C	-2		+2	%
ERROR AMPLIFIER						
I_{EAREF}	N.I. bias current	V_{EAREF} = 3V		10		µA
	EAREF Input Resistance	Vs. GND		300		kΩ
I_{FB}	I.I. bias current	V_{FB} = 0V to 3V		0.01	0.5	µA
V_{CM}	Common Mode Voltage		0.8		3	V
V_{COMP}	Output Voltage		0.5		4	V
G_V	Open Loop Voltage Gain		70	85		dB
GBWP	Gain-Bandwidth Product			10		MHz
SR	Slew-Rate	COMP = 10pF		10		V/µs
GATE DRIVERS						
I_{HGATE}	High Side Source Current	V_{BOOT} - V_{PHASE} = 12V V_{HGATE} - V_{PHASE} = 6V	1	1.3		A
R_{HGATE}	High Side Sink Resistance	V_{BOOT} - V_{PHASE} = 12V		2	4	Ω
I_{LGATE}	Low Side Source Current	Vcc = 12V; V_{LGATE} = 6V	0.9	1.1		A
R_{LGATE}	Low Side Sink Resistance	Vcc = 12V		1.5	3	Ω
	Output Driver Dead Time	PHASE connected to GND	90		210	ns
PROTECTIONS						
I_{OCSET}	OCSET Current Source	V_{OCSET} = 4V	170	200	230	µA
	Over Voltage Trip (V_{FB} / V_{EAREF})	V_{FB} Rising		117	120	%
I_{OSC}	OSC Sourcing Current	V_{FB} > OVP Trip	15	30		mA
POWER GOOD						
	Upper Threshold (V_{FB} / V_{EAREF})	V_{FB} Rising	108	110	112	%
	Lower Threshold (V_{FB} / V_{EAREF})	V_{FB} Falling	88	90	92	%
	Hysteresis (V_{FB} / V_{EAREF})	Upper and Lower threshold		2		%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -4mA		0.4		V
I_{PGOOD}	Output Leakage Current	V_{PGOOD} = 6V		0.2	1	µA

4 DEVICE DESCRIPTION

The device is an integrated circuit realized in BCD technology. The controller provides complete control logic and protection for a high performance step-down DC-DC converter. It is designed to drive N Channel Mosfets in a synchronous-rectified buck topology. The output voltage of the converter can be precisely regulated down to 900mV with a maximum tolerance of ±1.5% when the internal reference is used (simply connecting together EAREF and VREF pins). The device allows also using an external reference (0.9V to 3V) for the regulation. The device provides voltage-mode control with fast transient response. It includes a 200kHz free-running oscillator that is adjustable from 50kHz to 1MHz. The error amplifier features a 10MHz gain-bandwidth product and 10V/µs slew rate that permits to realize high converter bandwidth for fast transient performance. The PWM duty cycle can range from 0% to 100%. The device protects against over-current conditions entering in HICCUP mode. The device monitors the current by using the $r_{DS(ON)}$ of the upper MOSFET(s) that eliminates the need for a current sensing resistor. The device is available in SO16 narrow package.

4.1 Oscillator

The switching frequency is internally fixed to 200kHz. The internal oscillator generates the triangular waveform for the PWM charging and discharging with a constant current an internal capacitor. The current delivered to the oscillator is typically 50µA (F_{sw} = 200KHz) and may be varied using an external resistor (R_T) connected between OSC pin and GND or V_{CC}. Since the OSC pin is maintained at fixed voltage (typ. 1.235V), the frequency is varied proportionally to the current sunk (forced) from (into) the pin.
In particular connecting R_T vs. GND the frequency is increased (current is sunk from the pin), according to the following relationship:

$$f_{OSC,RT} = 200KHz + \frac{4.94 \cdot 10^6}{R_T(K\Omega)}$$

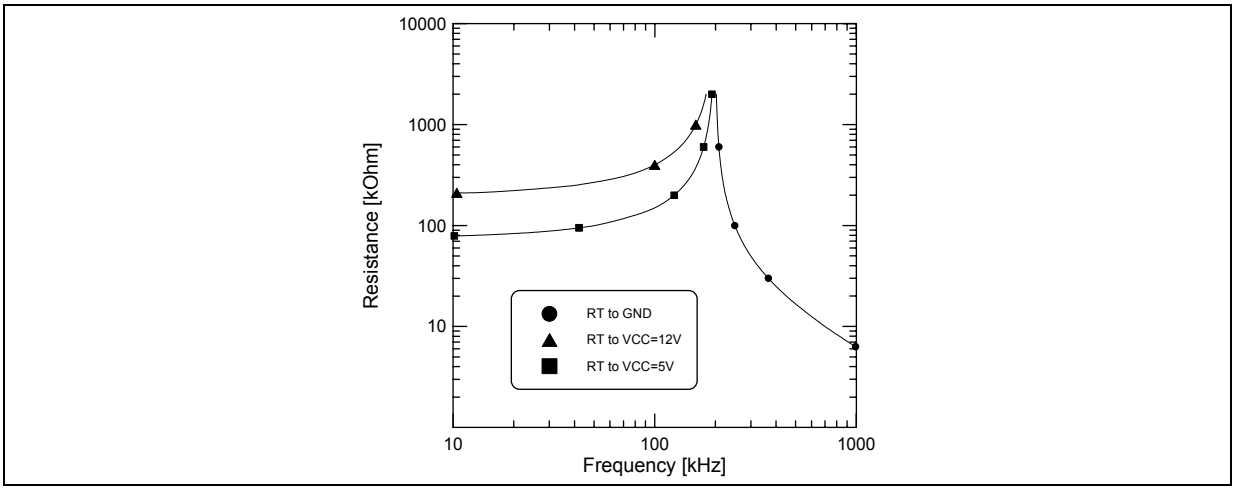
Connecting R_T to V_{CC} = 12V or to V_{CC} = 5V the frequency is reduced (current is forced into the pin), according to the following relationships:

$$f_{OSC,RT} = 200KHz - \frac{4.306 \cdot 10^7}{R_T(K\Omega)} \qquad V_{CC} = 12V$$

$$f_{OSC,RT} = 200KHz - \frac{15 \cdot 10^6}{R_T(K\Omega)} \qquad V_{CC} = 5V$$

Switching frequency variation vs. RT are repeated in Fig. 4.
Note that forcing a 50µA current into this pin, the device stops switching because no current is delivered to the oscillator.

Figure 4.



4.2 Reference

A precise ±1.5% 0.9V reference is available. This reference must be filtered with 1nF ceramic capacitor to avoid instability in the internal linear regulator. It is able to deliver up to 100µA and may be used as reference for the device regulation and also for other devices. If forced under 70% of its nominal value, the device enters in Hiccup mode until this condition is removed.

Through the EAREF pin the reference for the regulation is taken. This pin directly connects the non-inverting input of the error amplifier. An external reference (or the internal 0.9V ±1.5%) may be used. The input for this pin can range from 0.9V to 3V. It has an internal pull-down (300kΩ resistor) that forces the device shutdown if no reference is connected (pin floating). However the device is shut down if the voltage on the EAREF pin is lower than 650mV (typ).

4.3 Soft Start

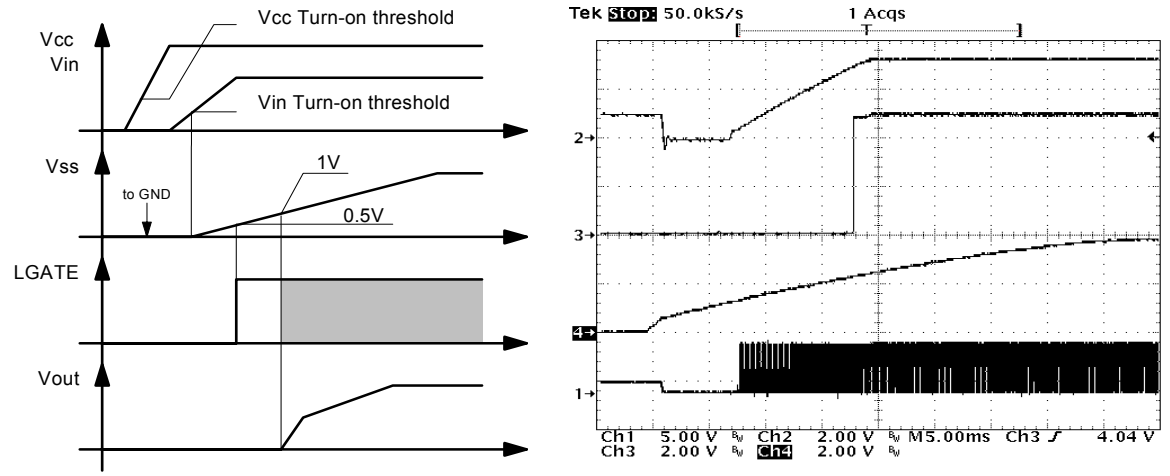
At start-up a ramp is generated charging the external capacitor C_{SS} with an internal current generator. The initial value for this current is of 35µA and speeds-up the charge of the capacitor up to 0.5V. After that it becames 10µA until the final charge value of approximatively 4V.

When the voltage across the soft start capacitor (V_{SS}) reaches 0.5V the lower power MOS is turned on to discharge the output capacitor. As V_{SS} reaches 1.1V (i.e. the oscillator triangular wave inferior limit) also the upper MOS begins to switch and the output voltage starts to increase.

No switching activity is observable if SS is kept lower than 0.5V and both mosfets are off.

If VCC and OCSET pins are not above their own turn-on thresholds and V_{EAREF} is not above 650mV, the Soft-Start will not take place, and the relative pin is internally shorted to GND. During normal operation, if any undervoltage is detected on one of the two supplies, the SS pin is internally shorted to GND and so the SS capacitor is rapidly discharged.

Figure 5. Soft Start (with Reference Present)



Timing Diagram

Acquisition: CH1 = PHASE; CH2 = V_{out}; CH3 = PGOOD; CH4 = V_{ss}

4.4 Driver Section

The driver capability on the high and low side drivers allows using different types of power MOS (also multiple MOS to reduce the R_{DSON}), maintaining fast switching transition.

The low-side mos driver is supplied directly by Vcc while the high-side driver is supplied by the BOOT pin.

Adaptative dead time control is implemented to prevent cross-conduction and allow to use several kinds of mosfets. The upper mos turn-on is avoided if the lower gate is over about 200mV while the lower mos turn-on is

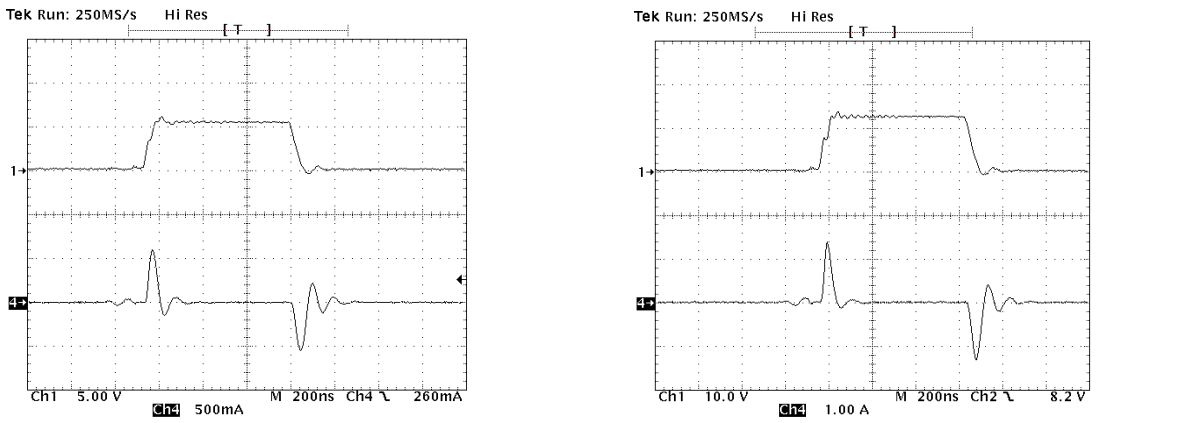
avoided if the PHASE pin is over about 500mV. The lower mos is in any case turned-on after 200ns from the high side turn-off.

The peak current is shown for both the upper (fig. 6) and the lower (fig. 7) driver at 5V and 12V. A 3.3nF capacitive load has been used in these measurements.

For the lower driver, the source peak current is 1.1A @ V_{CC} = 12V and 500mA @ V_{CC} = 5V, and the sink peak current is 1.3A @ V_{CC} = 12V and 500mA @ V_{CC} = 5V.

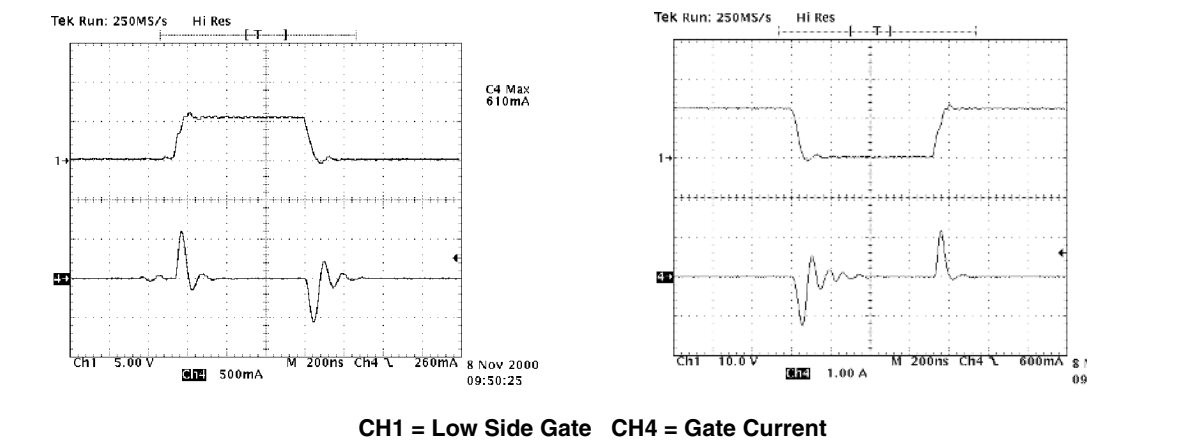
Similarly, for the upper driver, the source peak current is 1.3A @ Vboot-Vphase = 12V and 600mA @ Vboot-Vphase = 5V, and the sink peak current is 1.3A @ Vboot-Vphase =12V and 550mA @ Vboot-Vphase = 5V.

Figure 6. High Side Driver Peak Current. Vboot-Vphase = 12V (right) Vboot-Vphase = 5V (left)



CH1 = High Side Gate CH4 = Gate Current

Figure 7. Low Side Driver Peak Current. V_{CC} = 12V (right) V_{CC} = 5V (left)



CH1 = Low Side Gate CH4 = Gate Current

4.5 Monitoring and Protections

The output voltage is monitored by means of pin FB. If it is not within ±10% (typ.) of the programmed value, the powergood output is forced low.

The device provides overvoltage protection, when the voltage sensed on pin FB reaches a value 17% (typ.) greater than the reference the OSC pin is forced high (3V typ.) and the lower driver is turned on as long as the over-voltage is detected.

Overcurrent protection is performed by the device comparing the drop across the high side MOS, due to the R_{DSON}, with the voltage across the external resistor (R_{OCS}) connected between the OCSET pin and drain of the upper MOS. Thus the overcurrent threshold (I_P) can be calculated with the following relationship:

$$I_P = \frac{R_{OCS} \cdot I_{OCS}}{R_{dsON}}$$

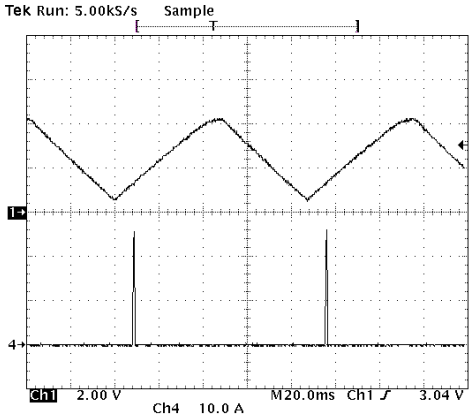
Where the typical value of I_{OCS} is 200µA. To calculate the R_{OCS} value it must be considered the maximum R_{dsON} (also the variation with temperature) and the minimum value of I_{OCS}. To avoid undesirable trigger of overcurrent protection this relationship must be satisfied:

$$I_P \geq I_{OUTMAX} + \frac{\Delta I}{2} = I_{PEAK}$$

Where ΔI is the inductance ripple current and I_{OUTMAX} is the maximum output current.

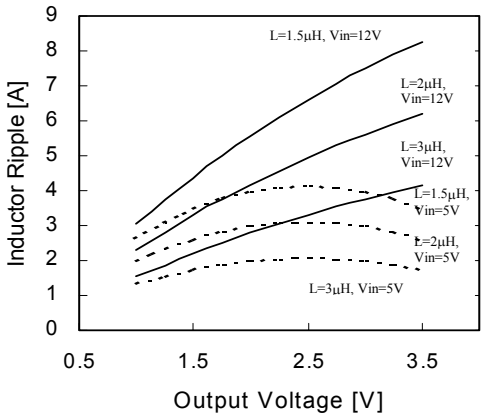
In case of over current detectionthe soft start capacitor is discharged with constant current (10µA typ.) and when the SS pin reaches 0.5V the soft start phase is restarted. During the soft start the over-current protection is always active and if such kind of event occurs, the device turns off both mosfets, and the SS capacitor is discharged again (after reaching the upper threshold of about 4V). The system is now working in HICCUP mode, as shown in figure 8. After removing the cause of the over-current, the device restart working normally without power supplies turn off and on.

Figure 8. Hiccup Mode



CH1 = SS; CH4 = Inductor current

Figure 9. Inductor Ripple Current vs. Vout



4.6 Inductor Design

The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current ΔI_L between 20% and 30% of the maximum output current. The inductance value can be calculated with this relationship:

$$L = \frac{V_{IN} - V_{OUT}}{f_{sw} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

Where f_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage. Figure 9 shows the ripple current vs. the output voltage for different values of the inductor, with V_{IN} = 5V and V_{IN} = 12V.

Increasing the value of the inductance reduces the ripple current but, at the same time, reduces the converter response time to a load transient. If the compensation network is well designed, the device is able to open or close the duty cycle up to 100% or down to 0%. The response time is now the time required by the inductor to change its current from initial to final value. Since the inductor has not finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required.

The response time to a load transient is different for the application or the removal of the load: if during the application of the load the inductor is charged by a voltage equal to the difference between the input and the output voltage, during the removal it is discharged only by the output voltage. The following expressions give approximate response time for ΔI load transient in case of enough fast compensation network response:

$$t_{application} = \frac{L \cdot \Delta I}{V_{IN} - V_{OUT}} \qquad t_{removal} = \frac{L \cdot \Delta I}{V_{OUT}}$$

The worst condition depends on the input voltage available and the output voltage selected. Anyway the worst case is the response time after removal of the load with the minimum output voltage programmed and the maximum input voltage available.

4.7 Output Capacitor

The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for first few microseconds they supply the current to the load. The controller recognizes immediately the load transient and sets the duty cycle at 100%, but the current slope is limited by the inductor value. The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

$$\Delta V_{OUT} = \Delta I_{OUT} \cdot ESR$$

A minimum capacitor value is required to sustain the current during the load transient without discharge it. The voltage drop due to the output capacitor discharge is given by the following equation:

$$\Delta V_{OUT} = \frac{\Delta I_{OUT}^2 \cdot L}{2 \cdot C_{OUT} \cdot (V_{INMIN} \cdot D_{MAX} - V_{OUT})}$$

Where D_{MAX} is the maximum duty cycle value that is 100%. The lower is the ESR, the lower is the output drop during load transient and the lower is the output voltage static ripple.

4.8 Input Capacitor

The input capacitor has to sustain the ripple current produced during the on time of the upper MOS, so it must have a low ESR to minimize the losses. The rms value of this ripple is:

$$I_{rms} = I_{OUT}\sqrt{D \cdot (1 - D)}$$

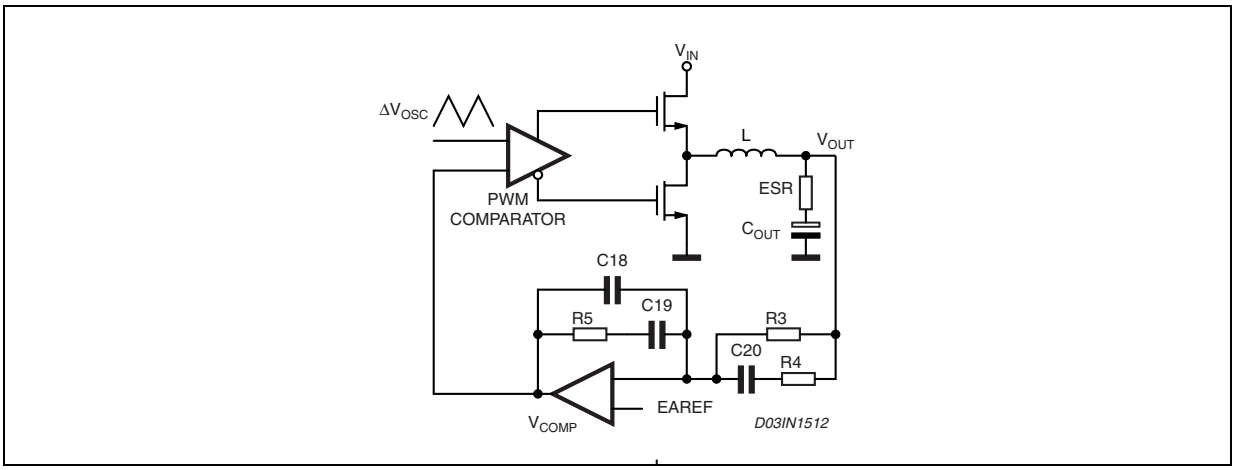
Where D is the duty cycle. The equation reaches its maximum value with D = 0.5. The losses in worst case are:

$$P = ESR \cdot I_{rms}^2$$

4.9 Compensation Network Design

The control loop is a voltage mode (figure 10). The output voltage is regulated to the input Reference voltage level (EAREF). The error amplifier output V_{COMP} is then compared with the oscillator triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. This wave is filtered by the output filter. The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function has a double pole at frequency F_{LC} depending on the L-C_{out} resonance and a zero at F_{ESR} depending on the output capacitor ESR. The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Figure 10. Compensation Network



The compensation network consists in the internal error amplifier and the impedance networks Z_{IN} (R3, R4 and C20) and Z_{FB} (R5, C18 and C19). The compensation network has to provide a closed loop transfer function with the highest 0dB crossing frequency to have fast response (but always lower than fsw/10) and the highest gain in DC conditions to minimize the load regulation.

A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45°. Include worst-case component variations when determining phase margin.

To locate poles and zeroes of the compensation networks, the following suggestions may be used:

Modulator singularity frequencies:

$$\omega_{LC} = \frac{1}{\sqrt{L \cdot C_{OUT}}} \qquad \omega_{ESR} = \frac{1}{ESR \cdot C_{OUT}}$$

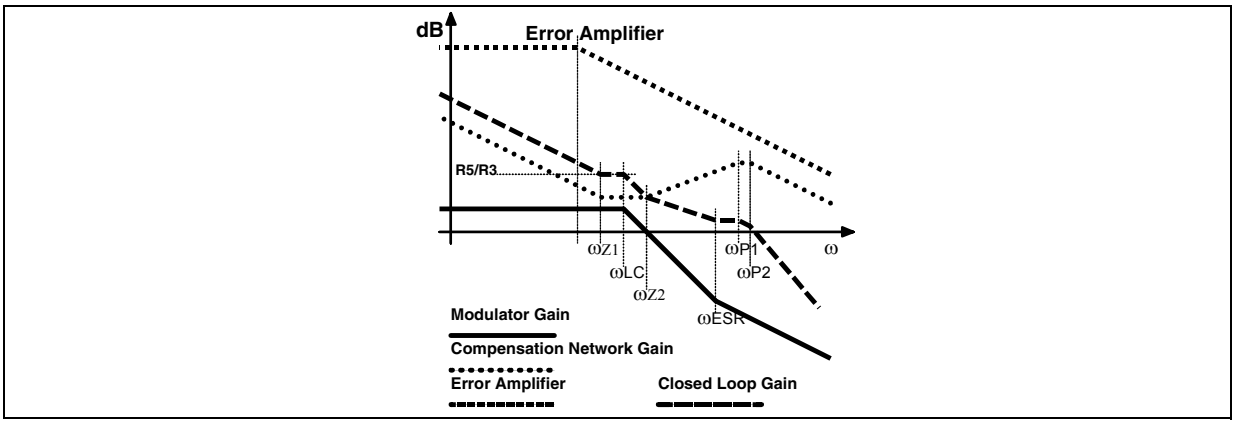
Compensation network singularity frequency:

$$\omega_{P1} = \frac{1}{R5 \cdot \left(\frac{C18 \cdot C19}{C18 + C19}\right)} \qquad \omega_{P2} = \frac{1}{R4 \cdot C20}$$

$$\omega_{Z1} = \frac{1}{R5 \cdot C19} \qquad \omega_{Z2} = \frac{1}{(R3 + R4) \cdot C20}$$

- Put the gain R5/R3 in order to obtain the desired converter bandwidth;
- Place ω_{Z1} before the output filter resonance ω_{LC};
- Place ω_{Z2} at the output filter resonance ω_{LC};
- Place ω_{P1} at the output capacitor ESR zero ω_{ESR};
- Place ω_{P2} at one half of the switching frequency;
- Check the loop gain considering the error amplifier open loop gain.

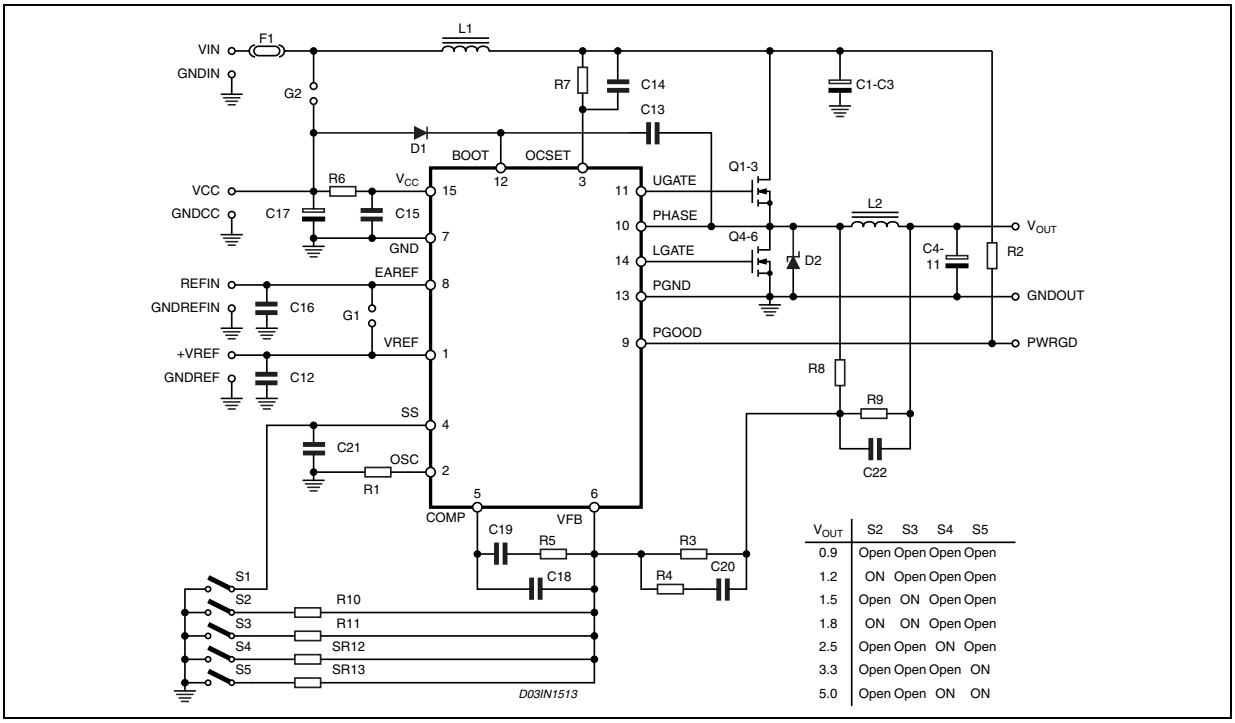
Figure 11. Asymptotic Bode Plot of Converter's Gain



5 15A DEMO BOARD DESCRIPTION

The demo board shows the operation of the device in a general purpose application. This evaluation board allows voltage adjustability from 0.9V to 5V through the switches S2-S5 according to the reported table when the internal 0.9V reference is used (G1 closed). Output current in excess of 20A can be reached dependently on the kind of mosfet used: up to three SO8 mosfet may be used for both High side and Low side switches. External reference may be used for the regulation simply leaving open G1 and the switches S2-S5. The device may also be disabled with the switch S1. The V_{CC} input rail supplies the device while the power conversion starts from the V_{IN} input rail. The device is also able to operate with a single supply voltage; in this case the jumper G2 has to be closed and a 5V to 12V input can be directly connected to the V_{IN} input. The four layers demo board's copper thickness is of 70µm in order to minimize conduction losses considering the high current that the circuit is able to deliver.The PGOOD signal is used as a logic level and it's been pulled up to V_{IN} because there's no other appropriate voltage available on the demo board. **In case of input voltage higher than 7V (PGOOD Pin Maximum Absolute Rating) a 5V reference is required.** Figure 12 shows the demo board's schematic circuit

Figure 12. 15A Demo Board Schematic



V_{OUT}	S2	S3	S4	S5
0.9	Open	Open	Open	Open
1.2	ON	Open	Open	Open
1.5	Open	ON	Open	Open
1.8	ON	ON	Open	Open
2.5	Open	Open	ON	Open
3.3	Open	Open	Open	ON
5.0	Open	Open	ON	ON

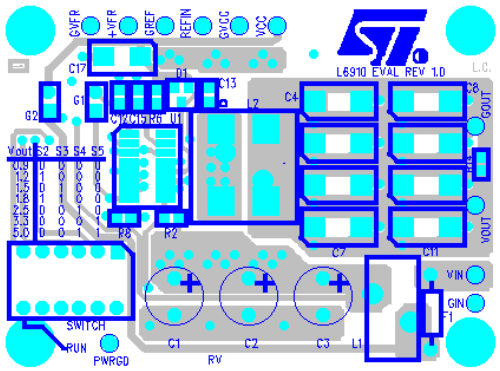
Table 6. Part List

Reference	Description	Manufacturer	
R1	N.C	NEOHM	
R2	10K 5% 125mW	NEOHM	SMD 0805
R3	4.7K 5% 125mW	NEOHM	SMD 0805
R4	1KOhm 5% 125mW	NEOHM	SMD 0805
R5	2.7K 5% 125mW	NEOHM	SMD 0805
R6	10Ohm 5% 125mW	NEOHM	SMD 0805
R7	510Ohm 5% 125mW	NEOHM	SMD 0805
R8	N.C		
R9	0 Ohm		SMD 0805
R10	14K 5% 125mW	NEOHM	SMD 0805
R11	6.98K 5% 125mW	NEOHM	SMD 0805
R12	2.61K 5% 125mW	NEOHM	SMD 0805
R13	1.74K 5 5% 125mW	NEOHM	SMD 0805
C1, C3	100µF - 20V	OSCON 20SA100M	RADIAL 10X10.5
C9, C10	330µF - 6.3V	POSCAP 6TPB330M	SMD7343
C12, C13, C15, C21	100nF	KEMET	SMD0805
C14	1nF	KEMET	SMD0805
C16	100nF	KEMET	
C17	4.7µF - 16V	AUX	SMA6032
C18	1.5nF	KEMET	SMD0805
C19	15nF	KEMET	SMD0805
C20	47nF	KEMET	SMD0805
C22	N.C		
L1	Short		
L2	3µH (T50-52B Core, 7T AWG15)	MICROMETALS	
Q2,Q3,Q4,Q6	STS11NF30L	ST	SO8
D1	1N4148		SOT23
D2	STPS2L25U	ST	SMB
U1	Device L6910G	ST	SO16Narrow
F1	Short		
SWITCH	DIP SWITCH 6 POS.		

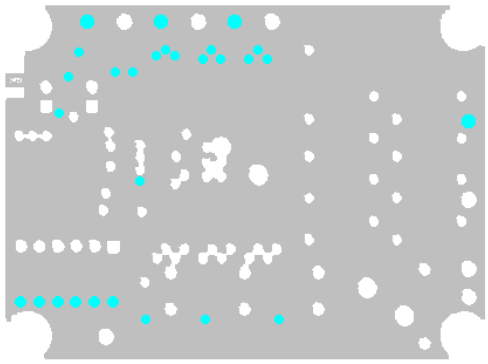
Table 7. Other Inductor Manufacturer

Manufacturer	Series	Inductor Value (µH)	Saturation Current (A)
WÜRTH ELEKTRONIK	744318	1.8 to 2.7	16 to 20
PANASONIC	ETQP6F1R8FA	1.8	20
SUMIDA	CDEP134-2R7MC-H	2.7	15

Figure 13. PCB and Components Layouts

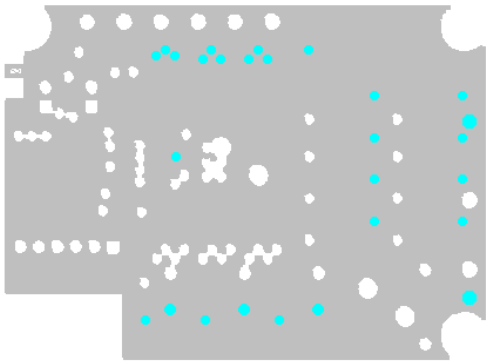


Component Side

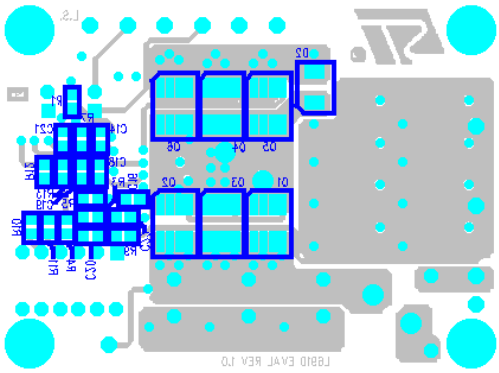


Internal Signal GND Layer

Figure 14. PCB and Components Layouts



Internal Power GND Layer



Solder Side

Figure 15. Efficiency vs Output Current

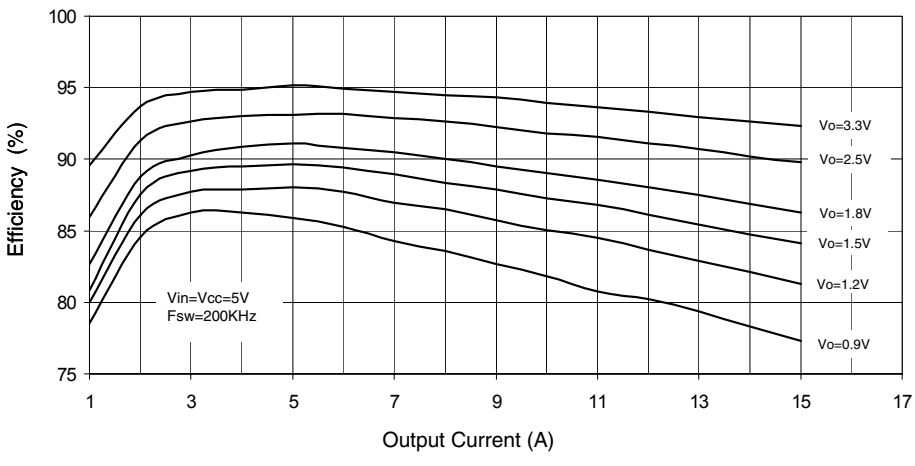
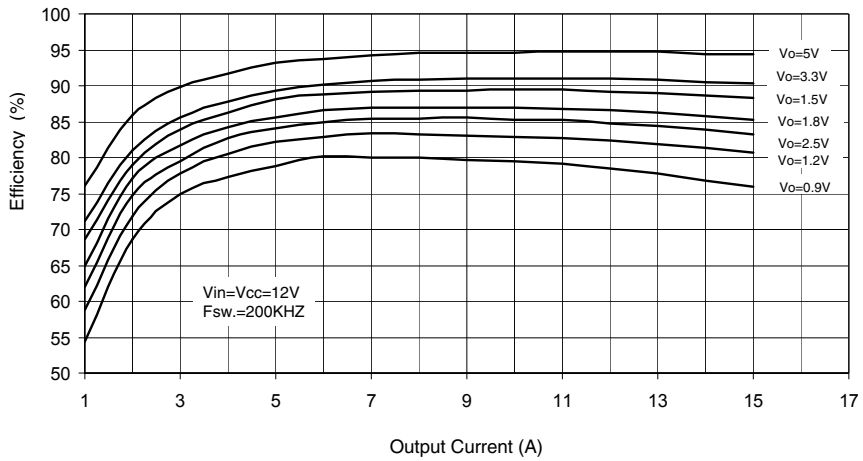


Figure 16. Efficiency vs Output Current



6 COMPONENTS SELECTION

6.1 Inductor Selection

To select the right inductor value, the application conditions must be fixed. For example we can consider:

Vin=12V Vout =3.3V Iout=15A

Considering a ripple of approximately 25% to 30% of Iout, the inductor value will be L=3 μH.

An iron powder core (TO50-52B) with 7 windings has been chosen.

6.2 Output Capacitors

2 POSCAP capacitors, model 6TPB330M, have been chosen, with a maximum ERS equal to 40mΩ each. Therefore, the resultant ESR is of 20mΩ. Considering a current ripple of 4A, the output voltage ripple is:

$$\Delta Vout = 4 \cdot 0.02 = 80mV$$

6.3 Input Capacitors

For I_{OUT} = 15A and D = 0.5 (worst case for input current ripple), the RMS current of the input capacitor is equal to 7.5A.

Two OSCON electrolytic capacitors 6SP680M, with a maximum ESR equal to 13mΩ, have been chosen to sustain the ripple. Therefore, the resultant ESR is equal to 13mΩ/2 = 6.5mΩ. The losses, in worst case, are:

$$P = ESR \cdot I^2rms = 366mW$$

6.4 Over-Current Protection

The current limit can be set to approximately 20A. Substituting the demo board parameters in the relationship reported in the relative section, (I_{OSCMIN} =170μA; IP = 20A; $R_{DSONMAX}$ = 9mΩ / 2=4.5mΩ) it results that R_{OCS} = 510Ω

6.5 APPLICATION SUGGESTIONS FOR HIGHER CURRENTS

For higher output currents, up to 20A, the following configuration can be used (with reference to the demo board schematic):

Q1,Q2,Q3: STS11NF30L

Q4,Q5,Q6: STS17NF3LL

L: 2.5μH Magnetic 77121A7 Core 7T 2x AWG16

In these conditions, the following performance have been achieved:

Table 8.

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	η (%)		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	η (%)
5	1.2	20	81		12	1.2	20	80
5	1.5	20	83		12	1.5	20	83
5	1.8	20	85		12	1.8	20	85
5	2.5	20	89		12	2.5	20	88
5	3.3	20	91		12	3.3	20	91
					12	5	20	93

For currents higher than 20A, bigger mosfets should be selected (e.g. STS25NH3LL) both for the high side and low side (depending on the duty cycle and input voltage).

7 6A DEMO BOARD DESCRIPTION

A compact demo board has been realized to manage currents in the range of 5A-6A .
The external power mosfets are included in a single SO8 package to save space and increase power density. Two separate rails are provided, for V_{CC} and V_{IN}. They can be connected together by shorting the jumper J1. The PGOOD signal is used as a logic level and it's been pulled up to V_{IN} because there's no other appropriate voltage available on the demo board. **In case of input voltage higher than 7V (PGOOD Pin Maximum Absolute Rating) a 5V reference is required.**

Figure 17. 6A Demo Board Schematic

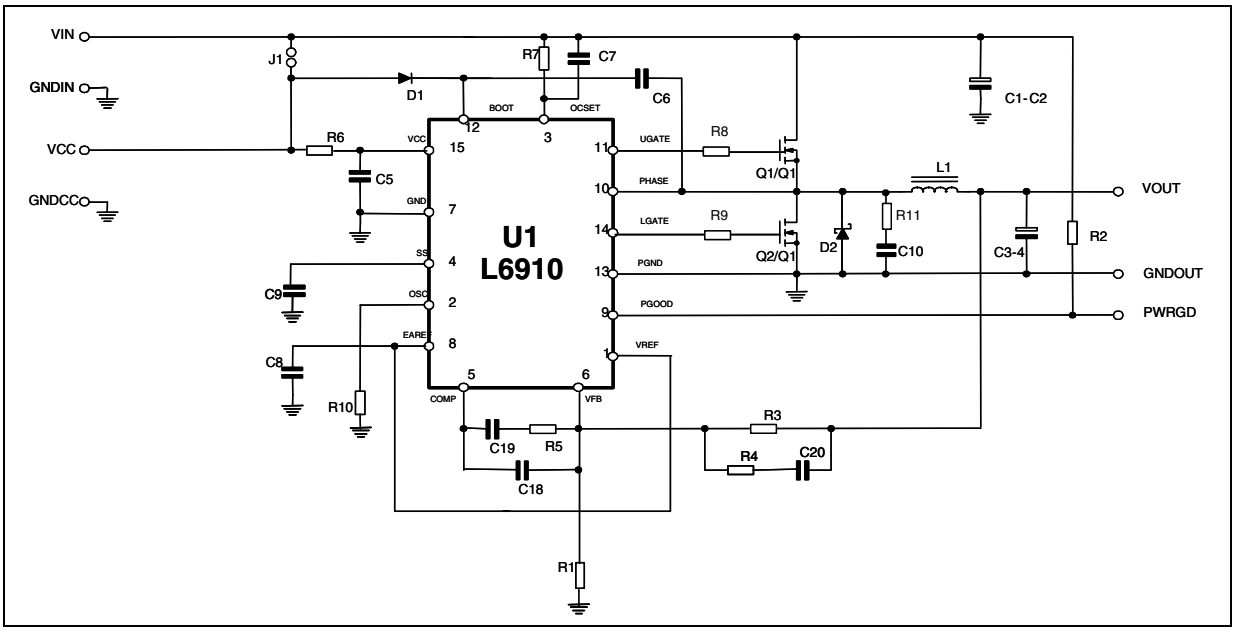


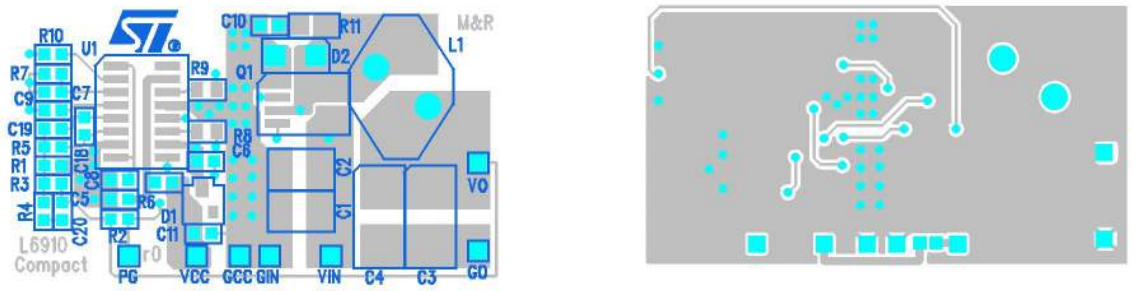
Table 9. Part List

Reference	Description	Manufacturer	
Resistor			
R1	2K7 Ohm 0805 5% 125mW	NEOHM	(Vout = 2.5V)
	1K8 Ohm 0805 5% 125mW	NEOHM	(Vout = 3.3V)
	1K Ohm 0805 5% 125mW	NEOHM	(Vout = 5V)
R2	10K 5% 125mW	NEOHM	SMD 0805
R3	4K7 5% 125mW	NEOHM	SMD 0805
R4	4K7 5% 125mW	NEOHM	SMD 0805
R5	2K7 5% 125mW	NEOHM	SMD 0805
R6	10 Ohm 5% 125mW	NEOHM	SMD 0805
R7	680 Ohm 5% 125mW	NEOHM	SMD 0805
R8 R9	2.2 Ohm 5% 125mW	NEOHM	SMD 0805
R10	N.C		
R11	N.C		
Capacitors			
C1,C2	10µF 25V	TOKIN	C34Y5U1E106ZTE12
C3,C4	100µF - 6.3V	POSCAP 6TPB100M	SMD7343
C5,C6,C9	100nF	KEMET	SMD0805
C7,C8	1nF	KEMET	SMD0805
C10	N.C		
C18	1.5nF	KEMET	SMD0805
C19	15nF	KEMET	SMD0805
C20	47nF	KEMET	SMD0805
Magnetics			
L1	7µH (T50-52B Core, 12T AWG 21)	MICROMETALS	
Transistor			
Q1	STS8DNF3LL	ST	
Diodes			
D1	1N4148		SOT23
D2	STPS2L25U	ST	SMB
Device			
U1	Device L6910G	ST	SO16Narrow

Table 10. Other inductor manufacturer

Manufacturer	Series	Inductor Value (µH)	Saturation Current (A)
WÜRTH ELEKTRONIK	744 382	4.8 to 5.8	7.5 to 8
PANASONIC	ETQP6F	4.6 to 6.4	9.3 to 7.9
SUMIDA	CDEP134-H	6 to 8	7.2 to 9.6
COILCRAFT	DO3316P-472HC	4.7	5.4
	DO3340P	10 to 22	8 to 5.5
COILTRONICS	DR125-8R2	8.2	7.8

Figure 18. PCB and Components Layouts



Component Side

Solder Side

7.1 Compact Demo Board Performances

Figures 19, 20 show the measured efficiency versus load current for different values of output voltage. The measure has been done at 5V and 12V input. Output voltage has been changed modifying the value of R1 in the demo board as reported in the part list.

Figure 19. Efficiency vs. Output Current

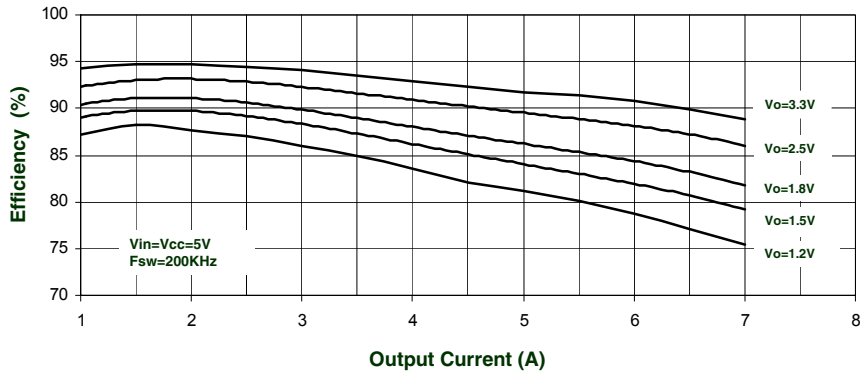
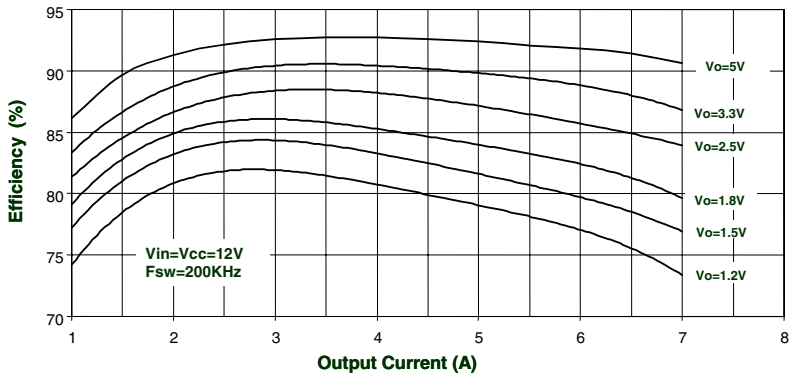


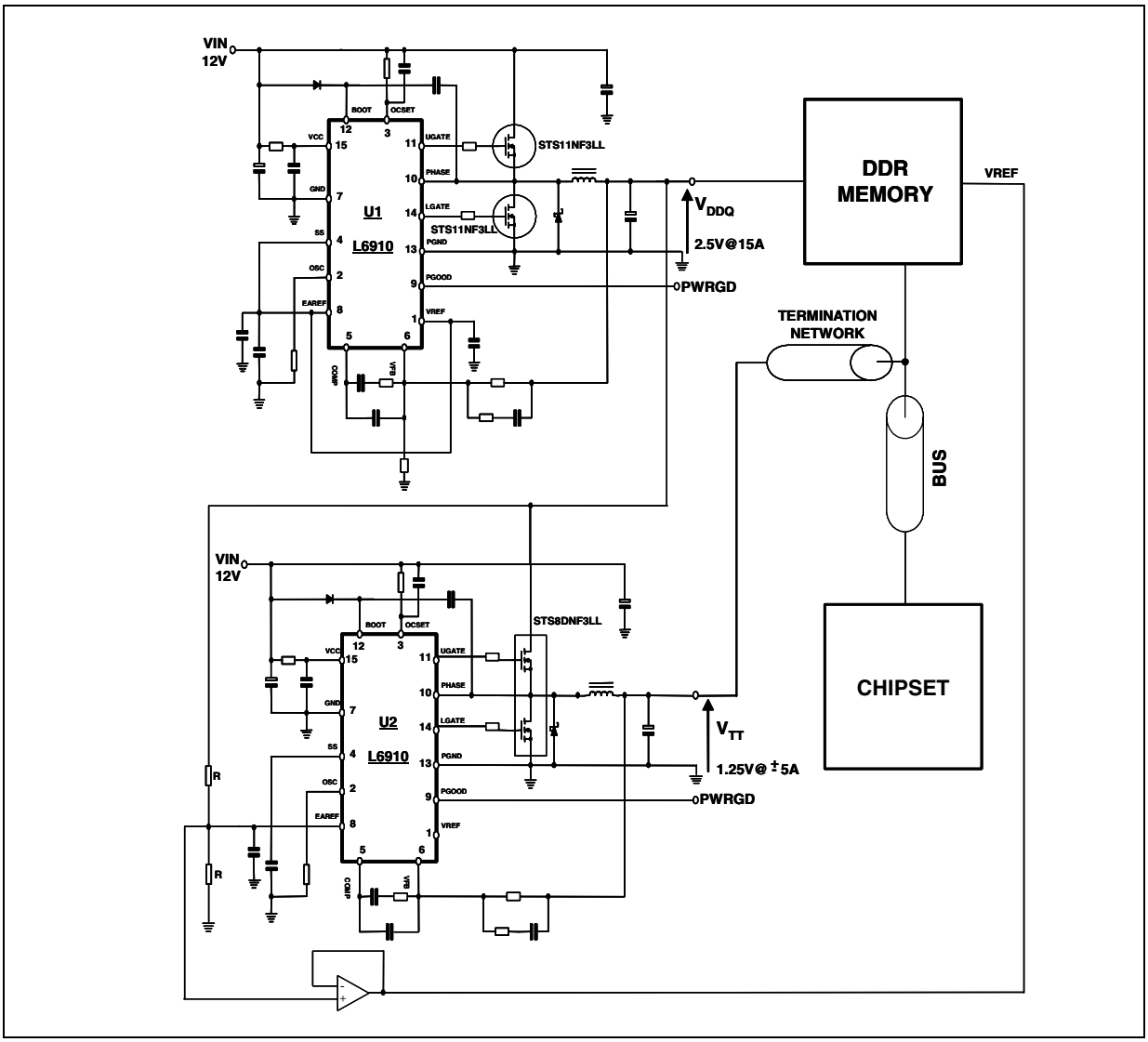
Figure 20. Efficiency vs. Output Current



8 APPLICATION IDEA 1: DDR MEMORY AND TERMINATION SUPPLY

Double Data Rate (DDR) Memories require a particular Power Management Architecture. This is due to the fact that the trace between the driving chipset and the memory input must be terminated with resistors.
Since the Chipset driving the Memory has a push pull output buffer, the Termination voltage must be capable of sourcing and sinking current.
Moreover, the Termination voltage must be equal to one half of the memory supply (the input of the memory is a differential stage requiring a reference bias midpoint) and in tracking with it. For DDRI the Memory Supply is 2.5V and the Termination voltage is 1.25V while, for DDRII, the Memory Supply is 1.8V and the Termination voltage is 0.9V. Fig. 23 shows a complete DDRI Memory and Termination Power Supply realized by using 2 x L6910G. The 2.5V section is powering the memory while the 1.25V section is providing the termination voltage. The tracking between the two sections is realized by providing the EAREF voltage of the 1.25V section through a resistor divider connected to the 2.5V.

Figure 21. Application idea : DDR Memory Supply



The current required by the memory and the termination supply, depends on the memory type and size.
The figure 22, 23 shows the efficiency of the L6910G for the termination section of the application shown in fig. 21, in sink and source mode. The figures show the efficiency values also when the input voltage is coming directly from the 12V rail.

Figure 22. Efficiency vs Output Current Source Mode

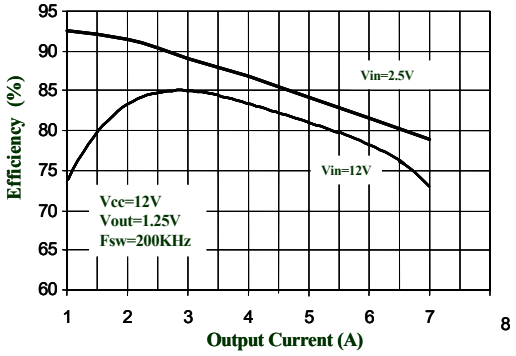
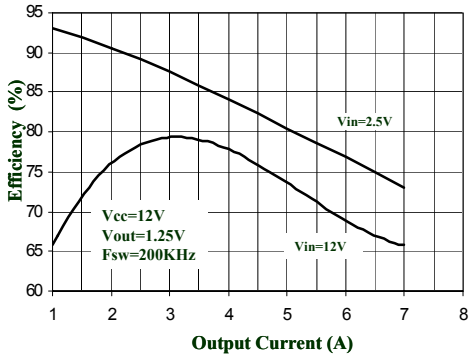


Figure 23. Efficiency vs Output Current Sink Mode



For very big systems (e.g. servers), the DDR memory termination can require much higher currents, in the range of 10A-15A and more.

Figures 24, 25 and 26, 27 show the efficiency of the L6910G in sink and source mode, up to 17A both for DDRI and DDRII memories.The measurements have been realized with the 15A demo board. (See pag.11)

Figure 24. Efficiency vs Output Current Sink Mode

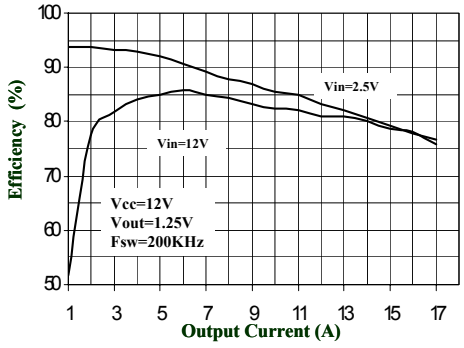


Figure 25. Efficiency vs Output Current Sink Mode

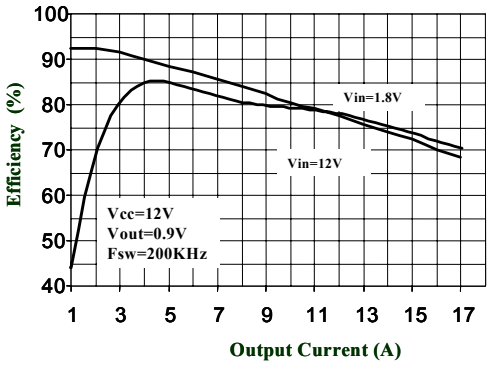


Figure 26. Efficiency vs Output Current Source Mode

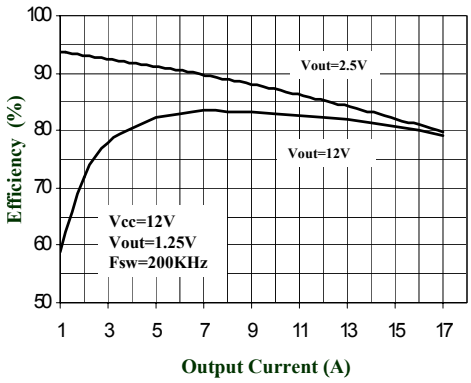
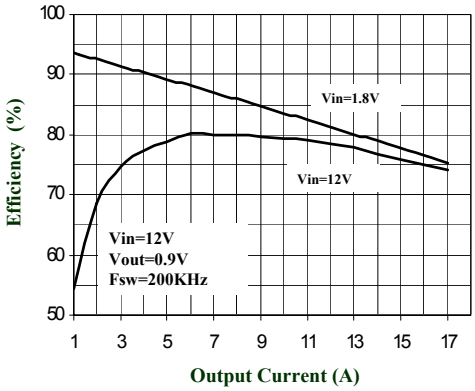


Figure 27. Efficiency vs Output Current Source Mode



9 APPLICATION IDEA 2: POSITIVE BUCK-BOOST REGULATOR 3V TO 13.2V INPUT / 5V 2.5A OUTPUT

In some applications the input voltage changes in a very wide range while the output must be regulated to a fixed value. In this case a Buck-Boost topology can be required in order to keep the output voltage in regulation.

The schematic below shows how to implement a Buck-Boost regulating 5V at the output from both 3.3V and 5V and 12V input buses.

In a Buck-Boost topology the current is delivered to the output during the OFF phase only. So, for a given current limit, the maximum output current depends strongly on the duty cycle. Assuming a 100% efficiency and neglecting the current ripple across the inductor, the relationship betweent the current limit and the maximum output current is the following:

$$I_{OMAX} = I_{LIM} \cdot (1 - D)$$

Where I_{LIM} is the current limit and D is the duty cycle of the application.

The worst case is with D_{MAX}. Since, in a Buck-Boost application, D is given by the following formula:

$$D = \frac{V_O}{V_{IN} + V_O}$$

The worst case is with V_{INMIN}.

Obviously, since the efficiency is lower than 100% and the ripple is usually not negligible, the maximum output current is always lower than the value calculated in the above formula

Figure 28. Positive buck-boost regulator 3V to 13.2V input / 5V 2.5A Output Circuit

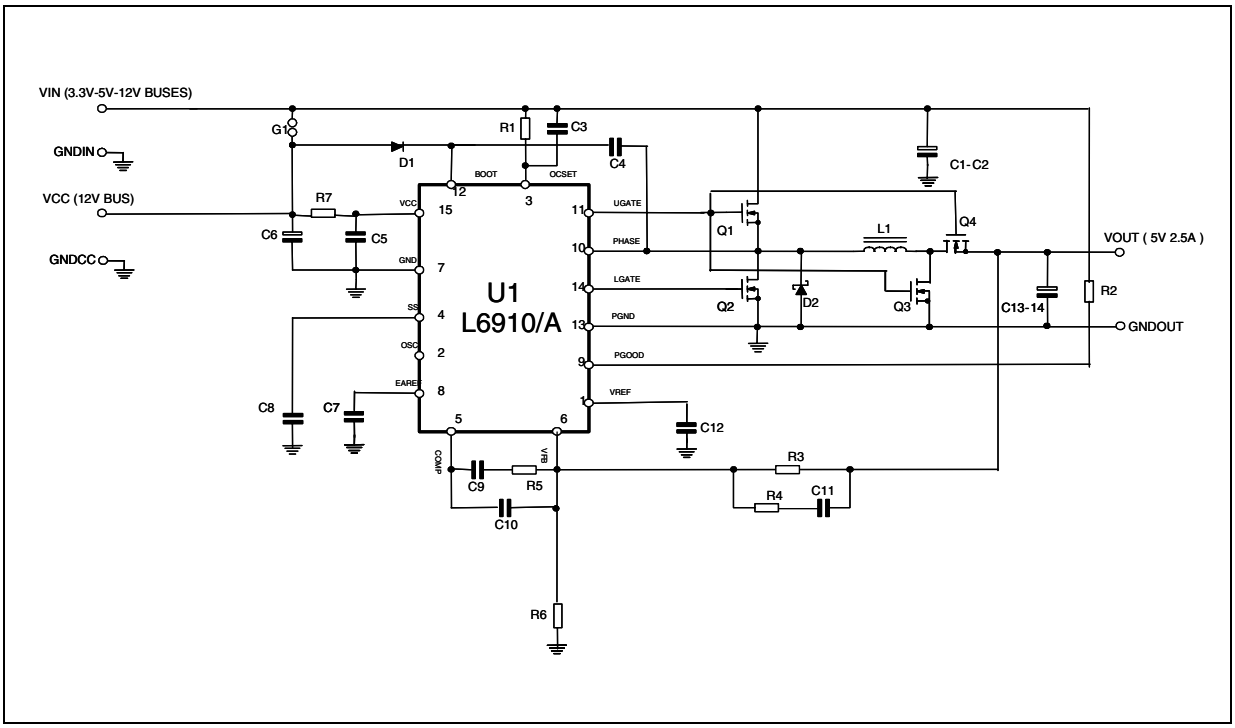
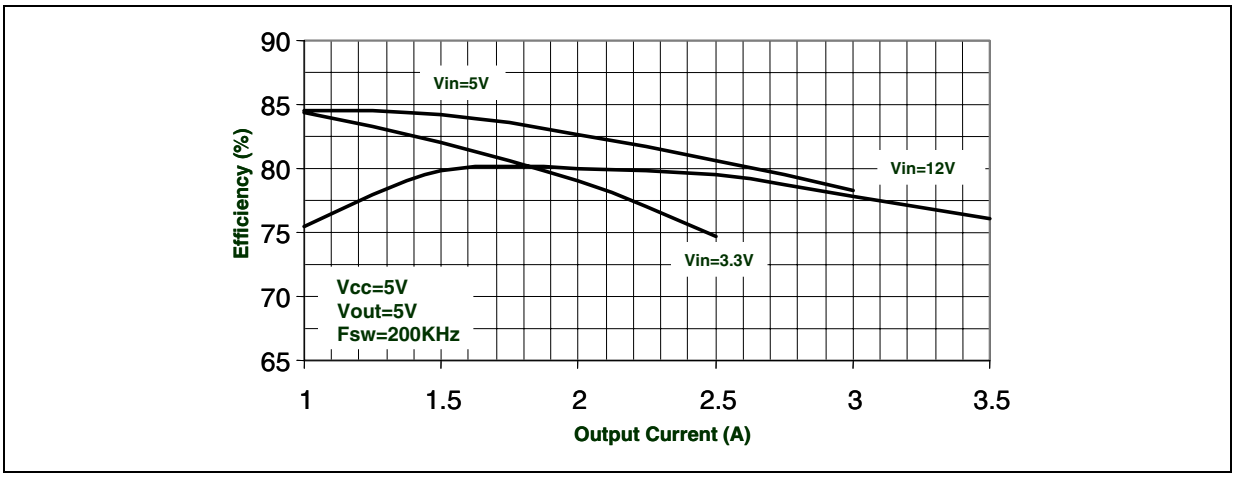


Table 11. Part List

Reference	Description	Manufacturer	
R1	910 Ohm 5% 125mW	NEOHM	SMD 0805
R2	10K 5% 125mW	NEOHM	SMD 0805
R3	4.7K 5% 125mW	NEOHM	SMD 0805
R4	1K 5% 125mW	NEOHM	SMD 0805
R5	2.7K 5% 125mW	NEOHM	SMD 0805
R6	1K1	NEOHM	SMD 0805
R7	10 Ohm 125mW	NEOHM	SMD 0805
C1,C2	100µF - 20V	OSCON 20SA100M	RADIAL 10X10.5
C13,C14	330µF - 6.3V	POSCAP 6TPB330M	SMD7343
C12,C5,C8	100nF	KEMET	SMD0805
C3	1nF	KEMET	SMD0805
C4	470nF	KEMET	SMD0805
C6	4.7µF - 16V	AUX	SMA6032
C7	100nF	KEMET	
C9	15nF	KEMET	SMD0805
C10	1.5nF	KEMET	SMD0805
C11	47nF	KEMET	SMD0805
G1	Open	Jumper	
L1	2.5µH (77121A7 Core, Double winding 7 AWG16)	MAGNETICS	
Q1,Q2,Q3	STS11NF30L	ST	SO8
Q4	STS5P30L	ST	SO8
D1	1N4148		SOT23
D2	STPS3L25U (STPS340U)	ST	SMB (D0144)
U1	Device L6910G	ST	SO16 Narrow

Figure 29. Efficiency vs. Output Current



10 APPLICATION IDEA 3: BUCK-BOOST REGULATOR 3V TO 5.5V INPUT/-5V 3A OUTPUT

In applications where a negative output voltage is required, a standard Buck-Boost topology can be implemented. The considerations related to the maximum output current are the same of the "Positive Buck-Boost" (Application Idea 2).

A particularity of this topology is that the device undergoes a voltage that is the sum of V_{IN} and V_{OUT}. So, converting 5V to -5V, the device undergoes 10V voltage. It must be checked that the sum of the input and output voltage is lower than the maximum operating input voltage of the device.

Figure 30. buck-boost regulator 3V to 5.5V input / -5V 3A Output Circuit

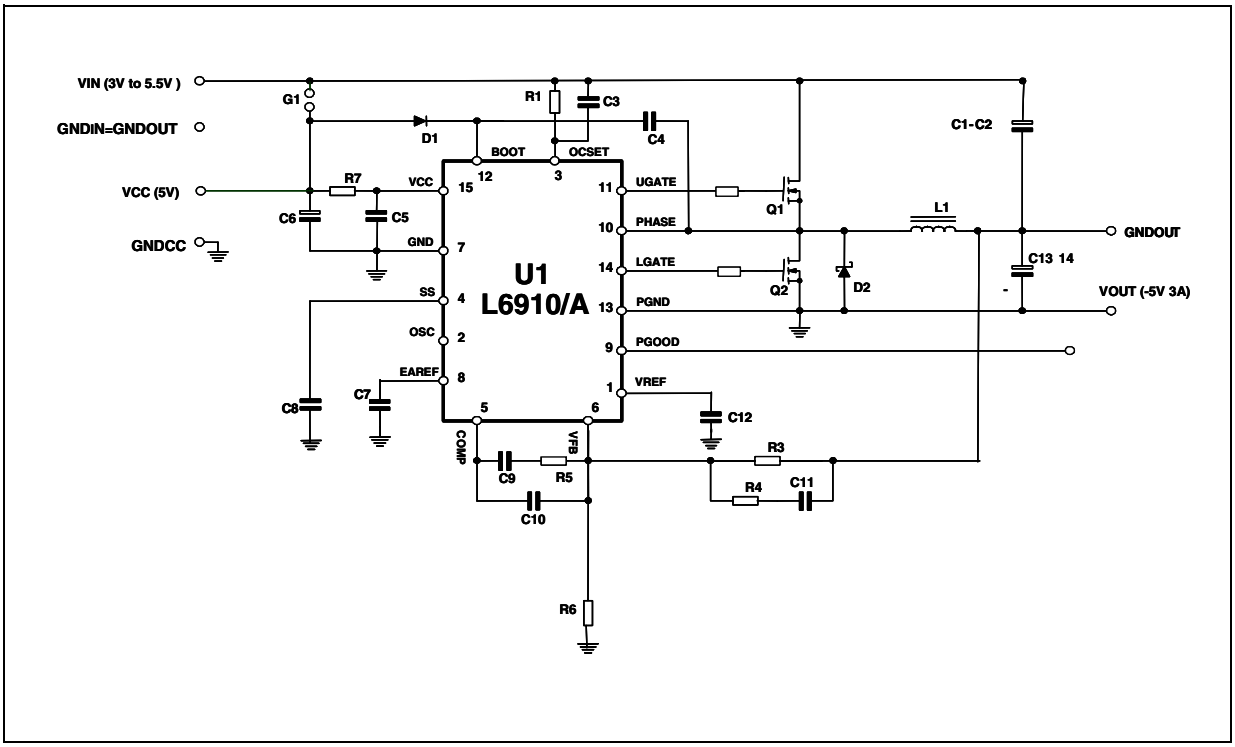


Table 12. Part List

Reference	Description	Manufacturer	
R1	910 Ohm 5% 125mW	NEOHM	SMD 0805
R2	10K 5% 125mW	NEOHM	SMD 0805
R3	4.7K 5% 125mW	NEOHM	SMD 0805
R4	1K Ohm 5% 125mW	NEOHM	SMD 0805
R5	2.7K 5% 125mW	NEOHM	SMD 0805
R6	1K 5% 125mW	NEOHM	SMD 0805
R7	10 Ohm 5% 125mW	NEOHM	SMD 0805
C1,C2	100µF - 20V	OSCON 20SA100M	RADIAL 10X10.5
C13,C14	330µF - 6.3V	POSCAP 6TPB330M	SMD7343
C12,C4,C5,C8	100nF	KEMET	SMD0805
C3	1nF	KEMET	SMD0805
C6	4.7µF - 16V	AUX	SMA6032
C7	100nF	KEMET	

Table 12. Part List (continued)

C9	15nF	KEMET	SMD0805
C10	1.5nF	KEMET	SMD0805
Reference	**Description**	**Manufacturer**	
C11	47nF	KEMET	SMD0805
G1	Open	Jumper	
L1	2.5µH (77121A7 Core, Double winding 7 AWG16)	MAGNETICS	
Q1,Q2	STS11NF30L	ST	SO8
D1	1N4148		SOT23
D2	STPS3L25U (STPS340U)	ST	SMB (D0144)
U1	Device L6910G	ST	SO16 Narrow

Figure 31. Efficiency vs. Output Current

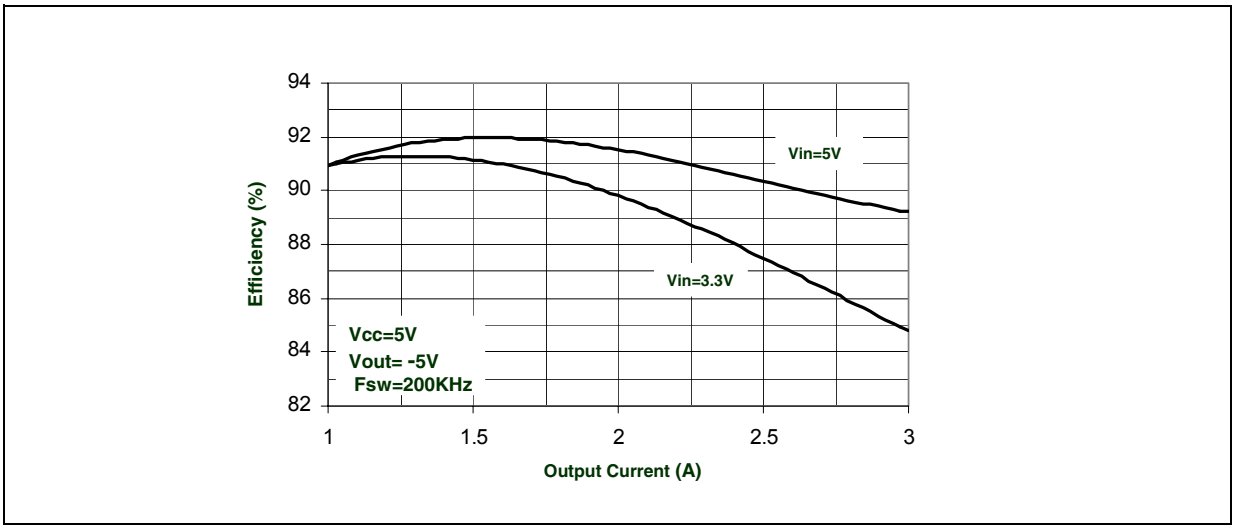
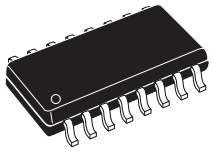


Figure 32. SO-16 (Narrow) Mechanical Data & Package Dimensions

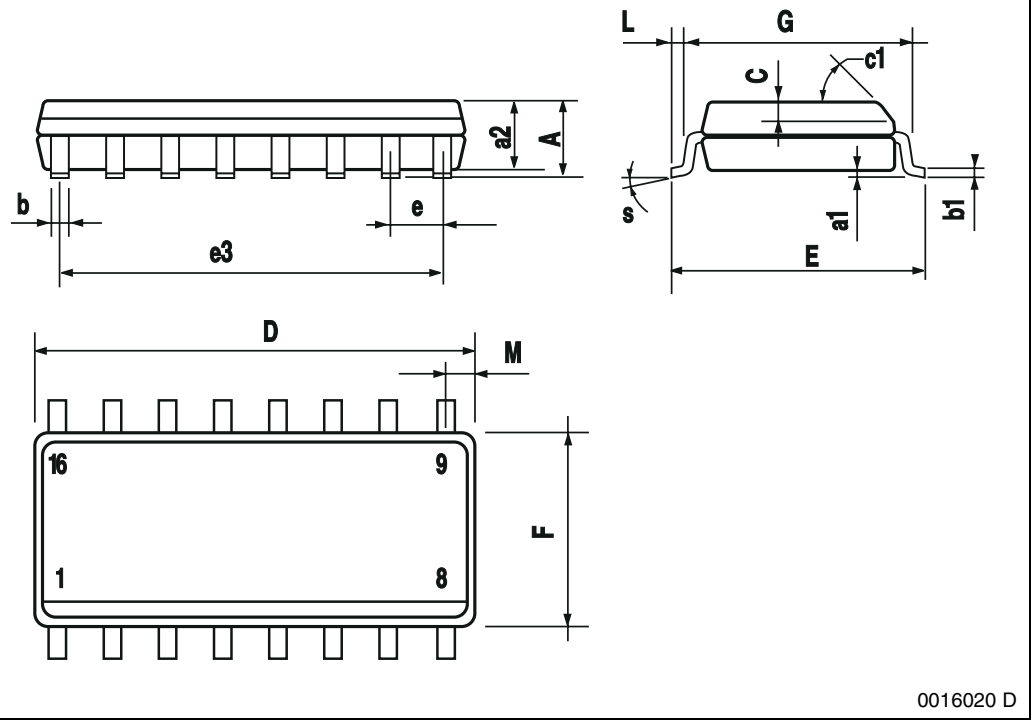
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 ° (max.)					

(1) "D" and "F" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.006inc.)

OUTLINE AND MECHANICAL DATA



SO16 (Narrow)



0016020 D

Table 1. Revision History

Date	Revision	Description of Changes
May 2005	1	First Issue