

# TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Open Drain Power-On Reset With 200-ms Delay (TPS775xx)
- Open Drain Power Good (TPS776xx)
- 500-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.6-V (TPS77516 Only), 1.8-V, 2.5-V, 2.8-V (TPS77628 Only), 3.3-V Fixed Output and Adjustable Versions
- Dropout Voltage to 169 mV (Typ) at 500 mA (TPS77x33)
- Ultralow 85  $\mu$ A Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- 20-Pin TSSOP PowerPAD™ (PWP) Package
- Thermal Shutdown Protection

## description

The TPS775xx and TPS776xx devices are designed to have a fast transient response and be stable with a 10- $\mu$ F low ESR capacitors. This combination provides high performance at a reasonable cost.

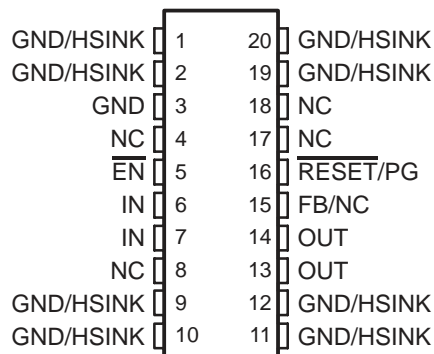
Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 169 mV at an output current of 500 mA for the TPS77x33) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85  $\mu$ A over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to  $\overline{\text{EN}}$  (enable) shuts down the regulator, reducing the quiescent current to 1  $\mu$ A at  $T_J = 25^\circ\text{C}$ .

The  $\overline{\text{RESET}}$  output of the TPS775xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS775xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

Power good (PG) of the TPS776xx is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS775xx and TPS776xx are offered in 1.5-V, 1.6-V (TPS77516 only), 1.8-V, 2.5-V, 2.8 V (TPS77628 only), and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V for TPS77501 option and 1.2 V to 5.5 V for TPS77601 option). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS775xx and TPS776xx families are available in 20 pin TSSOP package.

PWP PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

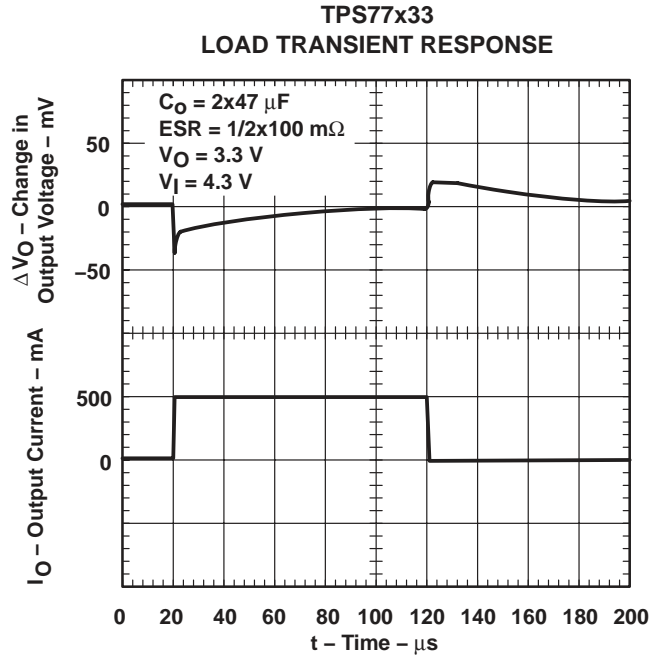
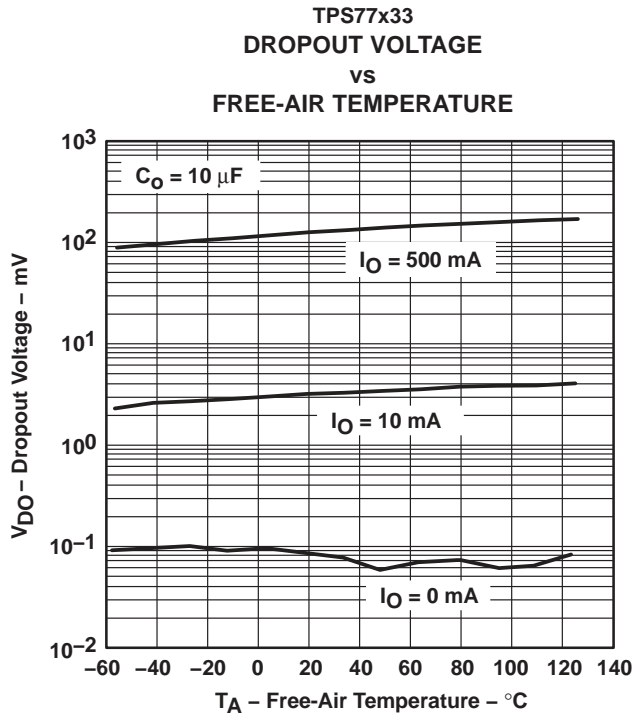


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**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
 TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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**AVAILABLE OPTIONST**

$T_J$	OUTPUT VOLTAGE (V)	PACKAGED DEVICES	
	TYP	TSSOP (PWP)	
–40°C to 125°C	3.3	TPS77533PWPQ1	TPS77633PWPQ1
	2.5	TPS77525PWPQ1	TPS77625PWPQ1
	2.8	—	TPS77628PWPQ1
	1.8	TPS77518PWPQ1	TPS77618PWPQ1
	1.6	TPS77516PWPQ1§	—
	1.5	TPS77515PWPQ1	TPS77615PWPQ1
	Adjustable† 1.2 V to 5.5 V	—	TPS77601PWPQ1
	Adjustable† 1.5 V to 5.5 V	TPS77501PWPQ1	—

† The TPS775xx has an open-drain power-on reset with a 200-ms delay function. The TPS776xx has an open-drain power good function.

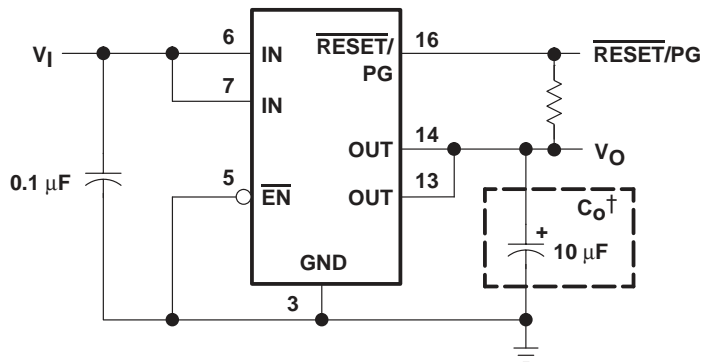
‡ The TPS77x01 is programmable using an external resistor divider (see application information). The PWP package is available taped and reeled. Add an R suffix to the device type (e.g., TPS77501QPWPRQ1).

§ TPS77516 is Product Preview.



**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
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 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

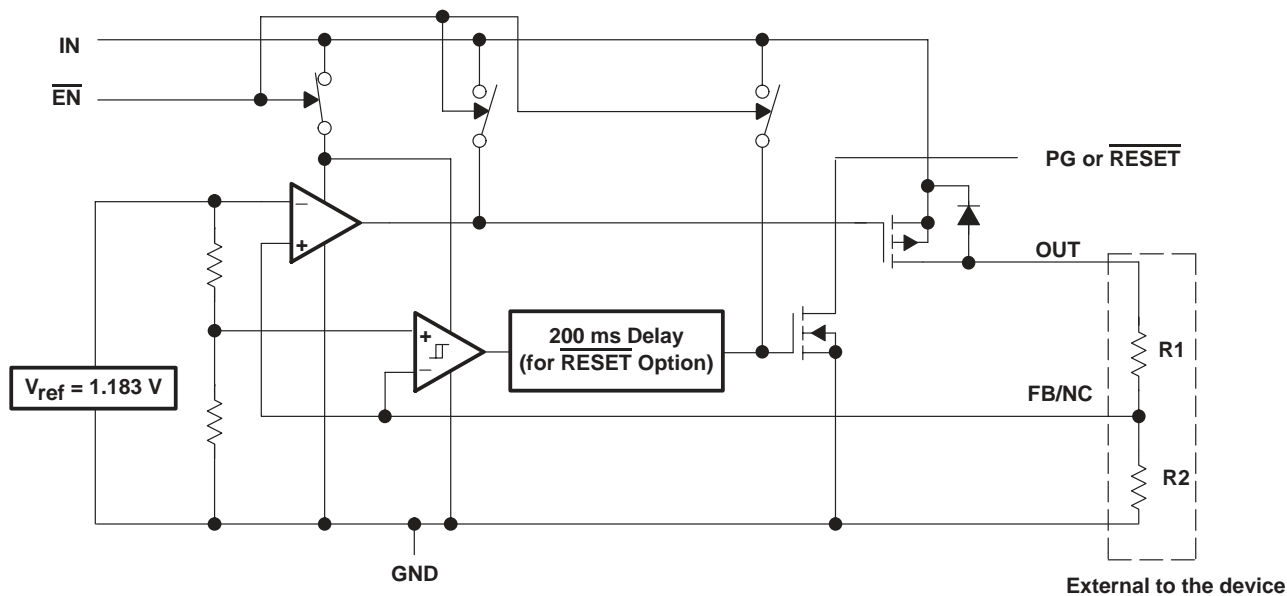
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† See application information section for capacitor selection details.

**Figure 1. Typical Application Configuration for Fixed Output Options**

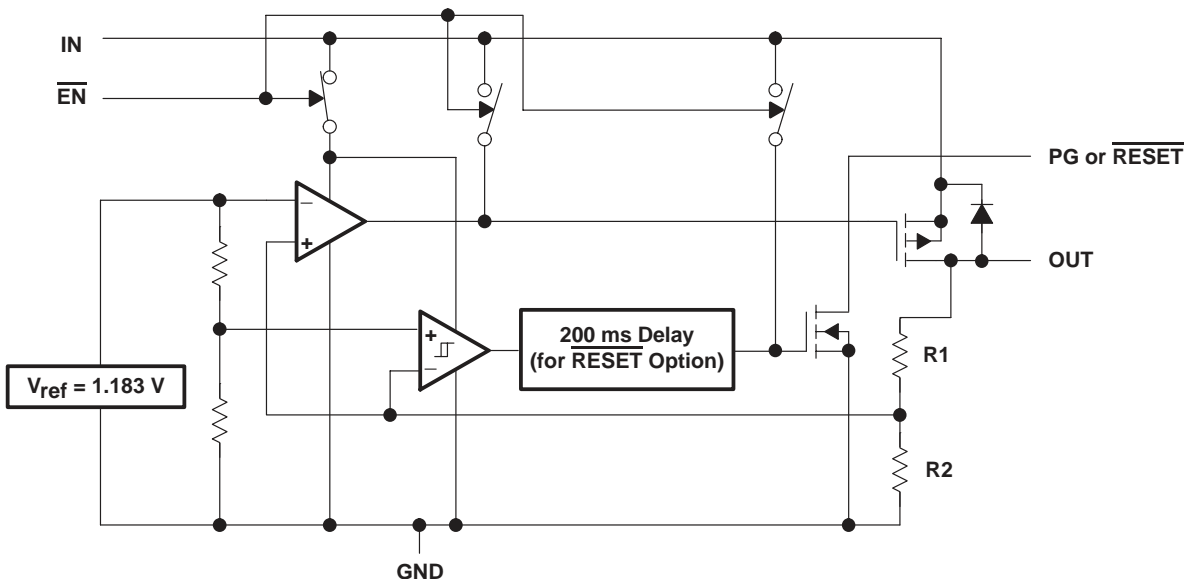
**functional block diagram—adjustable version**



**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
 TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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**functional block diagram—fixed-voltage version**



**Terminal Functions**

**TSSOP Package (TPS775xx)**

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
RESET	16	O	RESET output

**TSSOP Package (TPS776xx)**

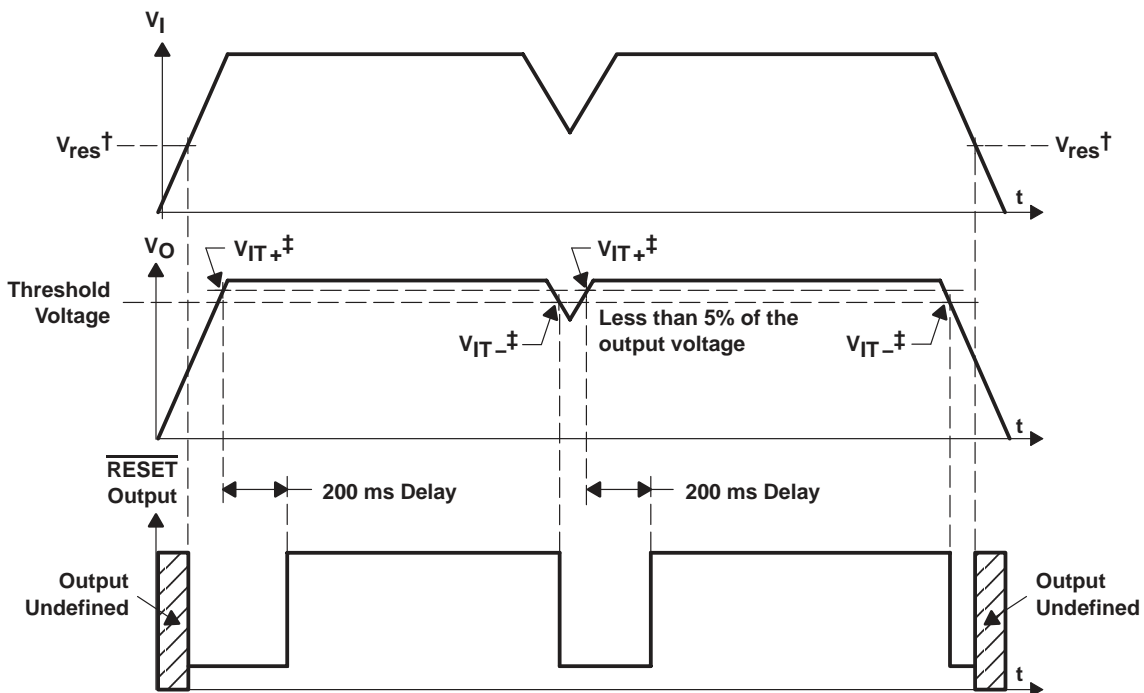
TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
PG	16	O	PG output



TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
 TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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TPS775xx RESET timing diagram



$^\dagger V_{res}$  is the minimum input voltage for a valid RESET. The symbol  $V_{res}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.

$^\ddagger V_{IT-}$  – Trip voltage is typically 5% lower than the output voltage ( $95\%V_O$ ).  $V_{IT-}$  to  $V_{IT+}$  is the hysteresis voltage.

**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT**  
**TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT**  
**FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Input voltage range‡, $V_I$ .....	-0.3 V to 13.5 V
Voltage range at EN .....	-0.3 V to 16.5 V
Maximum RESET voltage (TPS775xx) .....	16.5 V
Maximum PG voltage (TPS776xx) .....	16.5 V
Peak output current .....	Internally limited
Output voltage, $V_O$ (OUT, FB) .....	7 V
Continuous total power dissipation .....	See dissipation rating tables
Operating virtual junction temperature range, $T_J$ .....	-40°C to 125°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C
ESD rating, HBM .....	2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

**DISSIPATION RATING TABLE – FREE-AIR TEMPERATURES**

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP§	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP¶	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

§ This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in<sup>2</sup>).

¶ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in<sup>2</sup>) and layers 3 and 6 at 100% coverage (6 in<sup>2</sup>). For more information, refer to T1 technical brief SLMA002.

**recommended operating conditions**

	MIN	MAX	UNIT	
Input voltage, $V_I$ #	2.7	10	V	
Output voltage range, $V_O$	TPS77501	1.5	5.5	V
	TPS77601	1.2	5.5	
Output current, $I_O$ (see Note 1)	0	500	mA	
Operating virtual junction temperature, $T_J$ (see Note 1)	-40	125	°C	

# To calculate the minimum input voltage for your maximum output current, use the following equation:  $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$ .

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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electrical characteristics over recommended operating free-air temperature range,  
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$ ,  $I_O = 1 \text{ mA}$ ,  $\overline{\text{EN}} = 0 \text{ V}$ ,  $C_O = 10 \mu\text{F}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 $\mu\text{A}$ to 500 mA load) (see Note 2)	TPS77501	$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$ , $T_J = 25^\circ\text{C}$		$V_O$		V
		$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$	$0.98V_O$	$1.02V_O$		
	TPS77601	$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$ , $T_J = 25^\circ\text{C}$		$V_O$		
		$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$	$0.98V_O$	$1.02V_O$		
	TPS77x15	$T_J = 25^\circ\text{C}$ , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.5		
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.470	1.530		
	TPS77516	$T_J = 25^\circ\text{C}$ , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.6		
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.568	1.632		
	TPS77x18	$T_J = 25^\circ\text{C}$ , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.8		
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.764	1.836		
	TPS77x25	$T_J = 25^\circ\text{C}$ , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.5		
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.450	2.550		
	TPS77628	$T_J = 25^\circ\text{C}$ , $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.8		
		$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.744	2.856		
	TPS77x33	$T_J = 25^\circ\text{C}$ , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		3.3		
$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		3.234	3.366			
Quiescent current (GND current) $\overline{\text{EN}} = 0 \text{ V}$ , (see Note 2)		$10 \mu\text{A} < I_O < 500 \text{ mA}$ , $T_J = 25^\circ\text{C}$		85		$\mu\text{A}$
		$I_O = 500 \text{ mA}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$		125		
Output voltage line regulation ( $\Delta V_O/V_O$ ) (see Notes 2 and 3)		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$ , $T_J = 25^\circ\text{C}$		0.01		%/V
Load regulation				3		mV
Output noise voltage (TPS77x18)		$\text{BW} = 200 \text{ Hz}$ to $100 \text{ kHz}$ , $I_C = 500 \text{ mA}$ $C_O = 10 \mu\text{F}$ , $T_J = 25^\circ\text{C}$		53		$\mu\text{V}_{\text{rms}}$
Output current limit		$V_O = 0 \text{ V}$		1.7	2	A
Thermal shutdown junction temperature				150		$^\circ\text{C}$
Standby current		$\overline{\text{EN}} = V_I$ , $T_J = 25^\circ\text{C}$ , $2.7 \text{ V} < V_I < 10 \text{ V}$		1		$\mu\text{A}$
		$\overline{\text{EN}} = V_I$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ $2.7 \text{ V} < V_I < 10 \text{ V}$			10	$\mu\text{A}$
FB input current	TPS77x01	$\text{FB} = 1.5 \text{ V}$		2		nA
High level enable input voltage				1.7		V
Low level enable input voltage					0.9	V
Power supply ripple rejection (see Note 2)		$f = 1 \text{ KHz}$ , $C_O = 10 \mu\text{F}$ , $T_J = 25^\circ\text{C}$		60		dB

NOTES: 2. Minimum IN operating voltage is 2.7 V or  $V_{O(\text{typ})} + 1 \text{ V}$ , whichever is greater. Maximum IN voltage 10V.

3. If  $V_O \leq 1.8 \text{ V}$  then  $V_{\text{Imin}} = 2.7 \text{ V}$ ,  $V_{\text{Imax}} = 10 \text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{Imax}} - 2.7 \text{ V})}{100} \times 1000$$

If  $V_O \geq 2.5 \text{ V}$  then  $V_{\text{Imin}} = V_O + 1 \text{ V}$ ,  $V_{\text{Imax}} = 10 \text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{Imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$



**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
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 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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**electrical characteristics over recommended operating free-air temperature range,  
 $V_I = V_{O(typ)} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{EN} = 0\text{ V}$ ,  $C_O = 10\text{ }\mu\text{F}$  (unless otherwise noted) (continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reset (TPS775xx)	Minimum input voltage for valid RESET	$I_O(\text{RESET}) = 300\text{ }\mu\text{A}$		1.1		V
	Trip threshold voltage	$V_O$ decreasing	92		98	% $V_O$
	Hysteresis voltage	Measured at $V_O$		0.5		% $V_O$
	Output low voltage	$V_I = 2.7\text{ V}$ , $I_O(\text{RESET}) = 1\text{ mA}$		0.15	0.4	V
	Leakage current	$V(\text{RESET}) = 5\text{ V}$			1	$\mu\text{A}$
	RESET time-out delay			200		ms
PG (TPS776xx)	Minimum input voltage for valid PG	$I_O(\text{PG}) = 300\text{ }\mu\text{A}$		1.1		V
	Trip threshold voltage	$V_O$ decreasing	92		98	% $V_O$
	Hysteresis voltage	Measured at $V_O$		0.5		% $V_O$
	Output low voltage	$V_I = 2.7\text{ V}$ , $I_O(\text{PG}) = 1\text{ mA}$		0.15	0.4	V
	Leakage current	$V(\text{PG}) = 5\text{ V}$			1	$\mu\text{A}$
Input current ( $\overline{EN}$ )		$\overline{EN} = 0\text{ V}$	-1	0	1	$\mu\text{A}$
		$\overline{EN} = V_I$	-1		1	
Dropout voltage (see Note 4)	TPS77628	$I_O = 500\text{ mA}$ , $T_J = 25^\circ\text{C}$		285		mV
		$I_O = 500\text{ mA}$ , $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			410	
	TPS77533	$I_O = 500\text{ mA}$ , $T_J = 25^\circ\text{C}$		169		
		$I_O = 500\text{ mA}$ , $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			287	
	TPS77633	$I_O = 500\text{ mA}$ , $T_J = 25^\circ\text{C}$		169		
		$I_O = 500\text{ mA}$ , $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			287	

NOTE 4:  $I_N$  voltage equals  $V_{O(typ)} - 100\text{ mV}$ ; TPS77x15, TPS77516, TPS77x18, and TPS77x25 dropout voltage limited by input voltage range limitations (i.e., TPS77x33 input voltage needs to drop to 3.2 V for purpose of this test).

**TYPICAL CHARACTERISTICS**

**Table of Graphs**

			FIGURE
$V_O$	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8
	Power supply ripple rejection	vs Frequency	9
	Output spectral noise density	vs Frequency	10
$Z_O$	Output impedance	vs Frequency	11
$V_{DO}$	Dropout voltage	vs Input voltage	12
		vs Free-air temperature	13
	Input voltage (min)	vs Output voltage	14
	Line transient response		15, 17
	Load transient response		16, 18
$V_O$	Output voltage	vs Time	19
	Equivalent series resistance (ESR)	vs Output current	21 – 24





TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
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TYPICAL CHARACTERISTICS

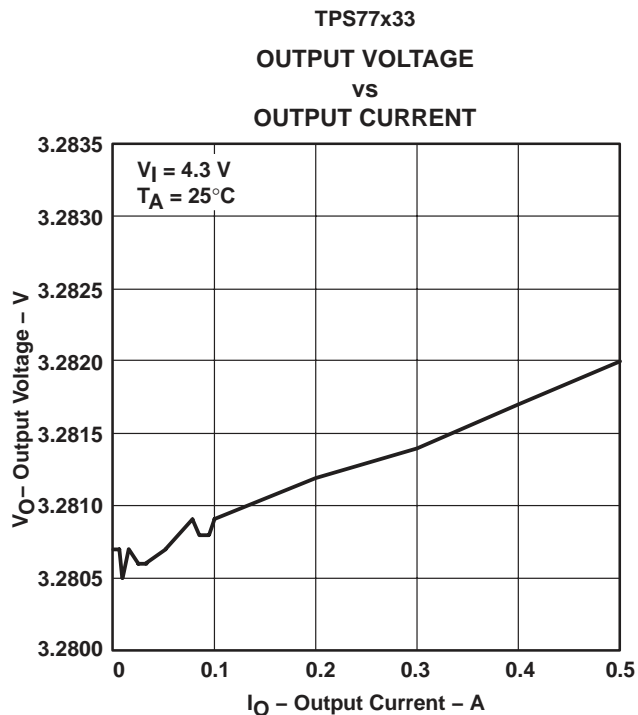


Figure 2

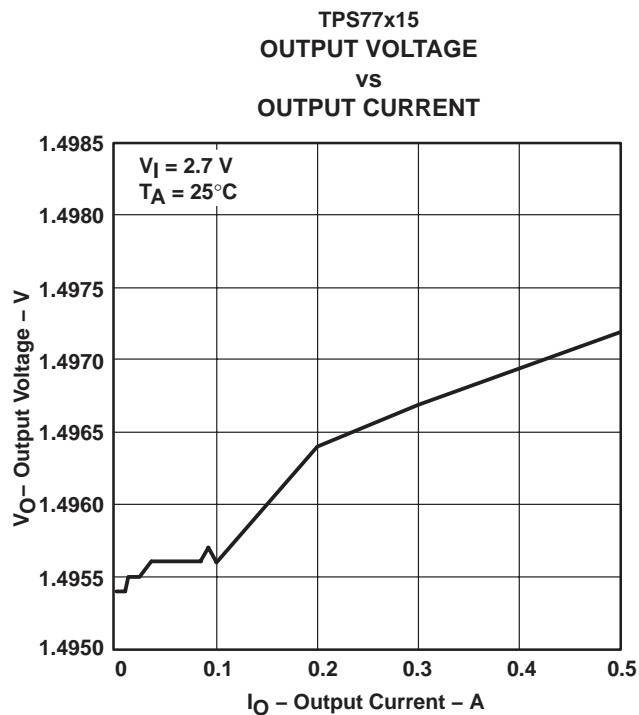


Figure 3

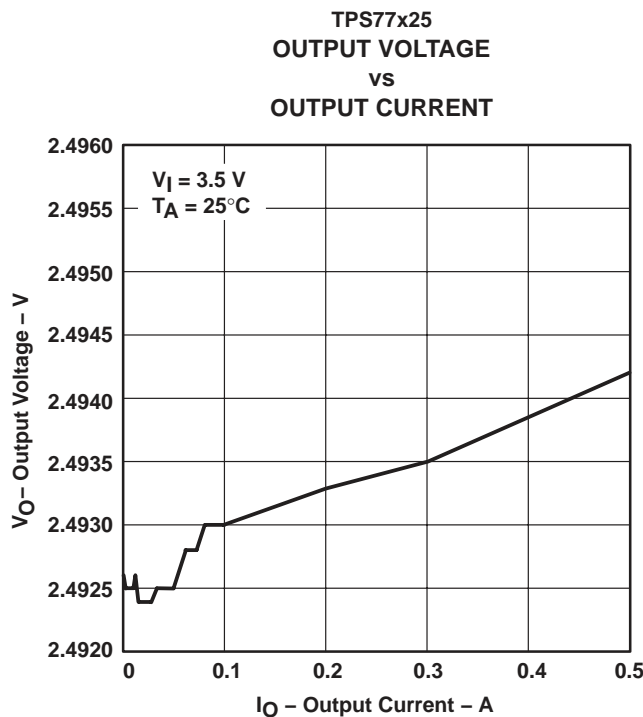


Figure 4

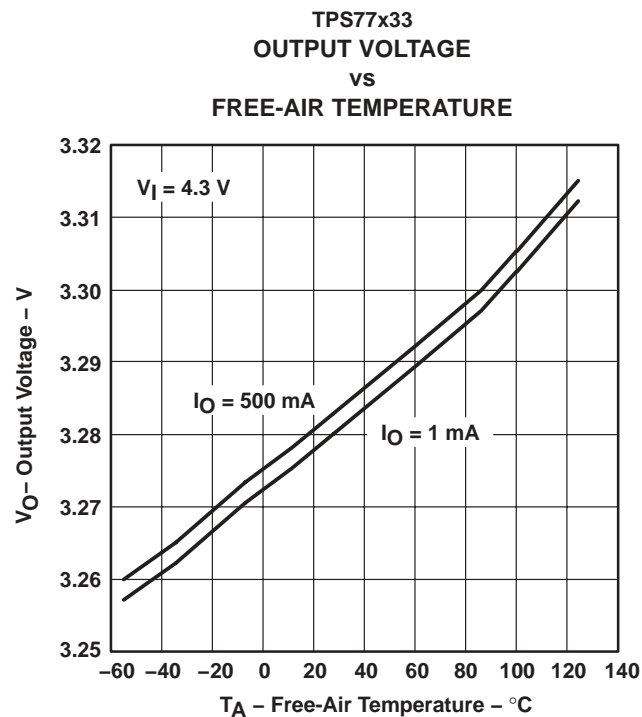


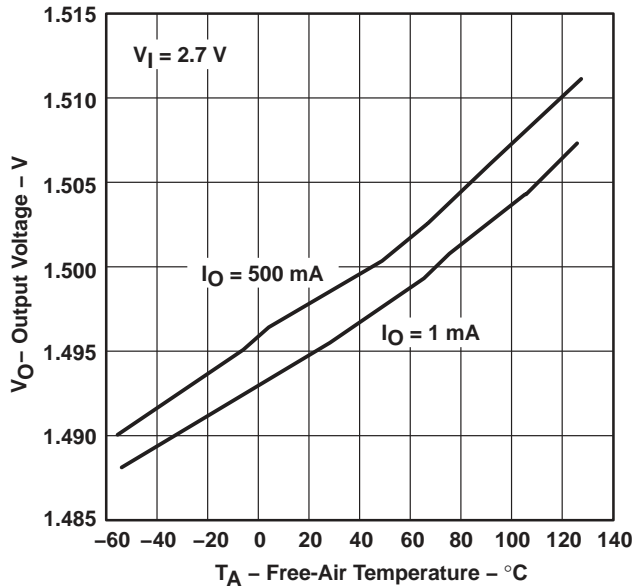
Figure 5

**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
 TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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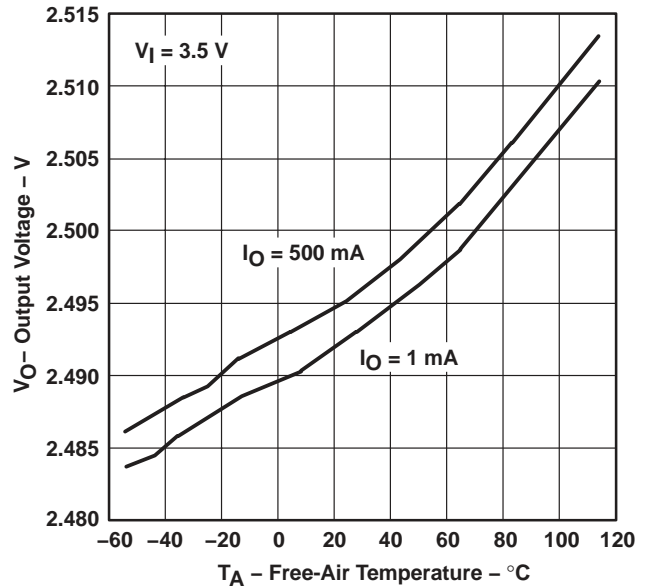
**TYPICAL CHARACTERISTICS**

**TPS77x15  
 OUTPUT VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE**



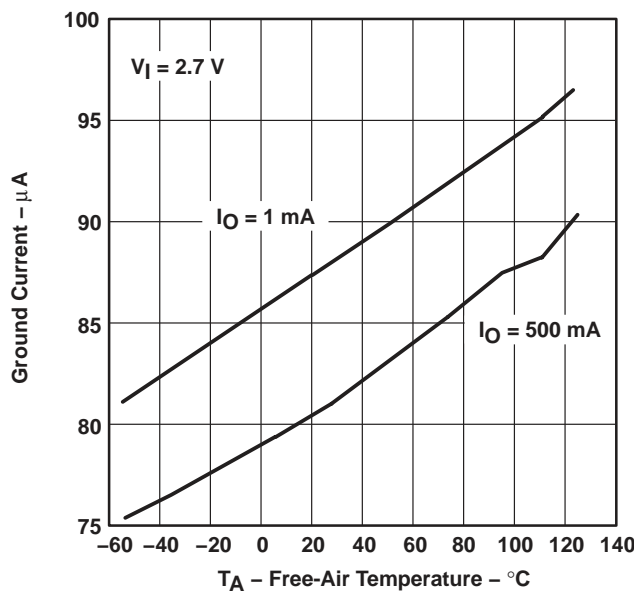
**Figure 6**

**TPS77x25  
 OUTPUT VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE**



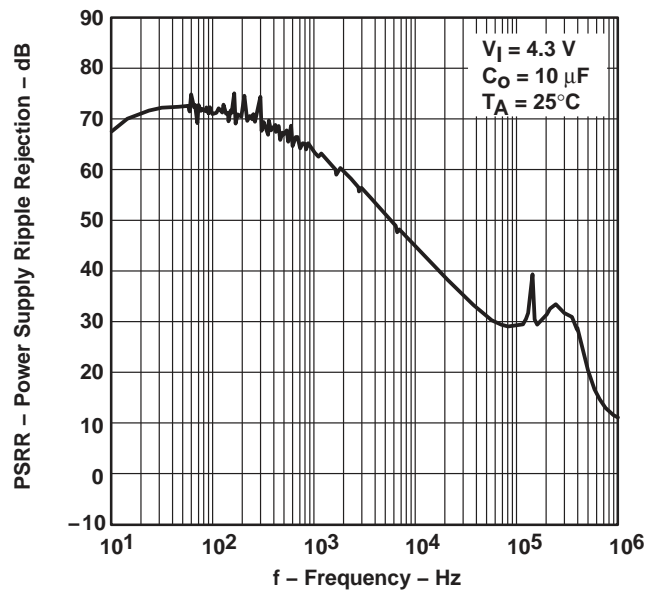
**Figure 7**

**TPS77xxx  
 GROUND CURRENT  
 vs  
 FREE-AIR TEMPERATURE**



**Figure 8**

**TPS77x33  
 POWER SUPPLY RIPPLE REJECTION  
 vs  
 FREQUENCY**



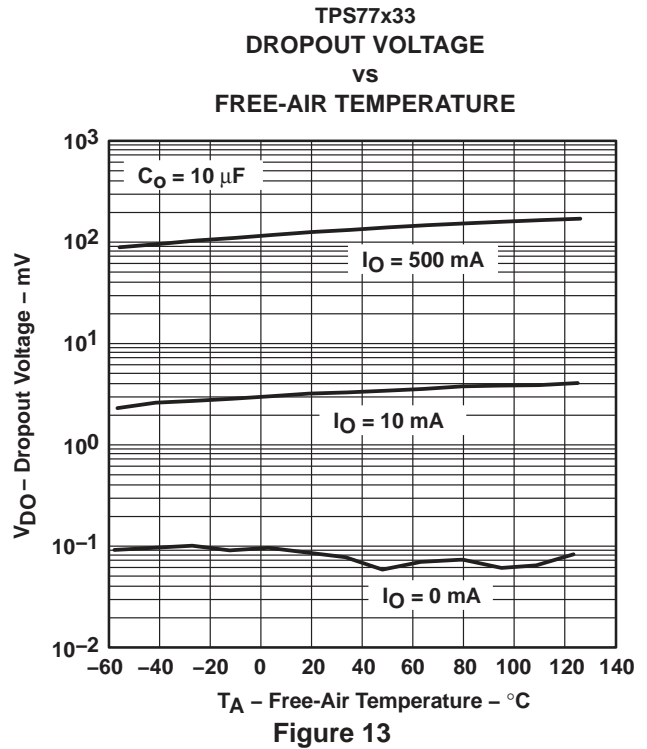
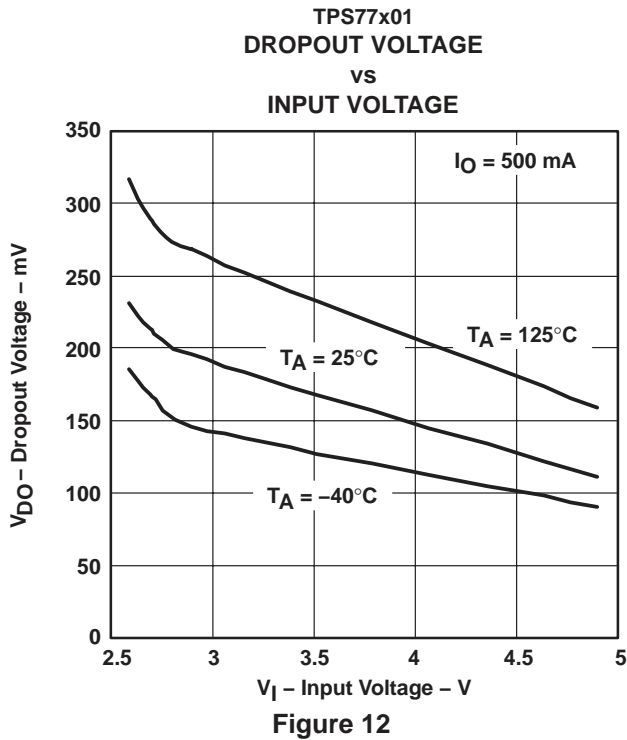
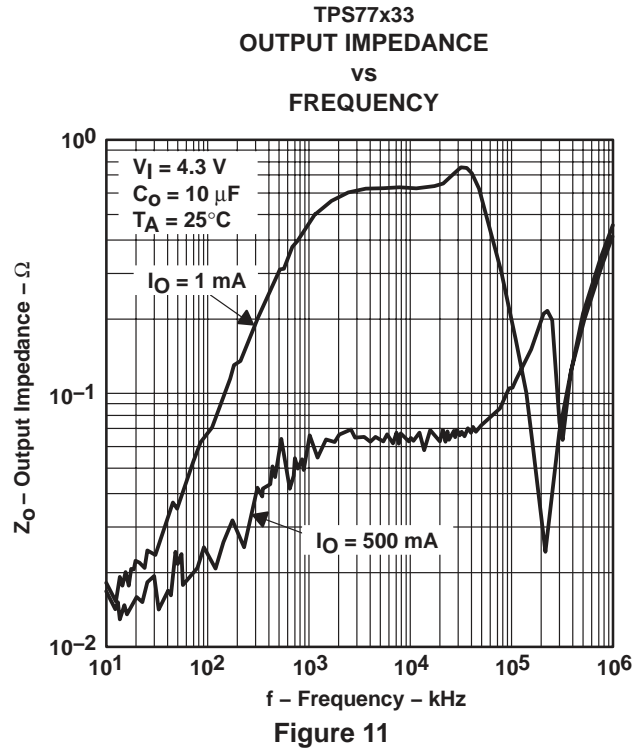
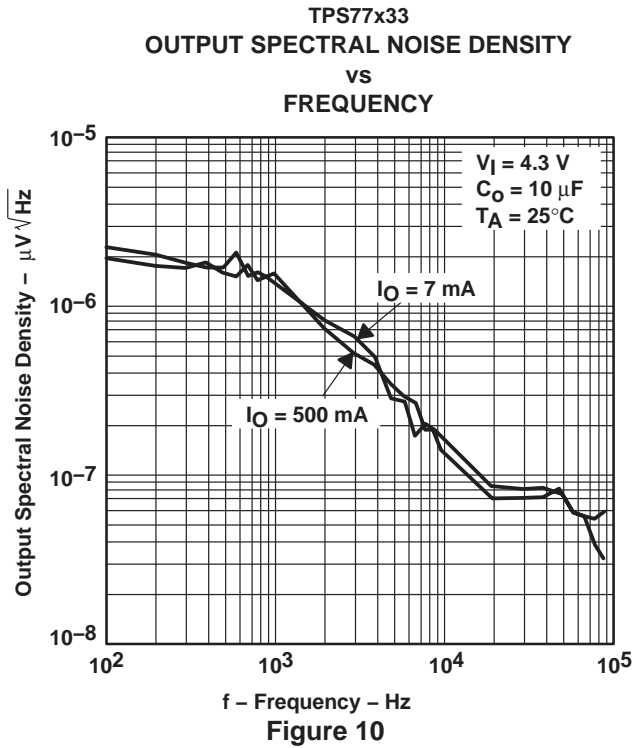
**Figure 9**



TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
 TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

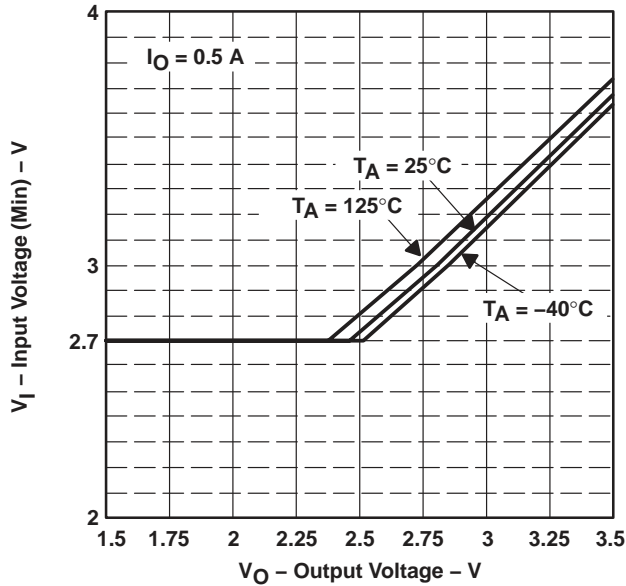


**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
 TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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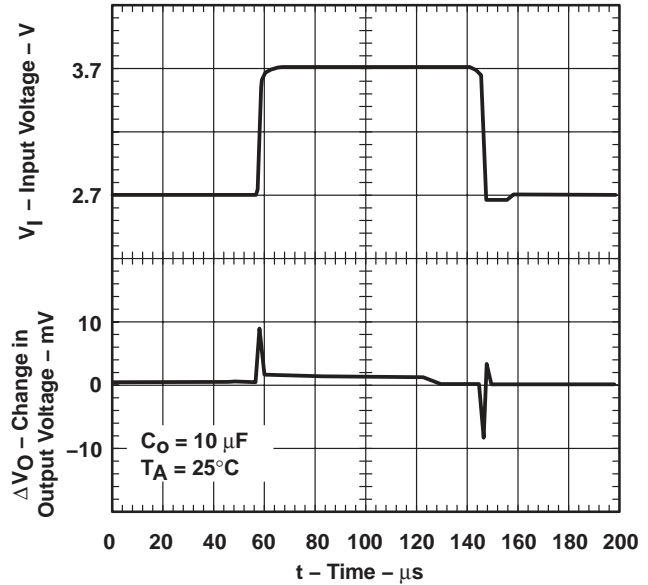
**TYPICAL CHARACTERISTICS**

**INPUT VOLTAGE (MIN)  
 vs  
 OUTPUT VOLTAGE**



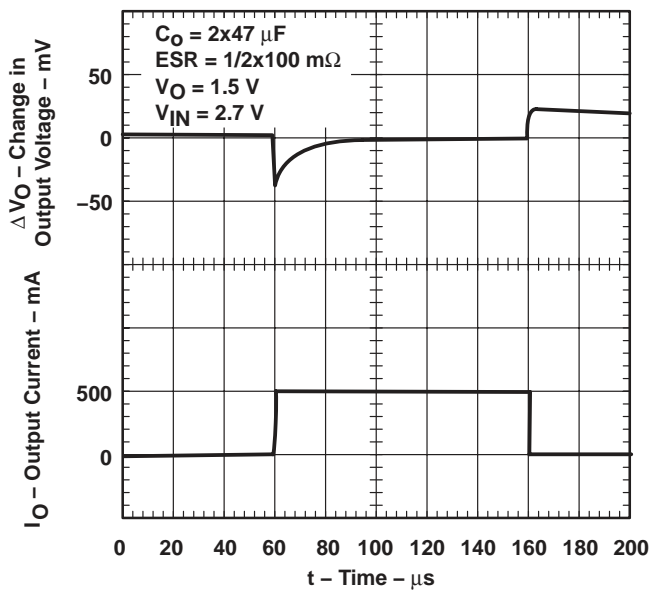
**Figure 14**

**TPS77x15  
 LINE TRANSIENT RESPONSE**



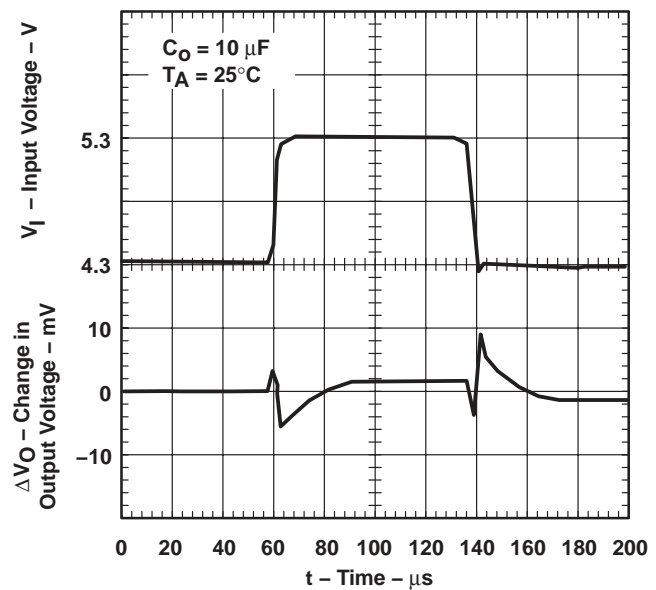
**Figure 15**

**TPS77x15  
 LOAD TRANSIENT RESPONSE**



**Figure 16**

**TPS77x33  
 LINE TRANSIENT RESPONSE**



**Figure 17**



TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
 TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

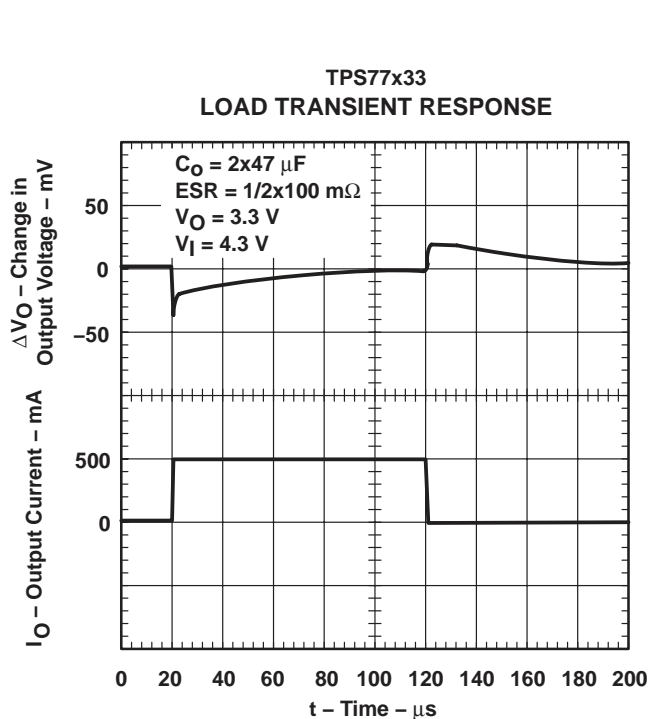


Figure 18

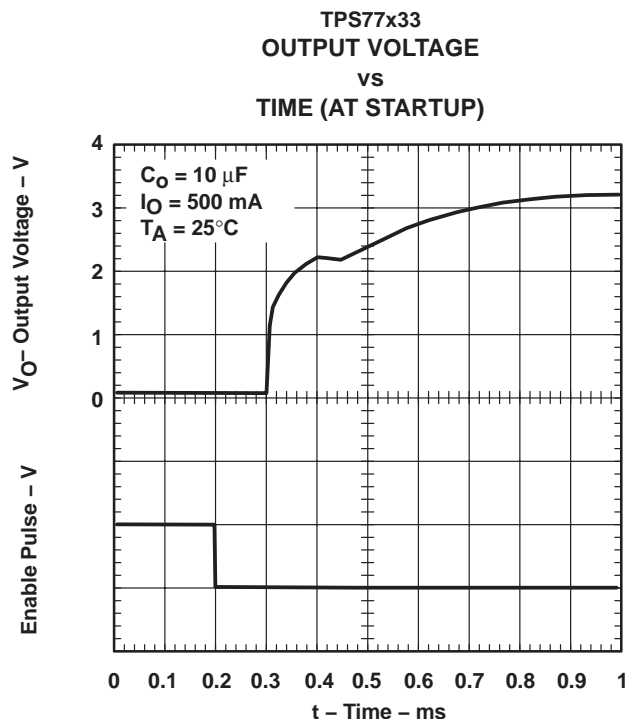


Figure 19

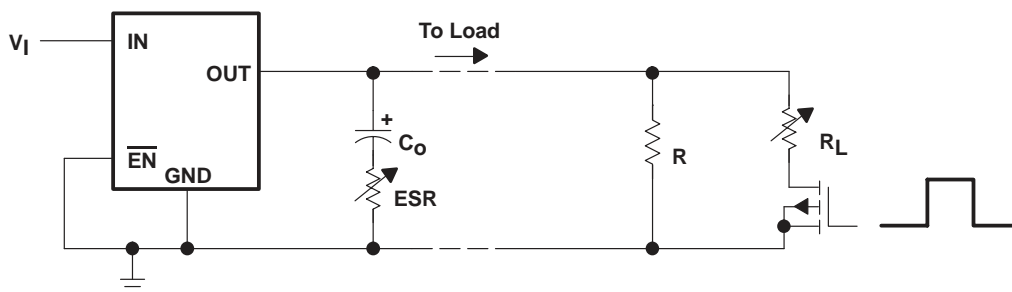


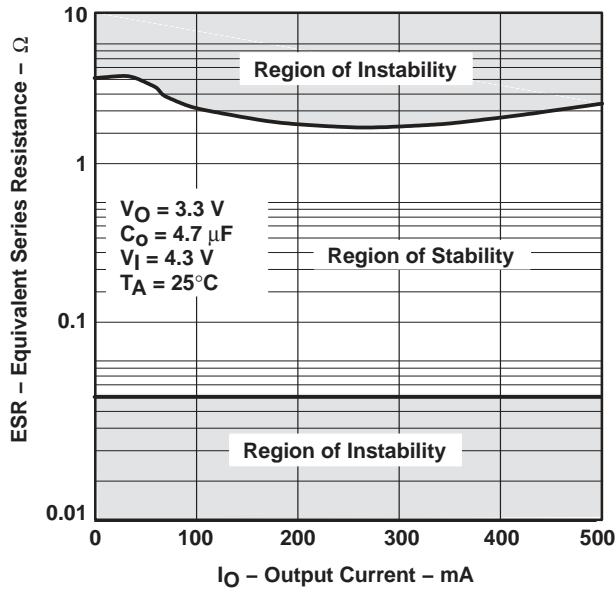
Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
 TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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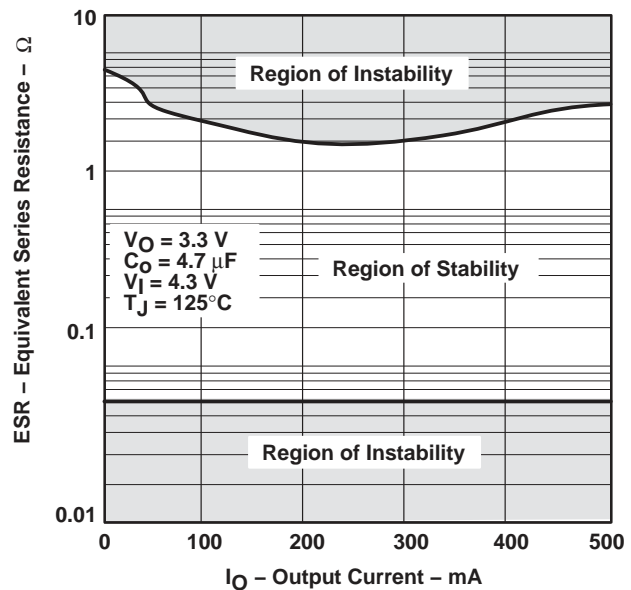
**TYPICAL CHARACTERISTICS**

**TYPICAL REGION OF STABILITY  
 EQUIVALENT SERIES RESISTANCE†  
 VS  
 OUTPUT CURRENT**



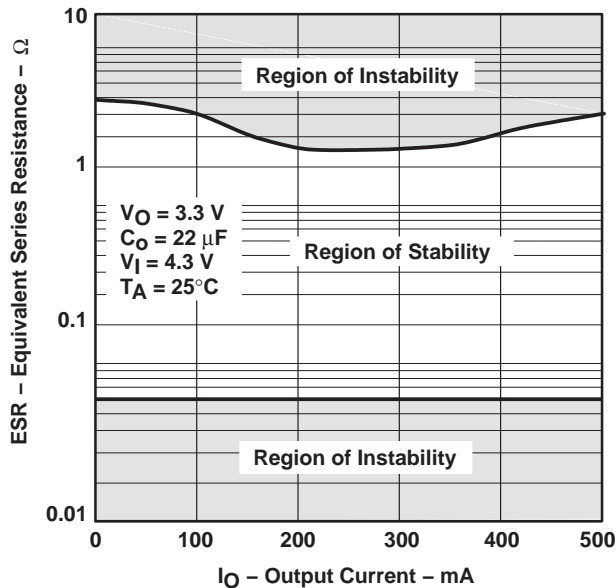
**Figure 21**

**TYPICAL REGION OF STABILITY  
 EQUIVALENT SERIES RESISTANCE†  
 VS  
 OUTPUT CURRENT**



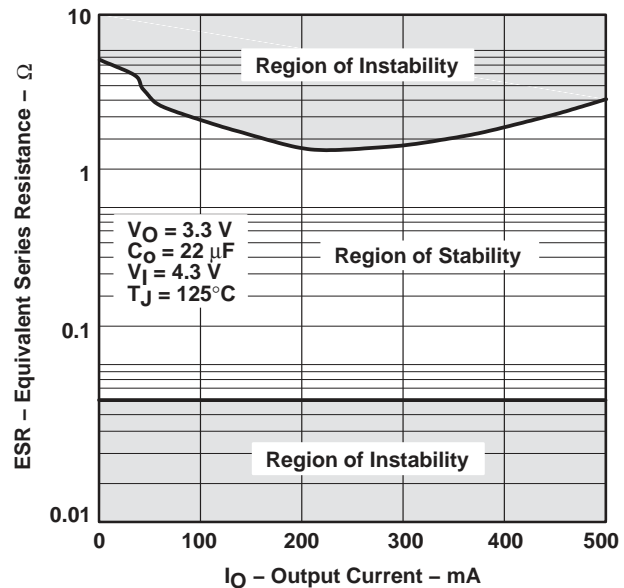
**Figure 22**

**TYPICAL REGION OF STABILITY  
 EQUIVALENT SERIES RESISTANCE†  
 VS  
 OUTPUT CURRENT**



**Figure 23**

**TYPICAL REGION OF STABILITY  
 EQUIVALENT SERIES RESISTANCE†  
 VS  
 OUTPUT CURRENT**



**Figure 24**

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C<sub>O</sub>.

# TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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## APPLICATION INFORMATION

The TPS775xx family includes five fixed-output voltage regulators (1.5 V, 1.6 V, 1.8 V, 2.5 V, and 3.3 V), and an adjustable regulator, the TPS77501 (adjustable from 1.5 V to 5.5 V).

The TPS776xx family includes five fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.8 V, and 3.3 V), and an adjustable regulator, the TPS77601 (adjustable from 1.2 V to 5.5 V).

### device operation

The TPS775xx and TPS776xx feature very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ( $I_B = I_C/\beta$ ). The TPS775xx and TPS776xx use a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in  $\beta$  forces an increase in  $I_B$  to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS775xx and TPS776xx quiescent currents remain low even when the regulator drops out, eliminating both problems.

The TPS775xx and TPS776xx families also feature a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2  $\mu$ A. If the shutdown feature is not used,  $\overline{EN}$  should be tied to ground.

### minimum load requirements

The TPS775xx and TPS776xx families are stable even at zero load; no minimum load is required for operation.

### FB—pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 26. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

### external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047  $\mu$ F or larger) improves load transient response and noise rejection if the TPS775xx or TPS776xx are located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS775xx and TPS776xx require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10  $\mu$ F and the ESR (equivalent series resistance) must be between 50 m $\Omega$  and 1.5  $\Omega$ . Capacitor values 10  $\mu$ F or larger are acceptable, provided the ESR is less than 1.5  $\Omega$ . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

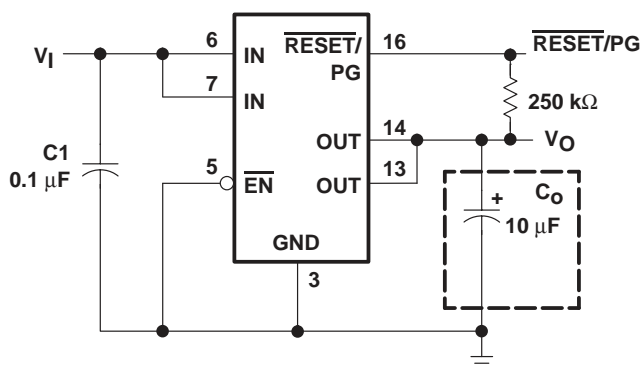


**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT**  
**TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT**  
**FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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**APPLICATION INFORMATION**

**external capacitor requirements (continued)**



**Figure 25. Typical Application Circuit (Fixed Versions)**

**programming the TPS77x01 adjustable LDO regulator**

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using:

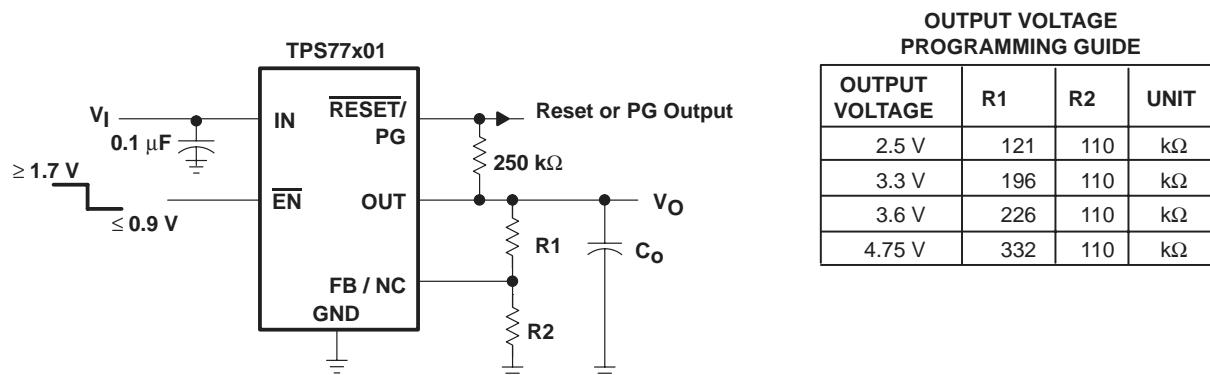
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 10-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 110 kΩ to set the divider current at approximately 10 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$



**Figure 26. TPS77x01 Adjustable LDO Regulator Programming**





**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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**APPLICATION INFORMATION**

**reset indicator**

The TPS775xx features a  $\overline{\text{RESET}}$  output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the  $\overline{\text{RESET}}$  output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating.  $\overline{\text{RESET}}$  can be used to drive power-on reset circuitry or as a low-battery indicator.  $\overline{\text{RESET}}$  does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

**power-good indicator**

The TPS776xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

**regulator protection**

The TPS775xx and TPS776xx PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS775xx and TPS776xx also feature internal current limiting and thermal protection. During normal operation, the TPS775xx and TPS776xx limit output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

**TPS77501-Q1, '515-Q1, '516-Q1, '518-Q1, '525-Q1, '533-Q1 WITH RESET OUTPUT  
TPS77601-Q1, '77615-Q1, '77618-Q1, '77625-Q1, '77628-Q1, '77633-Q1 WITH PG OUTPUT  
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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**APPLICATION INFORMATION**

**power dissipation and junction temperature**

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

$T_{Jmax}$  is the maximum allowable junction temperature.

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, i.e., 32.6°C/W for the 20-terminal PWP with no airflow.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS77501QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77515QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77518QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77525QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77533QPWPRQ1	ACTIVE	HTSSOP	PWP	20	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77601QPWPRG4Q1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77601QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77615QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77618QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77625QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS77633QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI

to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS77501-Q1, TPS77515-Q1, TPS77518-Q1, TPS77525-Q1, TPS77533-Q1, TPS77601-Q1, TPS77615-Q1, TPS77618-Q1, TPS77625-Q1, TPS77633-Q1 :**

- Catalog: [TPS77501](#), [TPS77515](#), [TPS77518](#), [TPS77525](#), [TPS77533](#), [TPS77601](#), [TPS77615](#), [TPS77618](#), [TPS77625](#), [TPS77633](#)
- Enhanced Product: [TPS77501-EP](#), [TPS77515-EP](#), [TPS77518-EP](#), [TPS77525-EP](#), [TPS77533-EP](#), [TPS77601-EP](#), [TPS77615-EP](#), [TPS77618-EP](#), [TPS77625-EP](#), [TPS77633-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS77501QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	77501Q1	<a href="#">Samples</a>
TPS77533QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	77533Q1	<a href="#">Samples</a>
TPS77601QPWPRG4Q1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	77601Q1	<a href="#">Samples</a>
TPS77601QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	77601Q1	<a href="#">Samples</a>
TPS77618QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	77618Q1	<a href="#">Samples</a>
TPS77633QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	77633Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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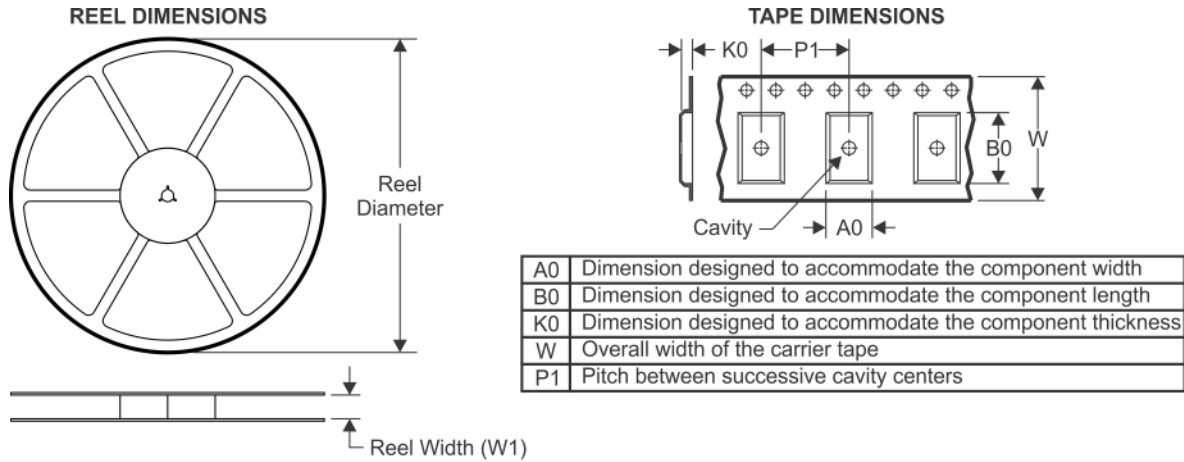
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**OTHER QUALIFIED VERSIONS OF TPS775-Q1, TPS776-Q1 :**

- Catalog: [TPS775](#), [TPS776](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77501QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77533QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77601QPWPRG4Q1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77601QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77618QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77633QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

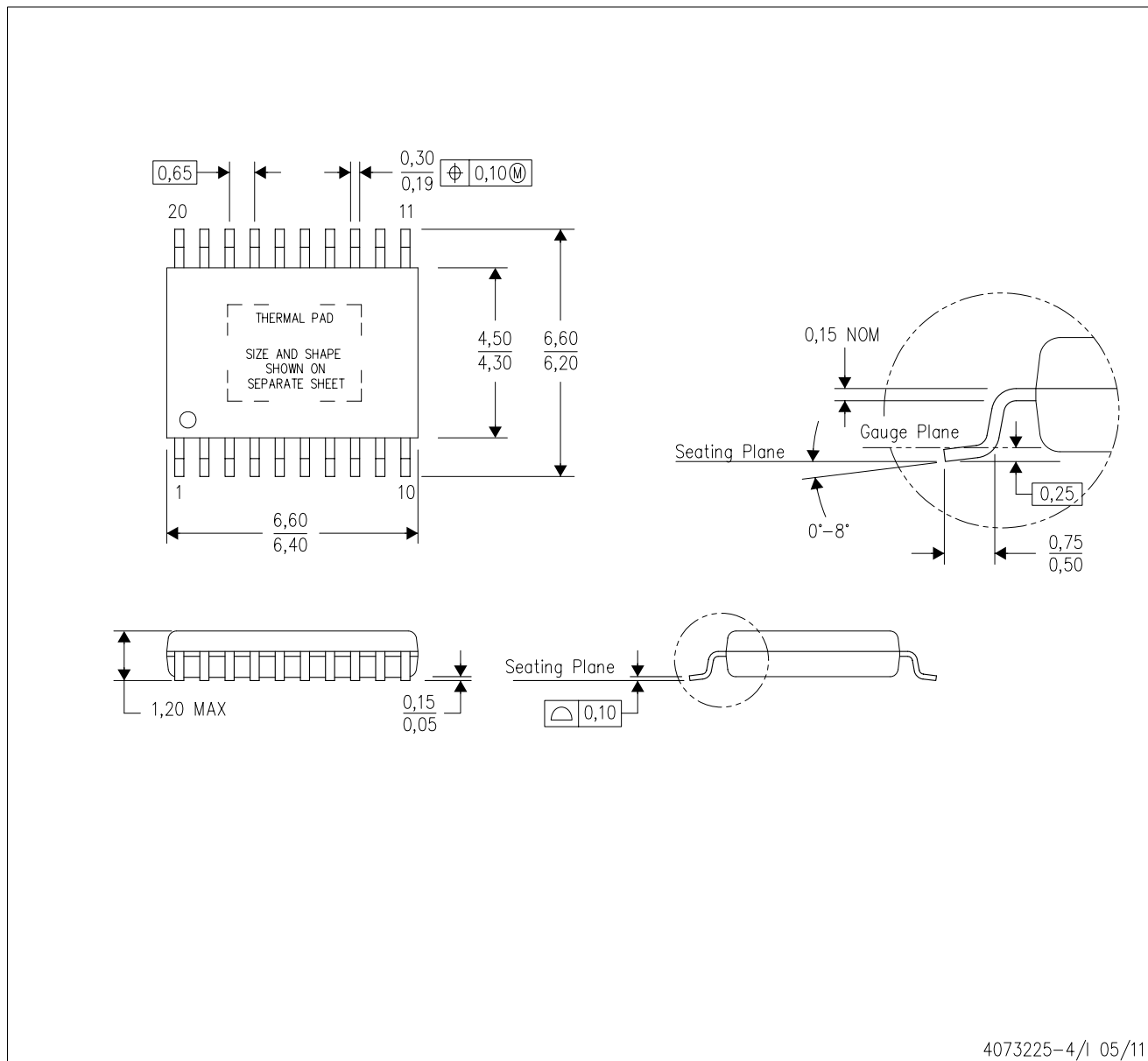
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77501QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77533QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77601QPWPRG4Q1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77601QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77618QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77633QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0



# MECHANICAL DATA

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

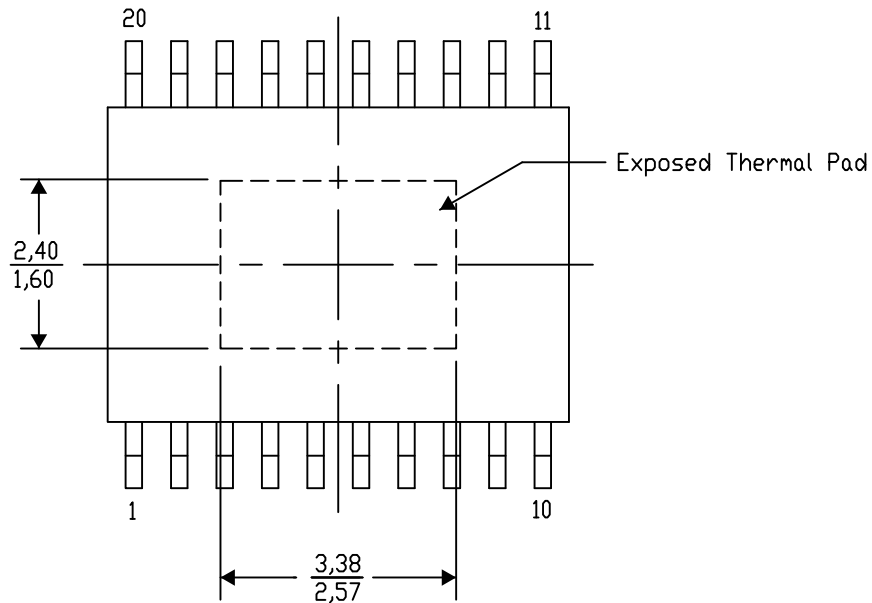
### PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

#### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

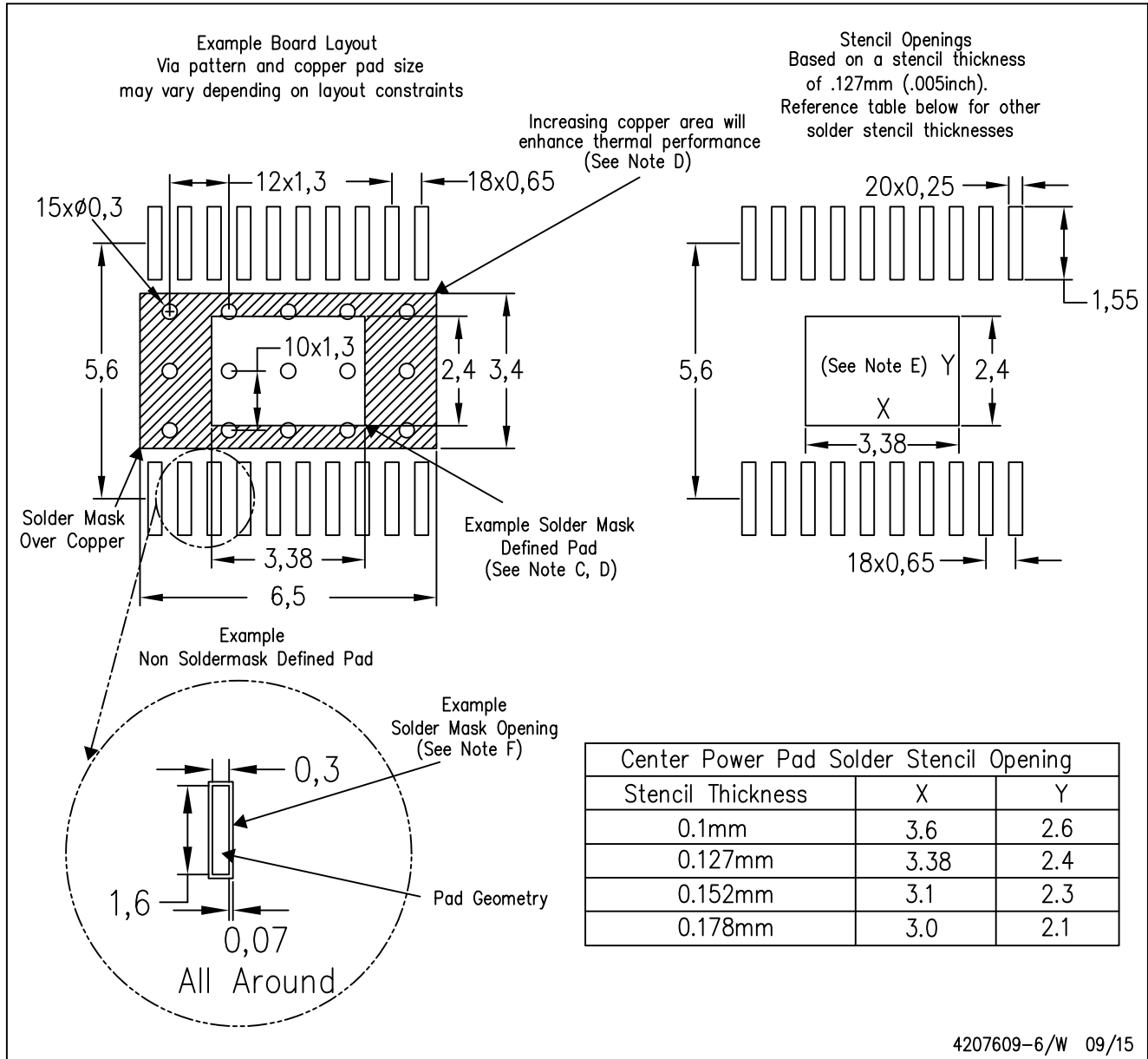
4206332-13/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

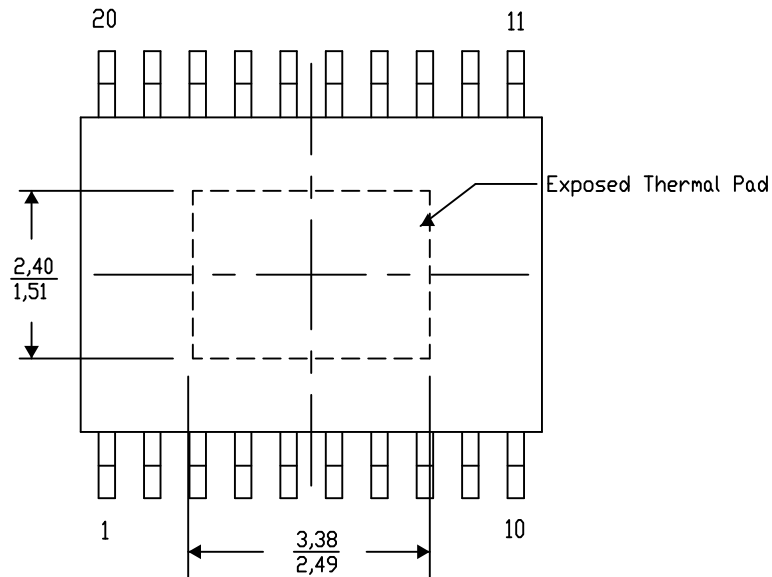
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-20/AO 01/16

NOTE: A. All linear dimensions are in millimeters

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# THERMAL PAD MECHANICAL DATA

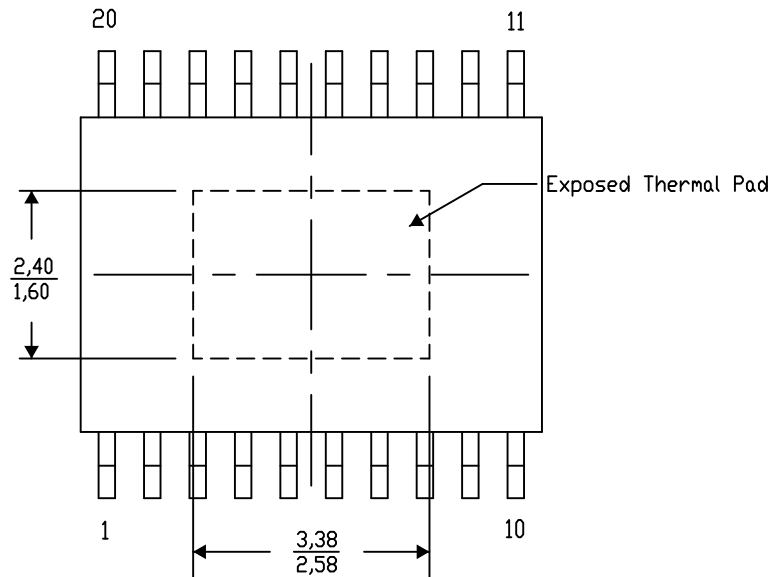
## PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206332-21/AO 01/16

NOTE: A. All linear dimensions are in millimeters

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## THERMAL PAD MECHANICAL DATA

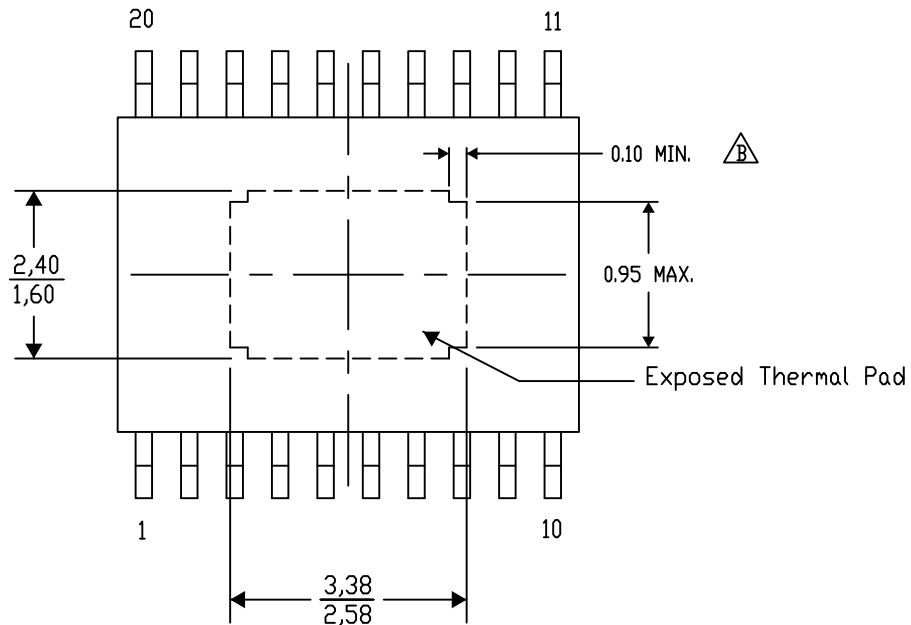
### PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

#### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-23/A0 01/16

NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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