To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

DATA SHEET

MOS FIELD EFFECT TRANSISTOR
NP82N06MLG, NP82N06NLG

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP82N06MLG and NP82N06NLG are N-channel MOS Field Effect Transistors designed for high current switching applications.

ORDERING INFORMATION

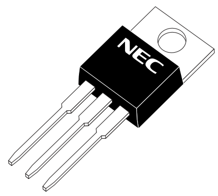
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP82N06MLG-S18-AY Note	Pure Sn (Tin)	Tube 50 p/tube	TO-220 (MP-25K) typ. 1.9 g
NP82N06NLG-S18-AY Note			TO-262 (MP-25SK) typ. 1.8 g

Note Pb-free (This product does not contain Pb in the external electrode.)

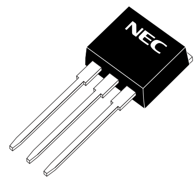
FEATURES

- Logic level
- Built-in gate protection diode
- Super low on-state resistance
  $R_{DS(on)1}$ = 7.4 mΩ MAX. (V_{GS} = 10 V, I_D = 41 A)
  $R_{DS(on)2}$ = 9.7 mΩ MAX. (V_{GS} = 5 V, I_D = 41 A)
- High current rating
  $I_{D(DC)}$ = ±82 A
- Low input capacitance
  C_{iss} = 5700 pF TYP.
- Designed for automotive application and AEC-Q101 qualified

(TO-220)



(TO-262)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±82	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±270	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	143	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	−55 to +175	°C
Repetitive Avalanche Current Note2	I_{AR}	37	A
Repetitive Avalanche Energy Note2	E_{AR}	137	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
2. T_{ch} ≤ 150°C, R_G = 25 Ω

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.05	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

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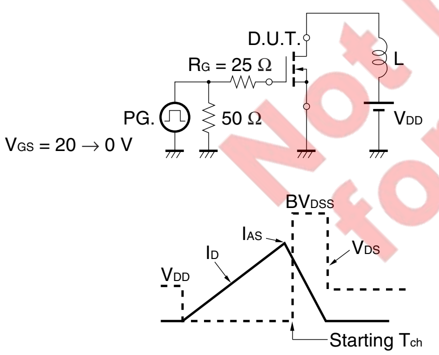
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

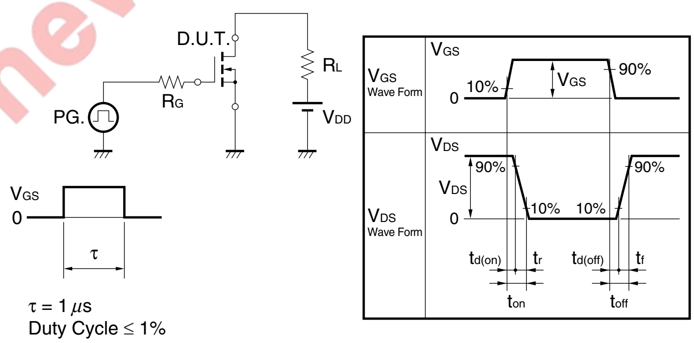
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5		2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 5 V, I_D = 41 A	19	68		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 41 A		5.9	7.4	mΩ
	$R_{DS(on)2}$	V_{GS} = 5 V, I_D = 41 A		6.7	9.7	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V,		5700	8550	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		420	630	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		275	500	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20 V, I_D = 41 A,		28	70	ns
Rise Time	t_r	V_{GS} = 10 V,		22	60	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		79	160	ns
Fall Time	t_f			9	30	ns
Total Gate Charge	Q_G	V_{DD} = 48 V,		106	160	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V,		29		nC
Gate to Drain Charge	Q_{GD}	I_D = 82 A		35		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 82 A, V_{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 82 A, V_{GS} = 0 V,		43		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		65		nC

Note Pulsed test

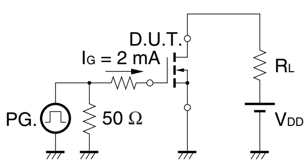
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

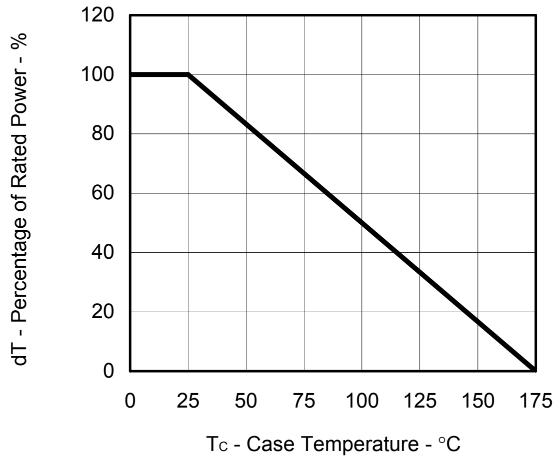


TEST CIRCUIT 3 GATE CHARGE

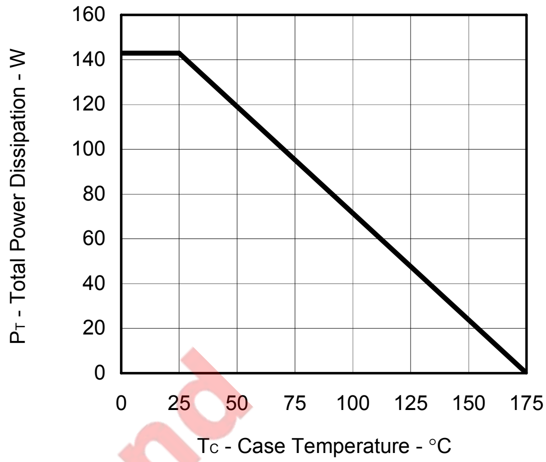


TYPICAL CHARACTERISTICS (T_A = 25°C)

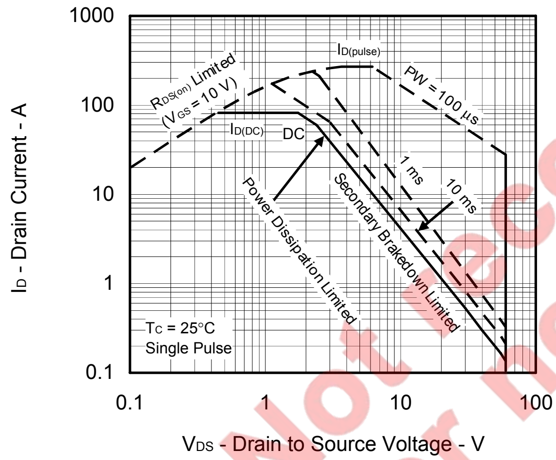
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



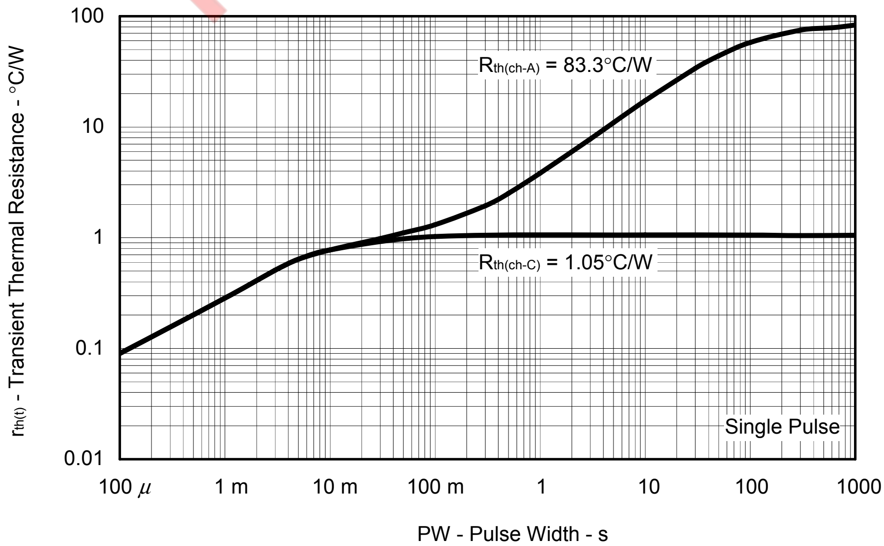
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



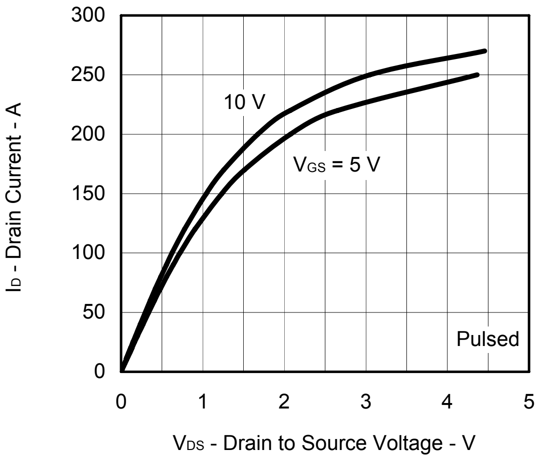
FORWARD BIAS SAFE OPERATING AREA



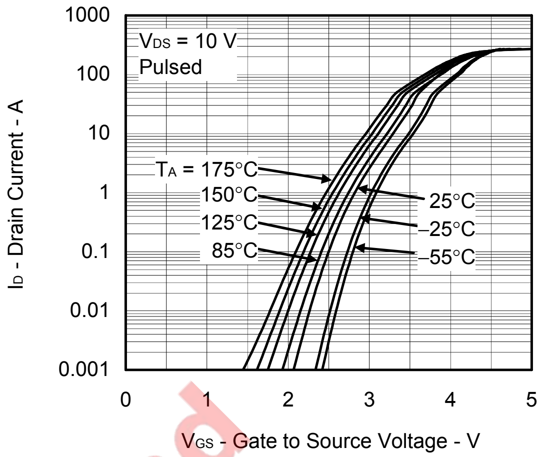
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



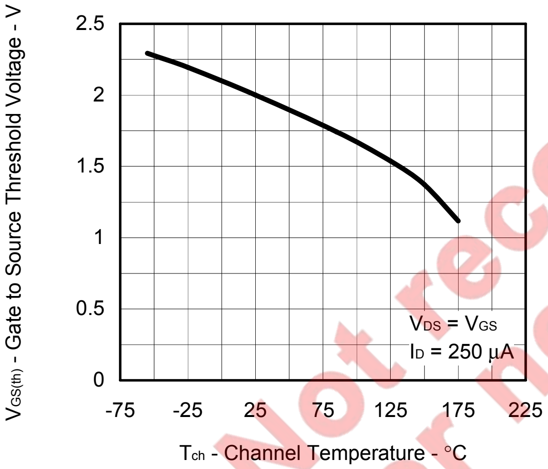
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



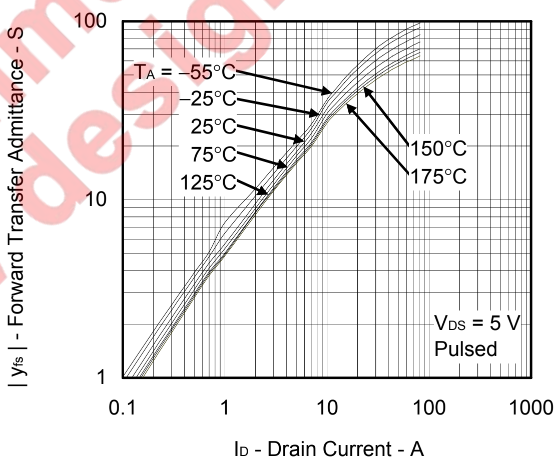
FORWARD TRANSFER CHARACTERISTICS



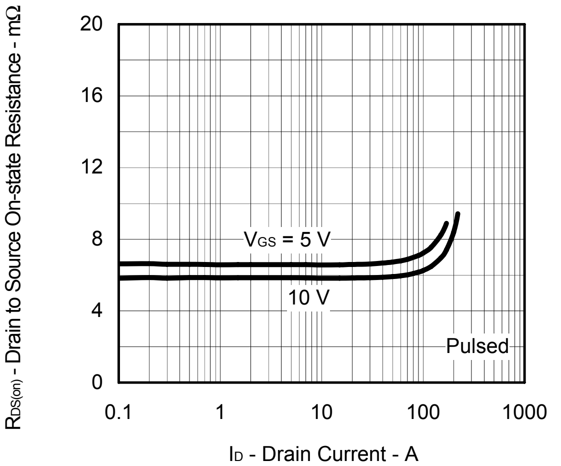
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



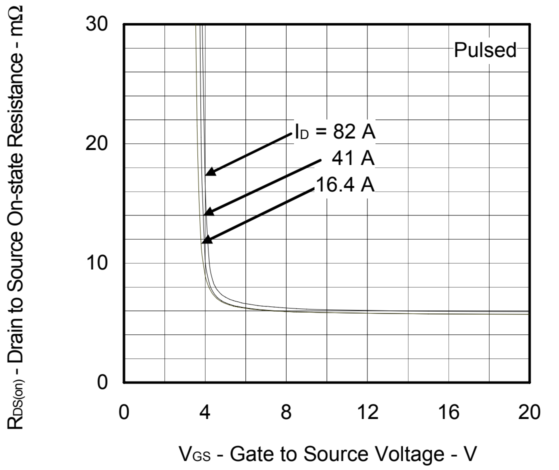
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



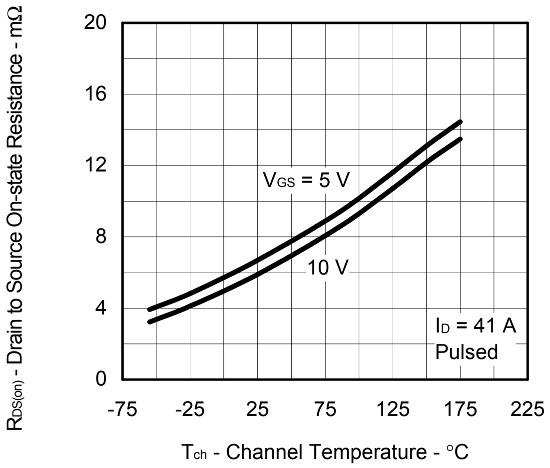
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



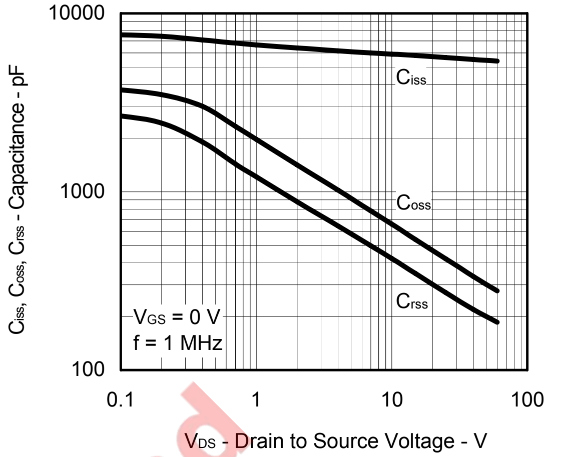
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



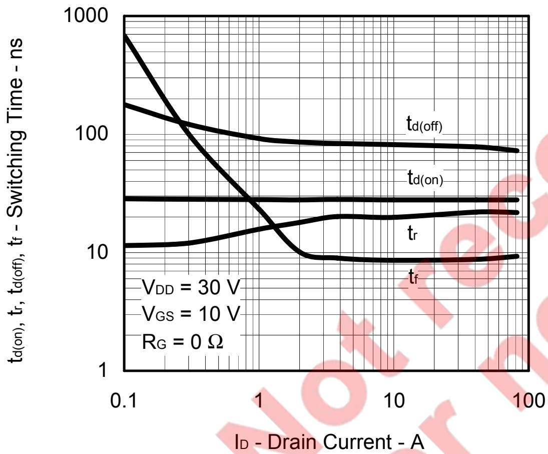
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



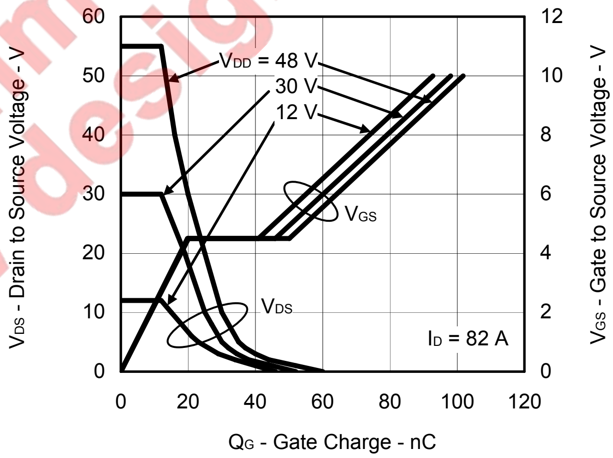
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



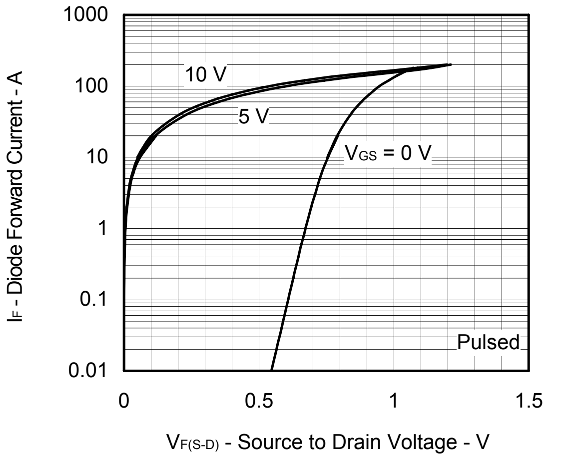
SWITCHING CHARACTERISTICS



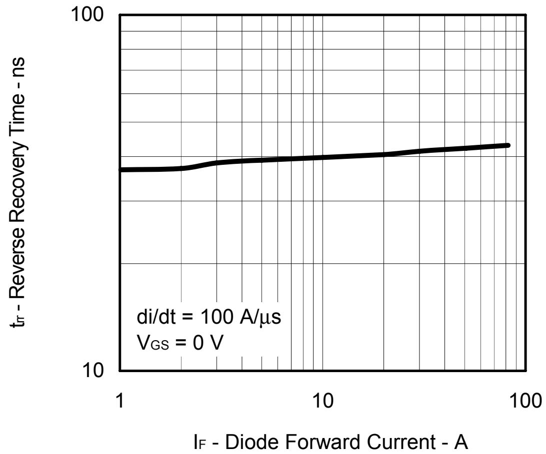
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

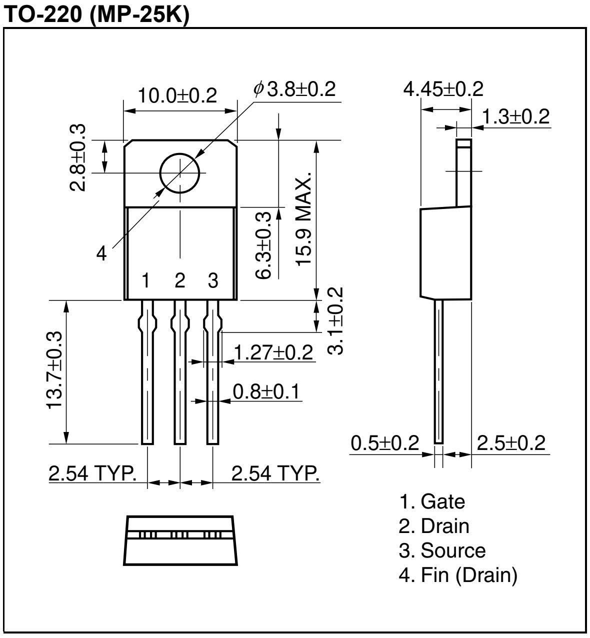


REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT

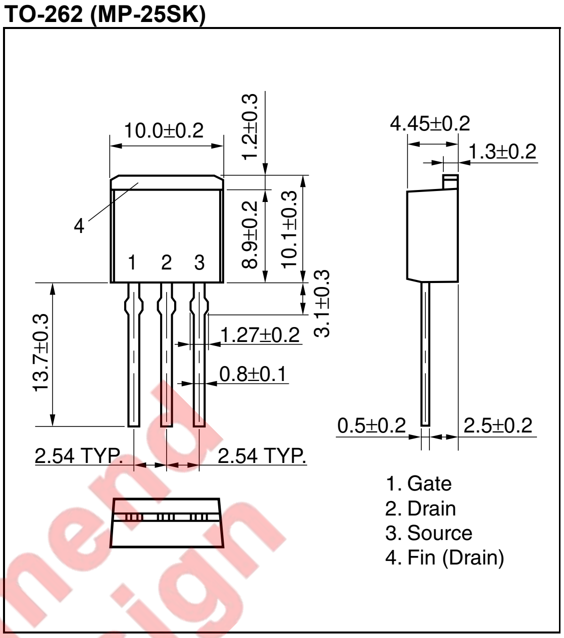


PACKAGE DRAWINGS (Unit: mm)

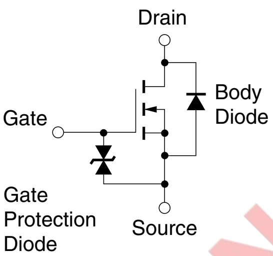
TO-220 (MP-25K)



TO-262 (MP-25SK)

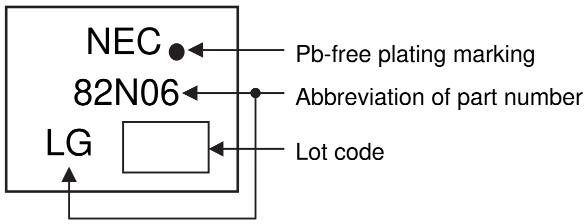


EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Wave soldering NP82N06MLG, NP82N06NLG	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating NP82N06MLG, NP82N06NLG	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).