

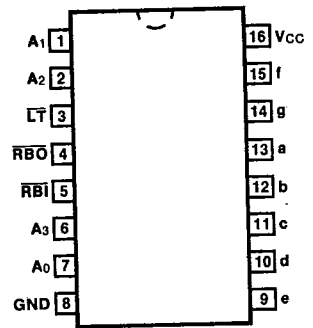
07

T-51-17

9307

7-SEGMENT DECODER

CONNECTION DIAGRAM PINOUT A



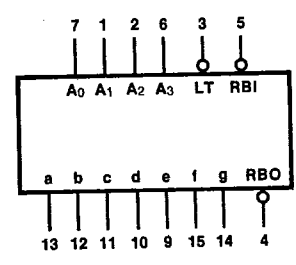
DESCRIPTION — The '07 7-segment decoder is designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a 7-segment numerical display. The decoder can be used with 7-segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays.

- AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING-EDGE ZEROES
- LAMP INTENSITY MODULATION CAPABILITY
- LAMP TEST FACILITY
- BLANKING INPUT
- ACTIVE HIGH OUTPUTS

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	9307PC		9B
Ceramic DIP (D)	A	9307DC	9307DM	6B
Flatpak (F)	A	9307FC	9307FM	4L

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
A ₀ — A ₃	BCD Inputs	0.25/1.0
RBI	Ripple Blanking Input (Active LOW)	0.25/0.5
LT	Lamp Test Input (Active LOW)	1.25/4.0
RBO	Ripple Blanking Output (Active LOW)	1.75/1.5
a — g	Segment Outputs (Active HIGH)	0/6.25

FUNCTIONAL DESCRIPTION — The '07 7-segment decoder accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a 7-segment matrix display used for representing the decimal numbers 0-9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in *Figure a*. The numeric designations chosen to represent the decimal numbers are shown in *Figure b*, together with the resulting displays for input code configurations in excess of binary nine.

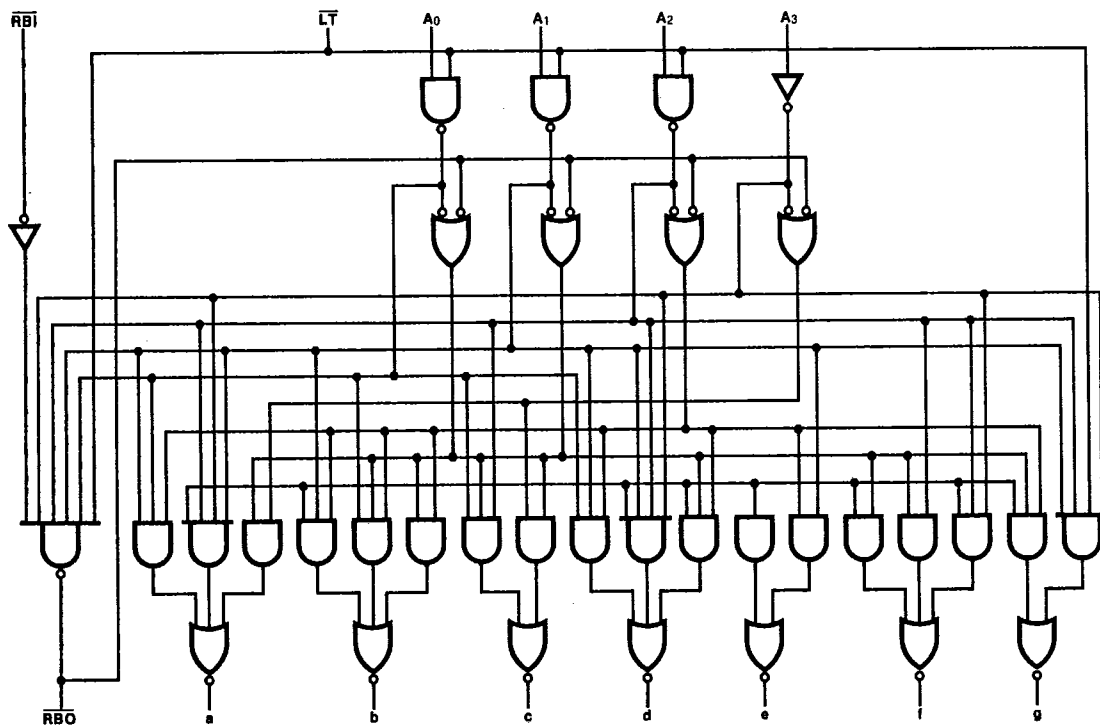
The decoder has active HIGH outputs so that a buffer transistor may be used directly to provide the high currents required for incandescent displays. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. The value of this resistor is constrained by the 10 mA current sinking capability of the output transistors of the circuit.

The device has provision for automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output (\overline{RBO}) of a decoder to the Ripple Blanking Input (\overline{RBI}) of the next lower stage device. The most significant decoder stage should have the \overline{RBI} input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the \overline{RBI} input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The \overline{RBO} terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL gates.

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LOGIC DIAGRAM



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TRUTH TABLE

INPUTS					OUTPUTS								
LT	RBI	A ₀	A ₁	A ₂	A ₃	a	b	c	d	e	f	g	RBO
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	0
H	X	H	L	L	L	L	H	H	L	L	L	L	1
H	X	L	H	L	L	H	H	L	H	H	L	H	2
H	X	H	H	L	L	H	H	H	H	L	L	H	3
H	X	L	L	H	L	L	H	H	L	L	L	H	4
H	X	H	L	H	L	H	L	H	H	L	H	H	5
H	X	L	H	H	L	H	L	H	H	H	H	H	6
H	X	H	H	H	L	H	H	H	L	L	L	H	7
H	X	L	L	L	H	H	H	H	H	H	H	H	8
H	X	H	L	L	H	H	H	H	L	H	H	H	9
H	X	L	H	L	H	L	L	L	H	H	L	H	10
H	X	H	H	L	H	L	L	L	H	L	L	H	11
H	X	L	L	H	H	L	H	H	L	L	H	H	12
H	X	H	L	H	H	H	L	H	H	L	H	H	13
H	X	L	H	H	H	L	L	L	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	H	15

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

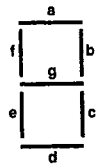


Fig. a Segment Designation

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Fig. b Numerical Designations

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX		UNITS	CONDITIONS
			Min	Max		
VOH	Output HIGH Voltage	at a-g	4.3		V	VCC = Min IOH = 0 mA
		at \overline{RBO}	XM XC	3.0 2.7	V	VCC = Min IOH = -70 μ A
VOL	Output LOW Voltage	at a-g	XM	0.4	V	IOL = 12.5 mA
			XC	0.45	V	IOL = 11.5 mA
		at \overline{RBO}	XM	0.4	V	IOL = 3.1 mA
			XC	0.45	V	IOL = 2.75 mA
		at a-g	XM	0.4	V	IOL = 10 mA
			XC	0.45	V	IOL = 10 mA
at \overline{RBO}	XM XC	0.4 0.45	V	IOL = 2.4 mA		
IA	Available Output Current at a-g	XM	-1.0	mA	VOUT = 0.85 V	
		XC	-1.1	mA	VOUT = 0.75 V	
IOS	Output Short Circuit Current at a-g	XM		mA	VCC = Max, TA = +25°C	
		XC		mA	VOUT = 0 V	
ICC	Power Supply Current	XM		mA	VCC = Max	
		XC		mA	VCC = Max	

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AC CHARACTERISTICS: VCC = +5.0 V, TA = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		93XX		UNITS	CONDITIONS
			CL = 30 pF			
			Min	Max		
tPLH tPHL	Propagation Delay A0 - A3 or \overline{RBI} to a-g or \overline{RBO}			750 750	ns	Fig. 3-20