



# PSMN3R3-40MLH

N-channel 40 V, 3.3 m $\Omega$ , logic level MOSFET in LFAK33 using NextPower-S3 technology

11 November 2019

Product data sheet

## 1. General description

118 A, logic level N-channel enhancement mode MOSFET in 175 °C LFAK33 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high efficiency applications at high switching frequencies.

## 2. Features and benefits

- Avalanche rated, 100% tested
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low  $Q_{rr}$ ,  $Q_G$  and  $Q_{GD}$  for high system efficiency, especially at high switching frequencies
- Low spiking and ringing for low EMI designs
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

## 3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Brushless DC motor drive
- LED lighting

## 4. Quick reference data

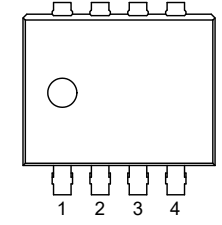
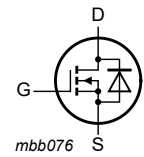
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	118	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	101	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	2.7	3.3	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	3.4	4.2	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	1.2	4	8	nC
$Q_{G(tot)}$	total gate charge		11	17	24	nC

[1] 118A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK33 (SOT1210)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R3-40MLH	LPAK33	Plastic, single ended surface mounted package (LPAK33); 8 leads; 0.65 mm pitch	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R3-40MLH	3H3L40

## 8. Limiting values

Table 5. Limiting values

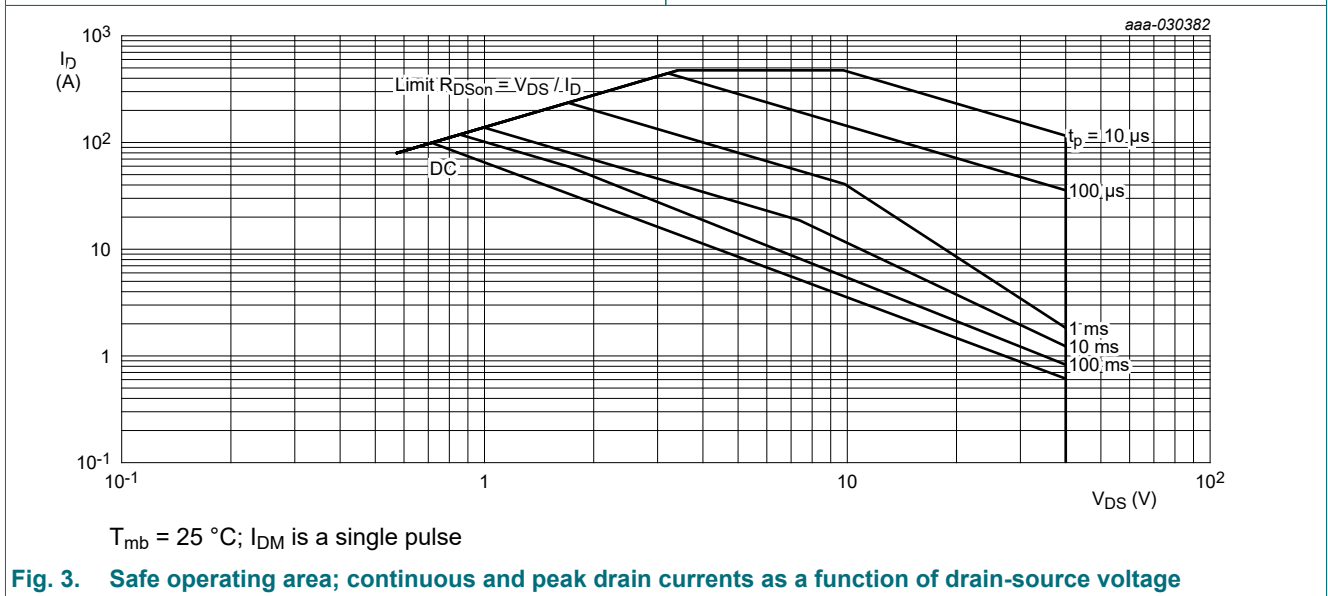
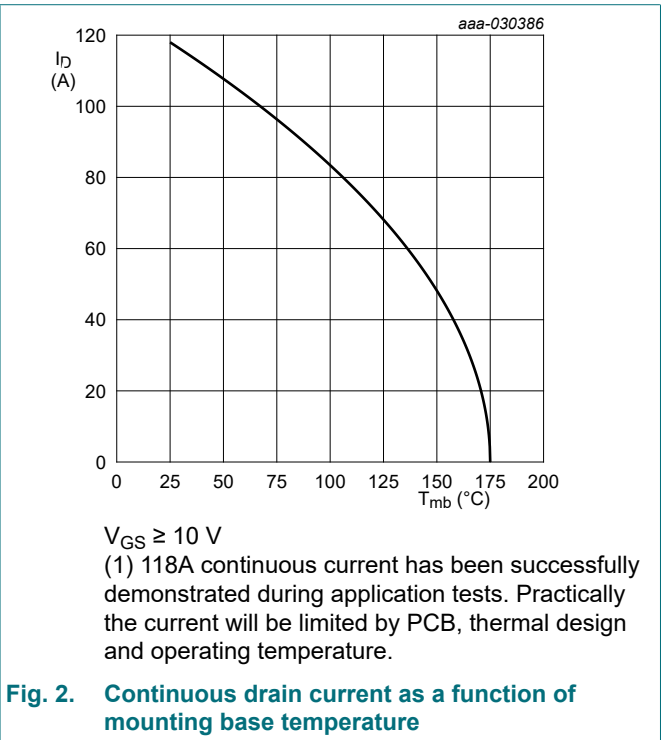
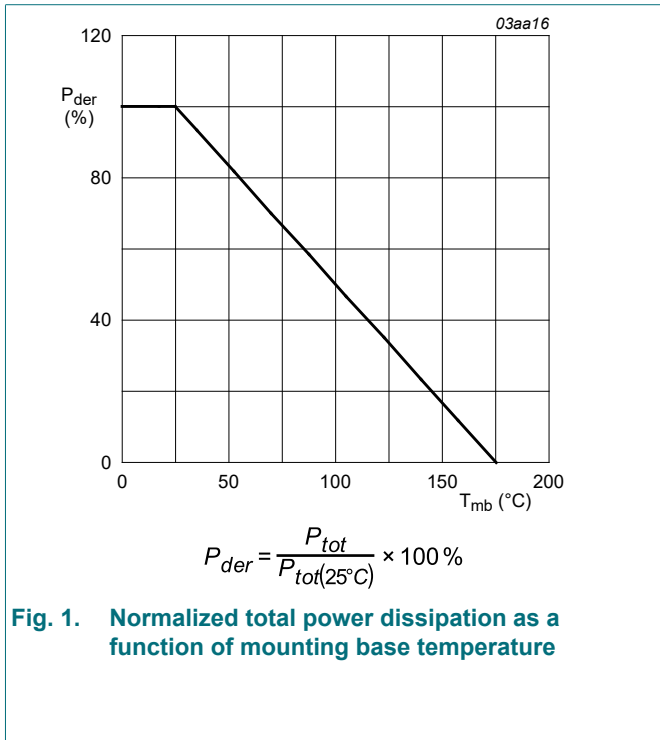
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
$V_{DSM}$	peak drain-source voltage	$t_p \leq 20\text{ ns}$ ; $f \leq 500\text{ kHz}$ ; $E_{DS(AL)} \leq 200\text{ nJ}$ ; pulsed		-	45	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$		-	40	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	101	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	118	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$		-	84	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>		-	475	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	101	A

N-channel 40 V, 3.3 mΩ, logic level MOSFET in LPAK33 using NextPower-S3 technology

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{SM}$	peak source current	pulsed; $t_p \leq 10 \mu s$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	475	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25 \text{ A}$ ; $V_{sup} \leq 40 \text{ V}$ ; $R_{GS} = 50 \Omega$ ; $V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; unclamped; $t_p = 308 \mu s$	-	200	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 40 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; $R_{GS} = 50 \Omega$	[2]	80	A

- [1] 118A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.3	1.48	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	130	-	K/W

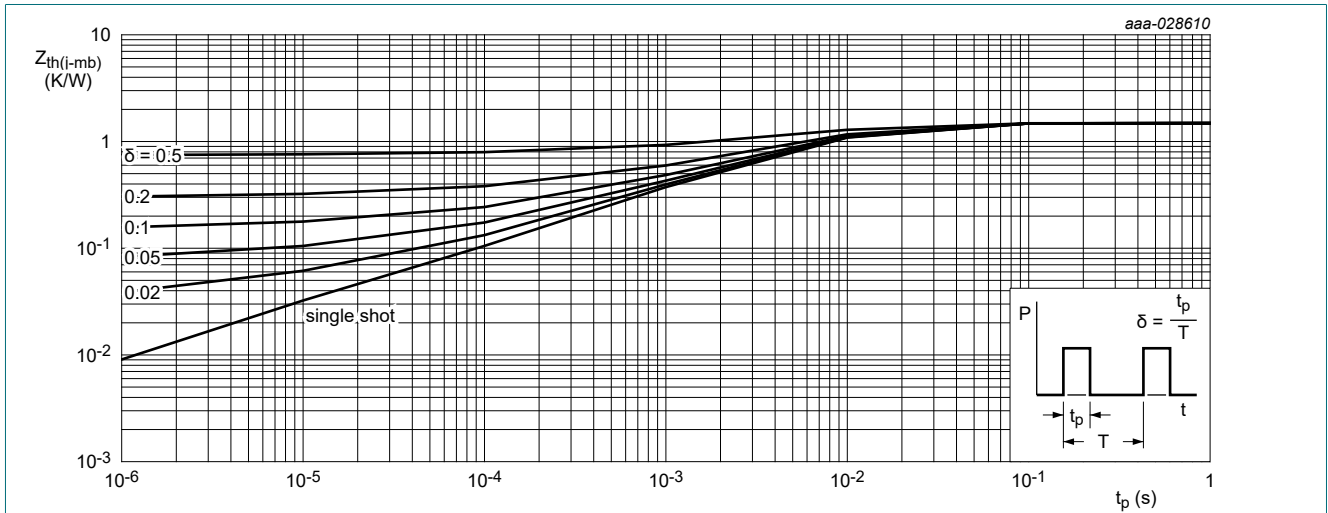


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-028026

Copper square 25.4 mm square; 70 μm thick on FR4 board

aaa-028025

70 μm thick copper on FR4 board

Fig. 5. PCB layout for resistance from junction to ambient

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

### 10. Characteristics

Table 7. Characteristics

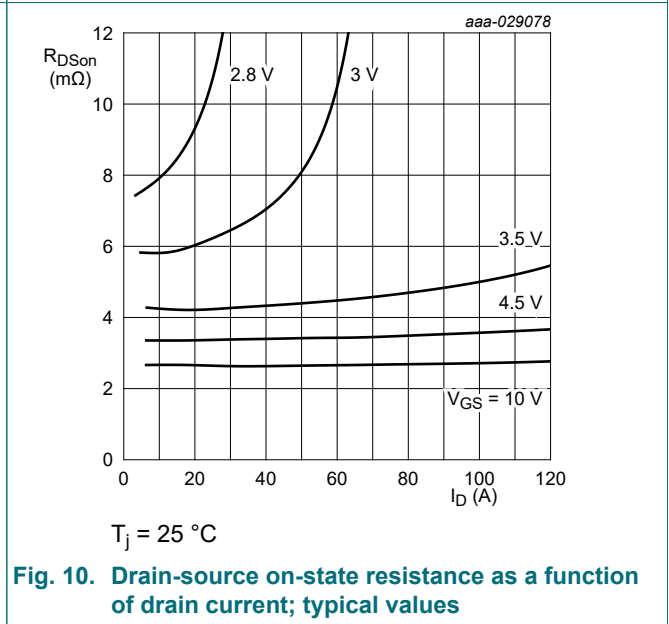
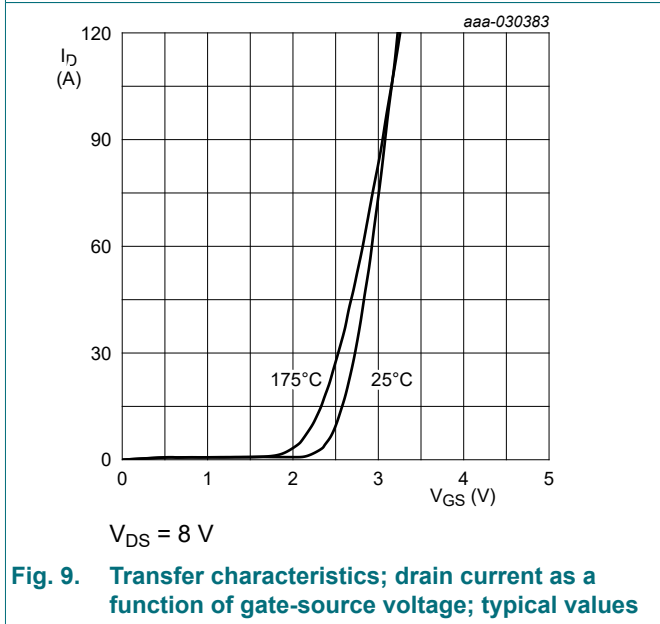
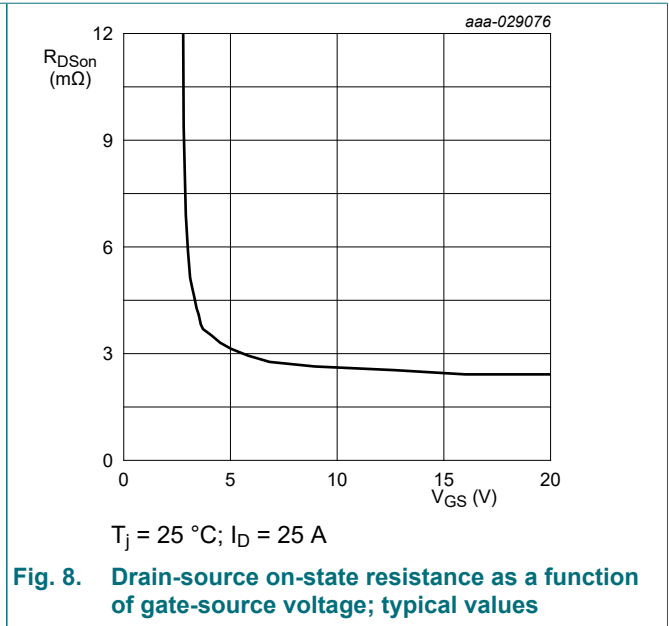
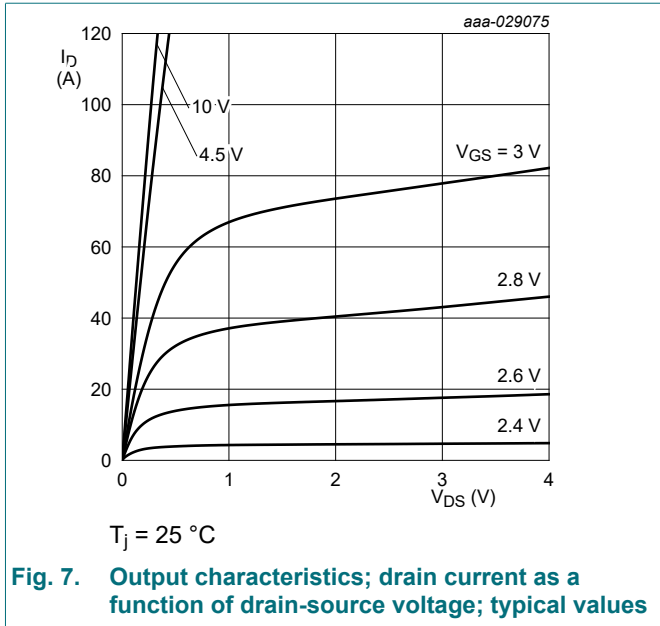
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V

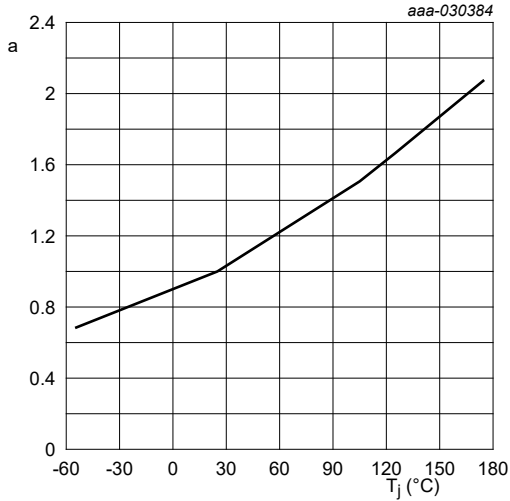
## N-channel 40 V, 3.3 mΩ, logic level MOSFET in LPAK33 using NextPower-S3 technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	1.45	1.77	2.15	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$	-	-4.4	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 32 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.01	1	$\mu\text{A}$
		$V_{DS} = 32 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 125 \text{ }^\circ\text{C}$	-	1.6	-	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -16 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	2.7	3.3	mΩ
		$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 175 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	-	-	7.2	mΩ
		$V_{GS} = 4.5 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	3.4	4.2	mΩ
		$V_{GS} = 4.5 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 175 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	-	-	9.2	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$	0.3	0.8	2	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}$ ; $V_{DS} = 20 \text{ V}$ ; $V_{GS} = 4.5 \text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	11	17	24	nC
		$I_D = 25 \text{ A}$ ; $V_{DS} = 20 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	24	38	54	nC
		$I_D = 0 \text{ A}$ ; $V_{DS} = 0 \text{ V}$	-	20	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}$ ; $V_{DS} = 20 \text{ V}$ ; $V_{GS} = 4.5 \text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	4	6.8	10.2	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		2.4	4	6	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		1.7	2.8	4.2	nC
$Q_{GD}$	gate-drain charge		1.2	4	8	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$ ; $V_{DS} = 20 \text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.8	-	V
$C_{iss}$	input capacitance	$V_{DS} = 20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 14</a>	1761	2710	3794	pF
$C_{oss}$	output capacitance		407	627	877	pF
$C_{rss}$	reverse transfer capacitance		30	101	222	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 \text{ V}$ ; $R_L = 0.8 \text{ } \Omega$ ; $V_{GS} = 4.5 \text{ V}$ ; $R_{G(ext)} = 5 \text{ } \Omega$	-	16	-	ns
$t_r$	rise time		-	19	-	ns
$t_{d(off)}$	turn-off delay time		-	17	-	ns
$t_f$	fall time		-	11	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 20 \text{ V}$ ; $f = 1 \text{ MHz}$	-	20	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 15</a>	-	0.8	1	V

N-channel 40 V, 3.3 mΩ, logic level MOSFET in LPAK33 using NextPower-S3 technology

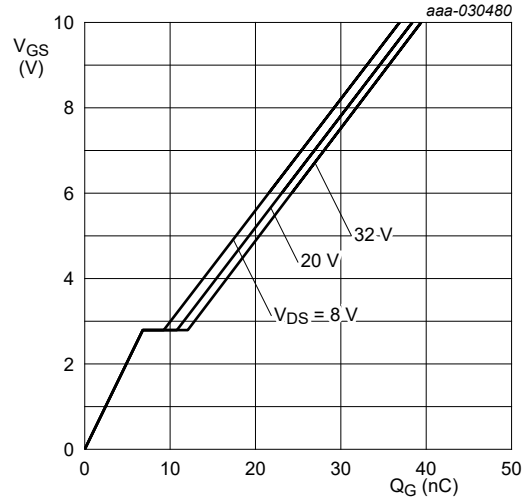
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; <a href="#">Fig. 16</a>	-	27	-	ns
$Q_r$	recovered charge		-	22	-	nC
$t_a$	reverse recovery rise time		-	16	-	ns
$t_b$	reverse recovery fall time		-	11	-	ns





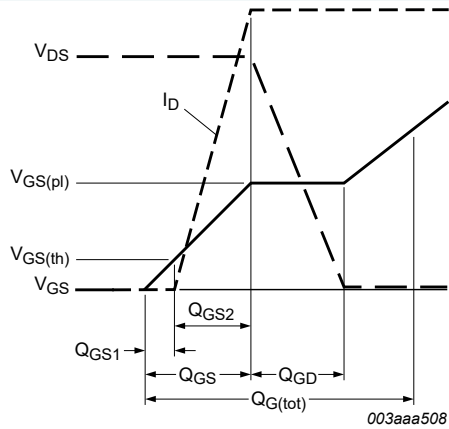
$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

**Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature**

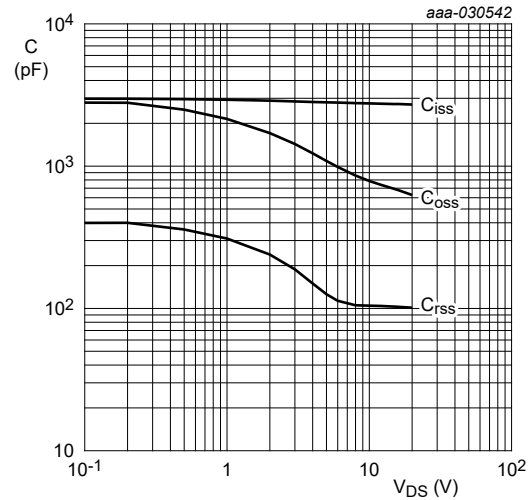


$T_j = 25^{\circ}\text{C}; I_D = 25\text{ A}$

**Fig. 12. Gate-source voltage as a function of gate charge; typical values**

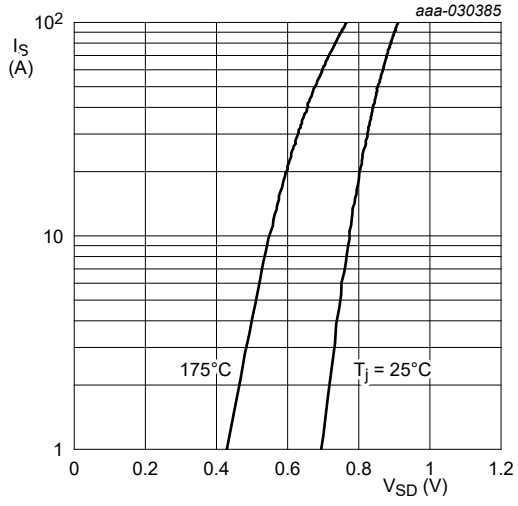


**Fig. 13. Gate charge waveform definitions**



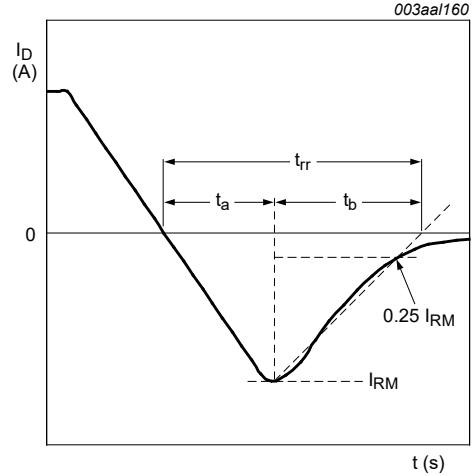
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$V_{GS} = 0\text{ V}$

**Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



**Fig. 16. Reverse recovery timing definition**



### 11. Package outline

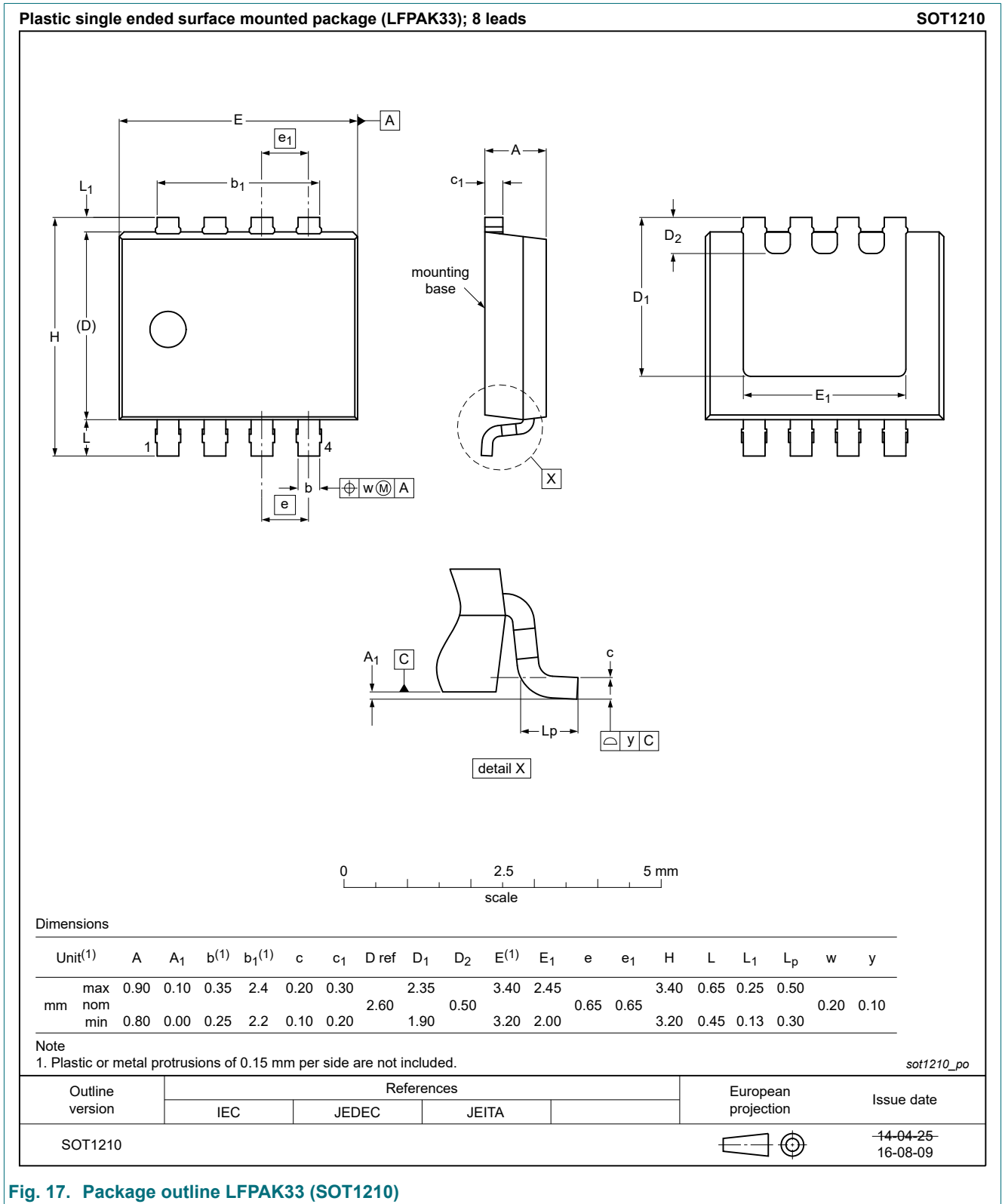
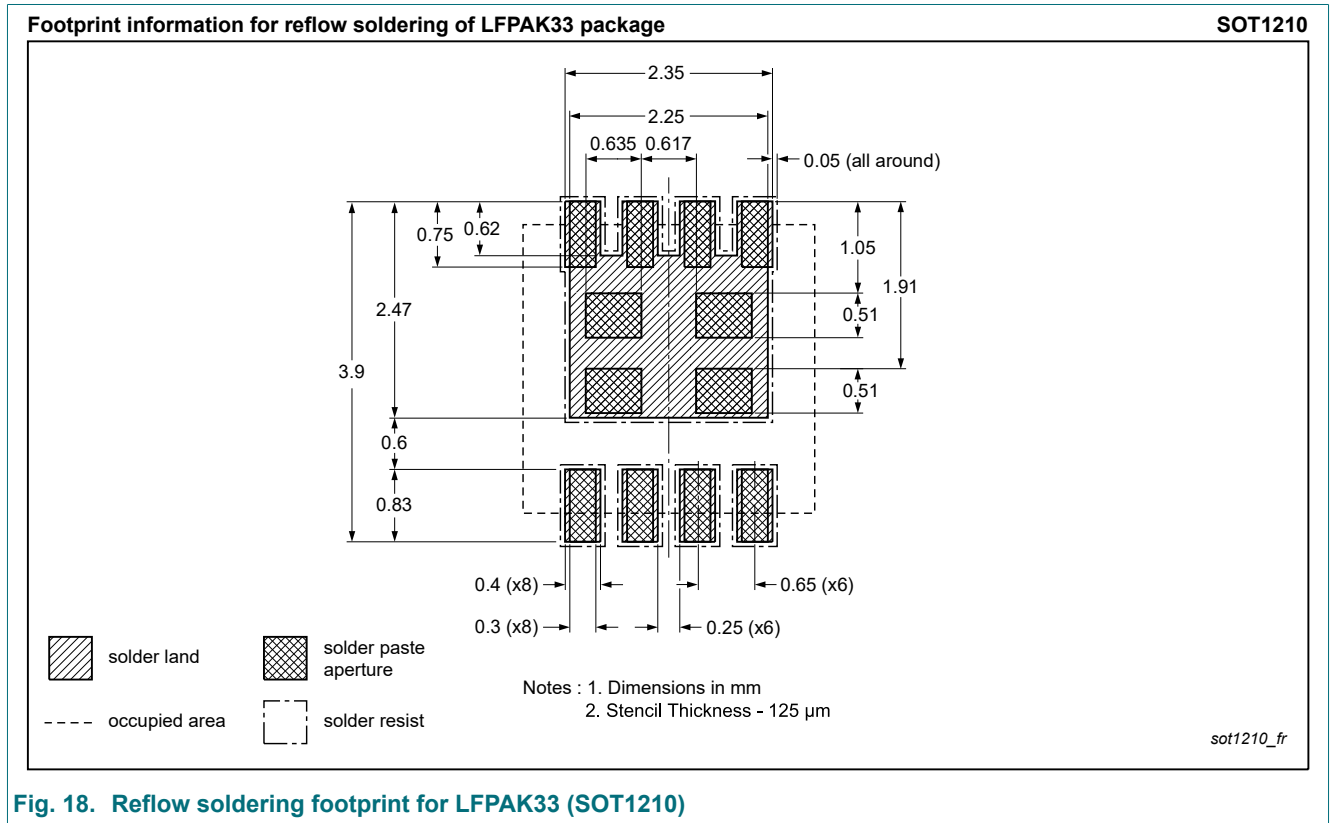


Fig. 17. Package outline LPAK33 (SOT1210)

## 12. Soldering



**Fig. 18. Reflow soldering footprint for LPAK33 (SOT1210)**

## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
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