To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

2SK3511

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3511 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance:
  $R_{DS(on)}$ = 12.5 mΩ MAX. (V_{GS} = 10 V, I_D = 42 A)
- Low C_{iss}: C_{iss} = 5900 pF TYP.
- Built-in gate protection diode

ORDERING INFORMATION

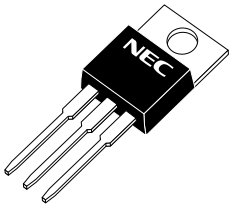
PART NUMBER	PACKAGE
2SK3511	TO-220AB
2SK3511-S	TO-262
2SK3511-ZJ	TO-263
2SK3511-Z	TO-220SMD Note

Note TO-220SMD package is produced only in Japan.

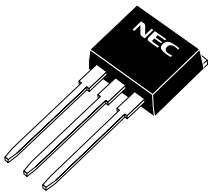
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	75	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±83	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±260	A
Total Power Dissipation (T_C = 25°C)	P_T	100	W
Total Power Dissipation (T_A = 25°C)	P_T	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	52	A
Single Avalanche Energy Note2	E_{AS}	250	mJ

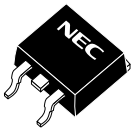
(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)



Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 35 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

THERMAL RESISTANCE

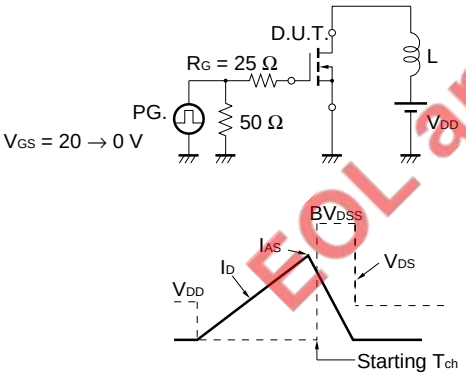
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.25	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

Document No. D15617EJ1V0DS00 (1st edition)
Date Published May 2002 NS CP(K)
Printed in Japan

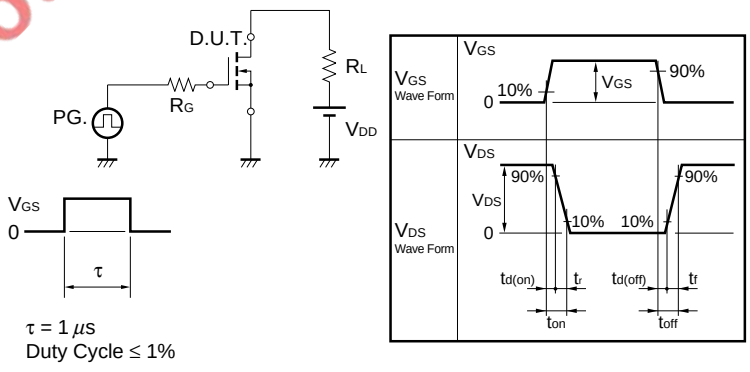
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 75 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.0	3.0	4.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 42 A	21	45		S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 42 A		9.5	12.5	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		5900		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		810		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		400		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 38 V, I_D = 42 A		30		ns
Rise Time	t_r	V_{GS} = 10 V		21		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		72		ns
Fall Time	t_f			12		ns
Total Gate Charge	Q_G	V_{DD} = 60 V		100		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		24		nC
Gate to Drain Charge	Q_{GD}	I_D = 83 A		35		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 83 A, V_{GS} = 0 V		1.1		V
Reverse Recovery Time	t_{rr}	I_F = 83 A, V_{GS} = 0 V		70		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		200		nC

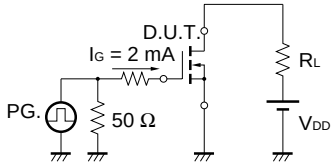
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

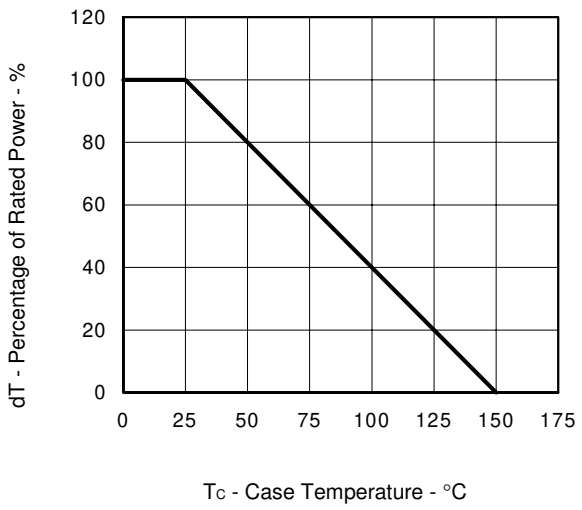


TEST CIRCUIT 3 GATE CHARGE

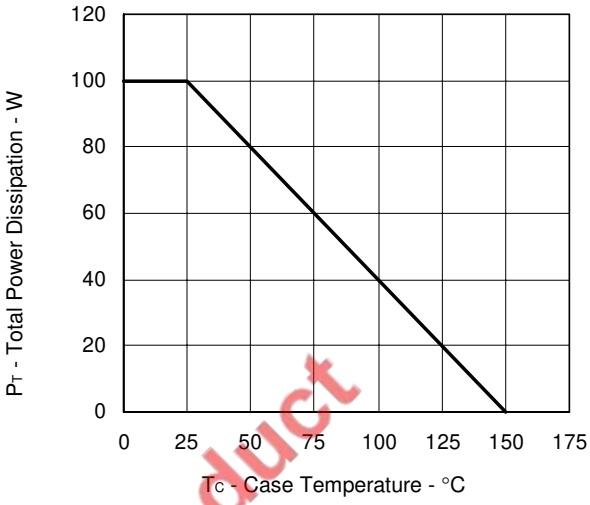


TYPICAL CHARACTERISTICS (T_A = 25°C)

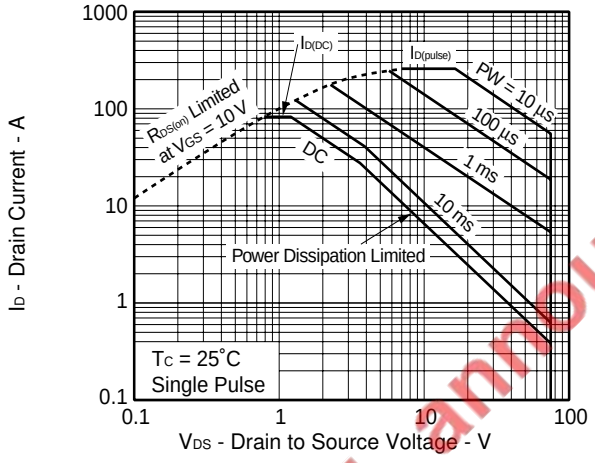
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



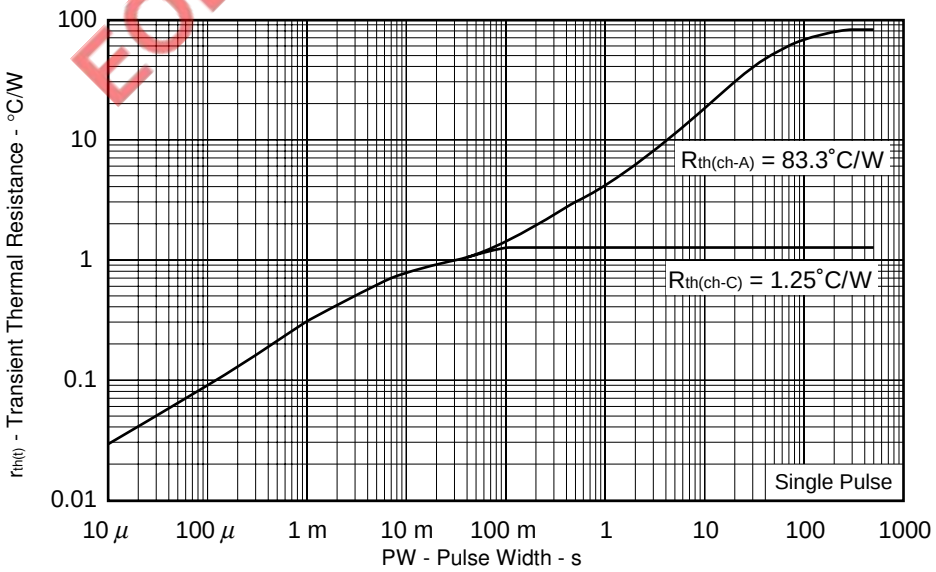
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



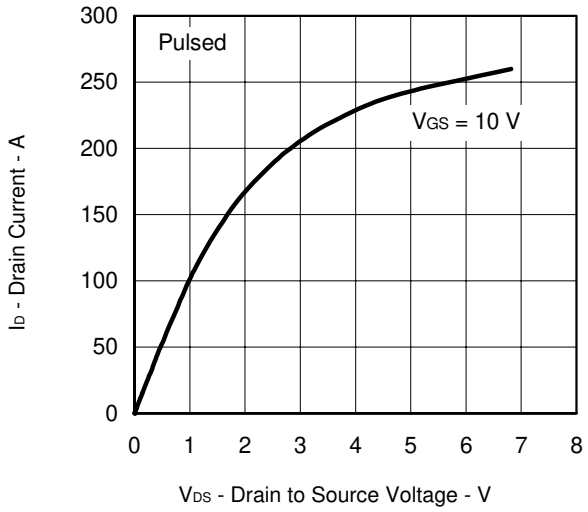
FORWARD BIAS SAFE OPERATING AREA



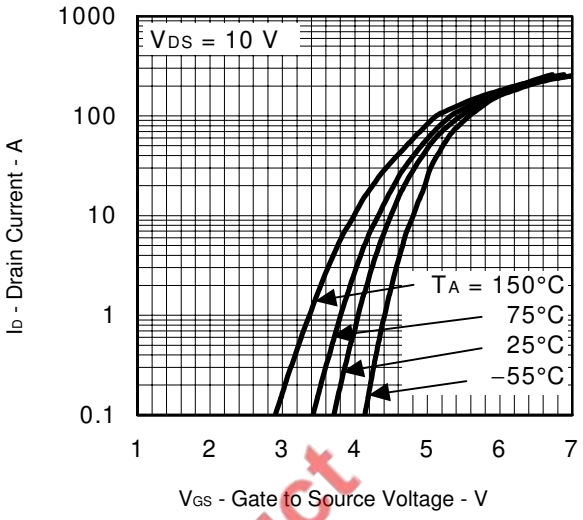
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



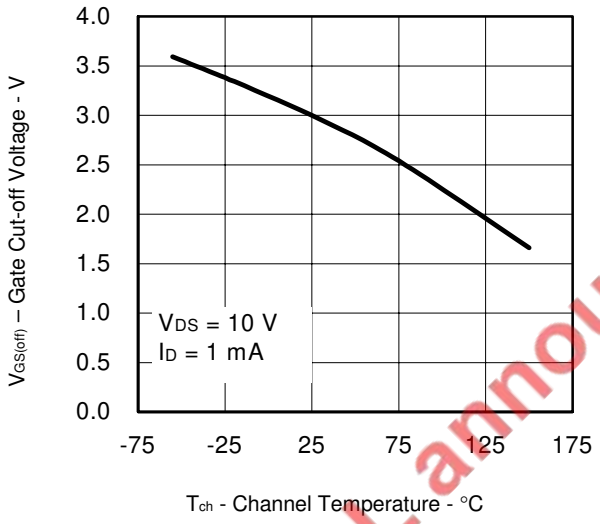
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



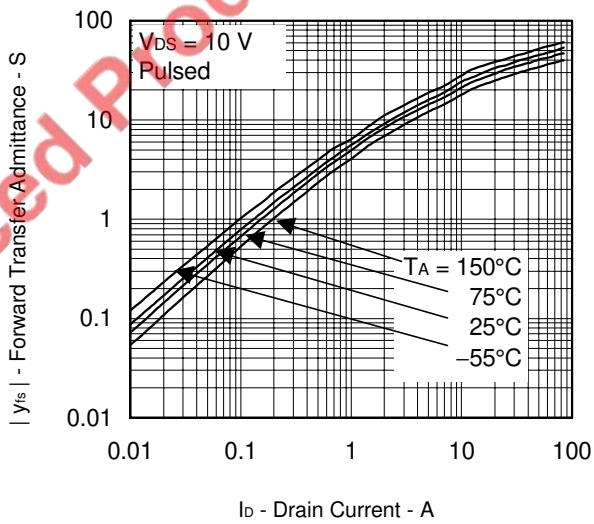
FORWARD TRANSFER CHARACTERISTICS



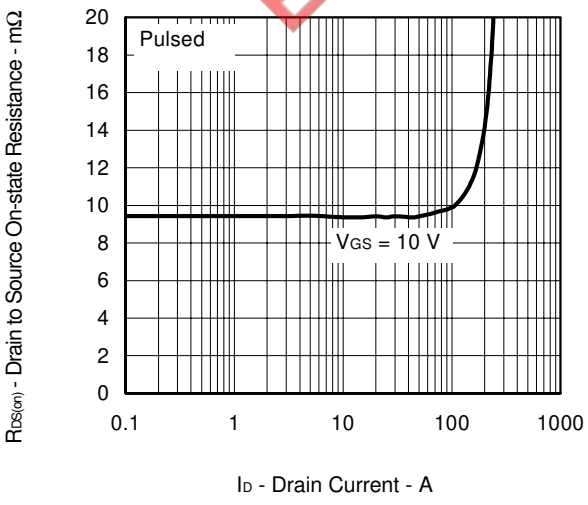
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



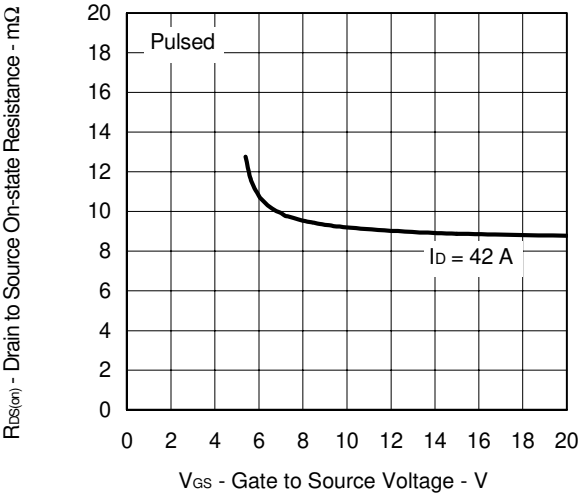
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



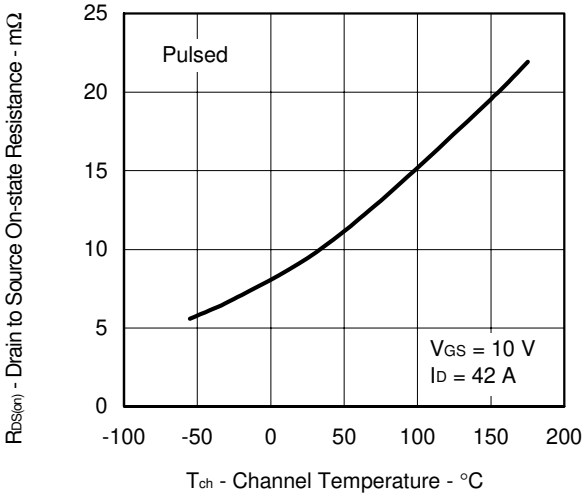
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



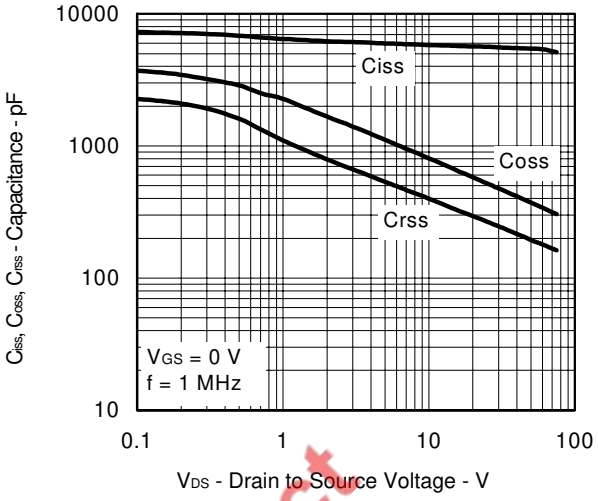
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



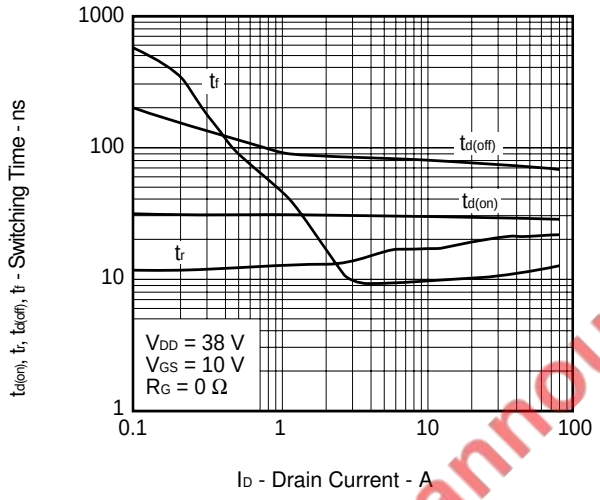
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



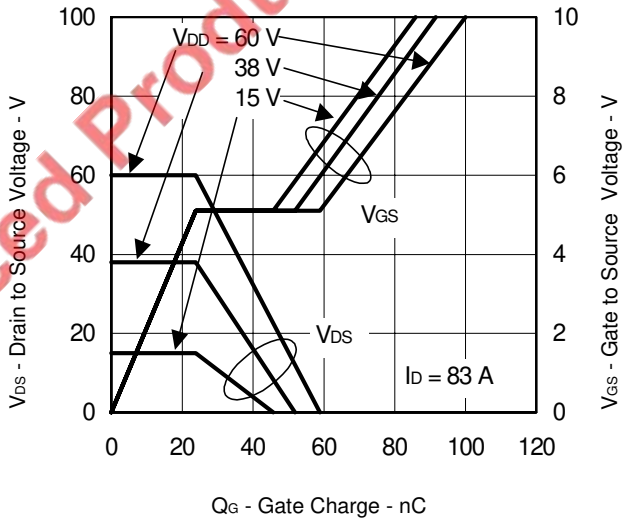
CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



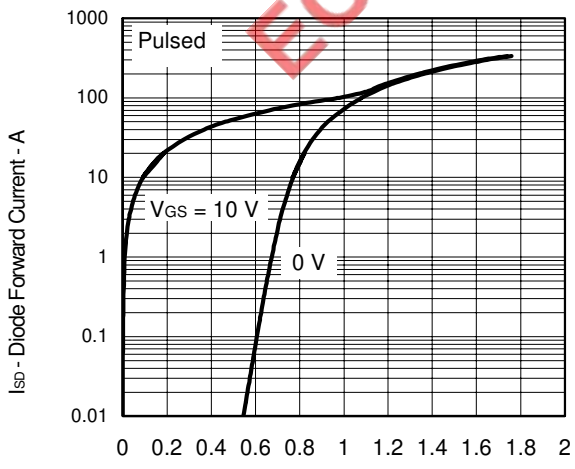
SWITCHING CHARACTERISTICS



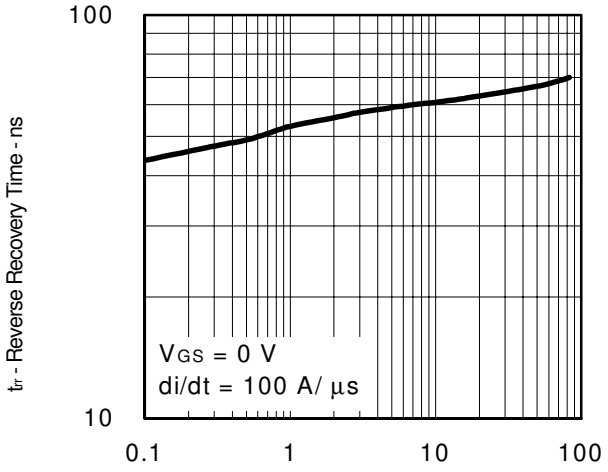
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



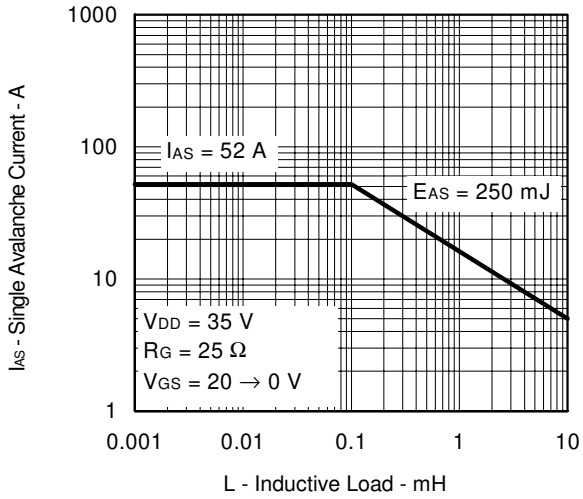
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



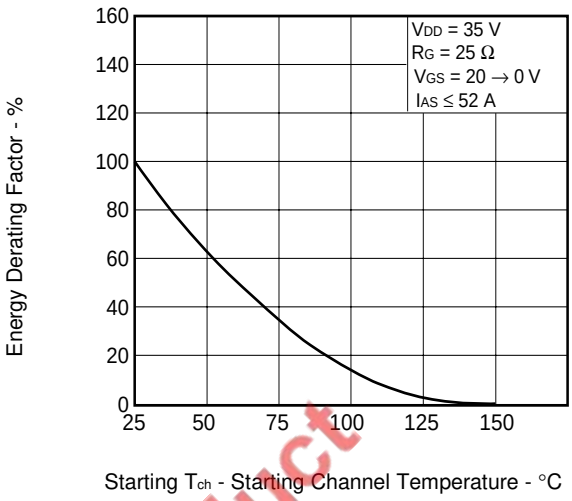
REVERSE RECOVERY TIME vs. DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

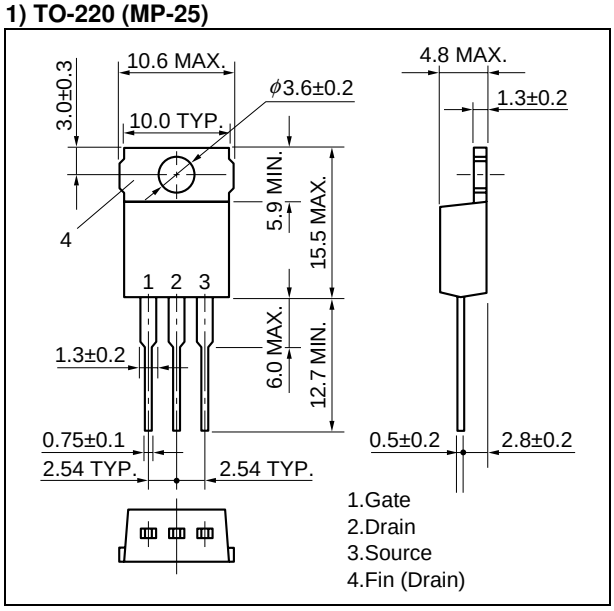


SINGLE AVALANCHE ENERGY
DERATING FACTOR

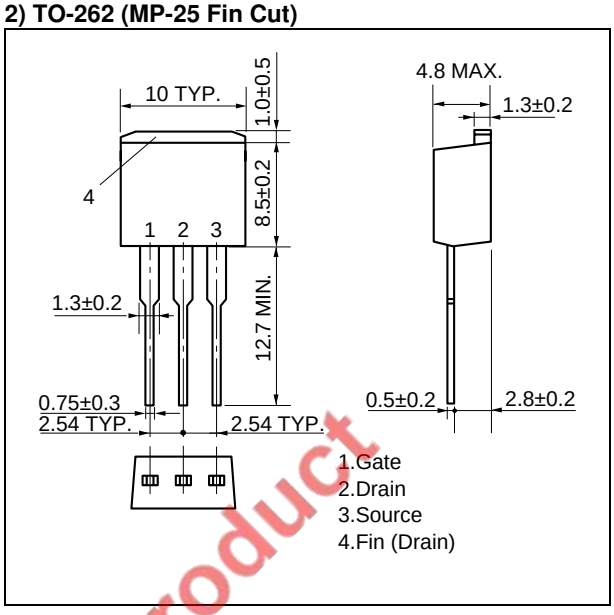


PACKAGE DRAWINGS (Unit: mm)

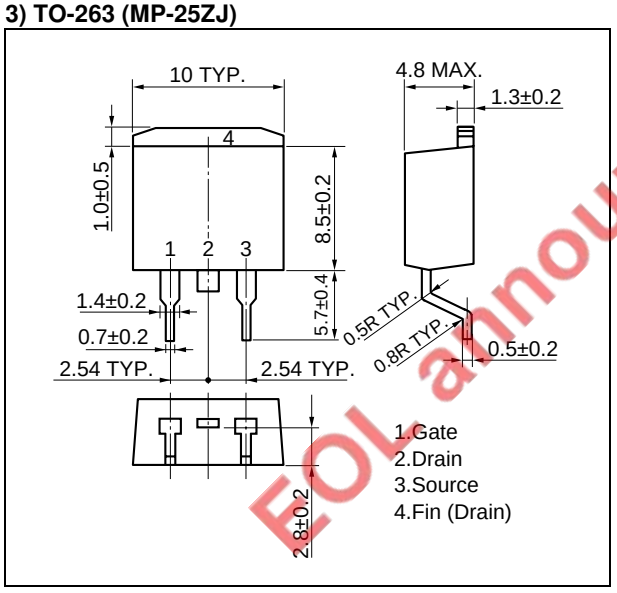
1) TO-220 (MP-25)



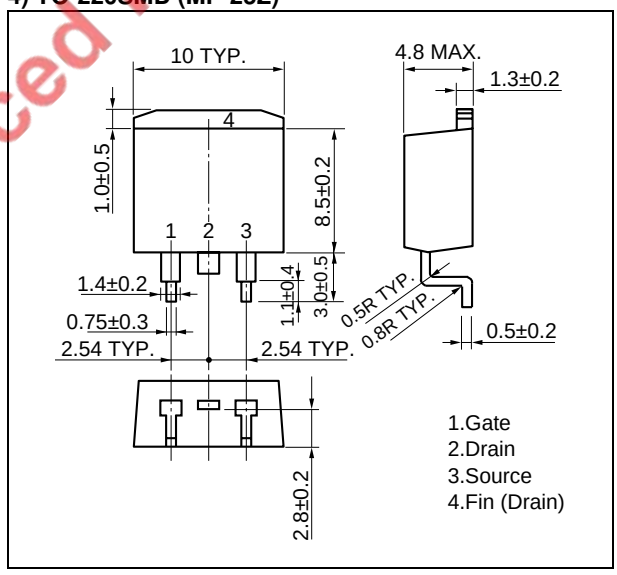
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)

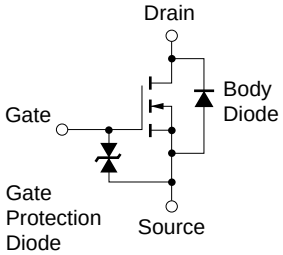


4) TO-220SMD (MP-25Z) Note



Note This Package is only produced in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.