Texas Instruments

TAS5086-5142V6EVM User's Guide

Evaluation Module for the TAS5086 6-Channel Digital Audio PWM Processor and TAS5142 Digital Amplifier Power Output Stage

User's Guide

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SLEU072

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Overview

The TAS5086-5142V6EVM PurePath Digital™ customer evaluation amplifier module demonstrates two audio integrated circuits, TAS5086 and TAS5142, from Texas Instruments (TI).

The TAS5086DBT is a high-performance, 32-bit (24-bit input) multichannel PurePath Digital™ pulse width modulator (PWM) based on Equibit™ technology, with a fully symmetrical AD modulation scheme. It accepts an input sample rate from 32 kHz to 192 kHz.

The TAS5142DDV is a compact, high-power, digital amplifier power stage designed to drive a 4-Ω loudspeaker up to 100 W/10% THD+N. It contains integrated gate drivers, four matched and electrically isolated enhancement-mode N-channel power DMOS transistors, and protection/fault-reporting circuitry. In this application output power is limited to 50 W due to thermal constraints.

The DDV package has a PowerPAD™ on the top side for heat transfer through a heatsink. The heatsink in this design is for evaluation purpose only.

This EVM, together with a TI input-USB board, is a complete 5.1-channel digital audio amplifier system, which includes digital input (S/PDIF), analog inputs, interface to PC, and features, such as digital volume control, input and output multiplexers, auto mute, and simple bass management. There are configuration options for power-stage failure protection and a mini-jack connector for headphones.

This system is designed for home theater applications, such as flatscreen TVs, DVD minicomponent systems, home theater in a box (HTIB), or DVD receivers.

1.1 TAS5086-5142V6EVM Features

- 5.1-channel PurePath Digital evaluation module
- Self-contained protection system (short circuit and thermal)
- Standard I^2S and I^2C/control connector for TI input board
- Double-sided plated-through PCB layout

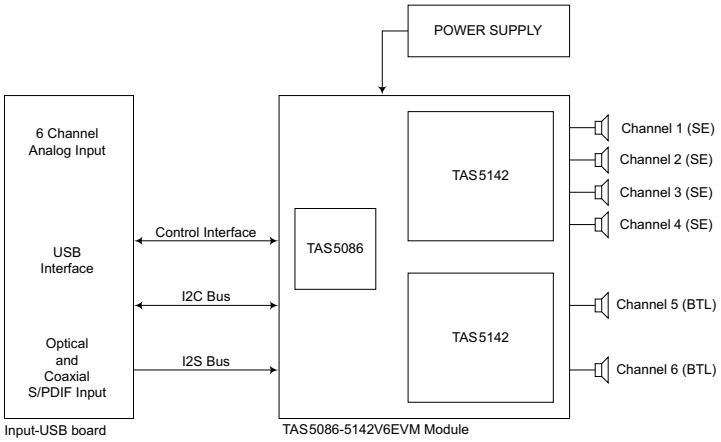


Figure 1-1. Integrated PurePath Digital™ Amplifier System

1.2 PCB Key Map

Physical structure for the TAS5086-5142V6EVM is illustrated in Figure 1-2.

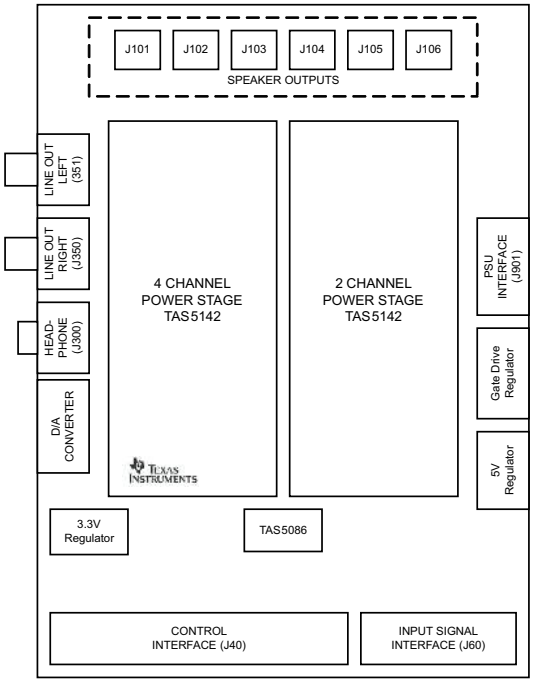


Figure 1-2. Physical Structure for TAS5086-5142V6EVM (Rough Outline)

System Interfaces

This chapter describes the TAS5086-5142V6EVM board in regards to power supplies and system interfaces.

2.1 Power Supply (PSU) Interface (J901)

The TAS5086-5142V6EVM module must be powered from external power supplies. High-end audio performance requires a stabilized power supply with low ripple voltage and low output impedance.

Note: The length of power-supply cable must be minimized. Increasing length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

Maximum output-stage supply voltage depends of the speaker load resistance. Please check the recommended maximum supply voltage in the TAS5142 data sheet.

Table 2-1. Recommended Supply Voltages

DESCRIPTION	VOLTAGE LIMITATIONS	CURRENT RECOMMENDATIONS
System power supply	15 V to 20 V	0.2 A
Output-stage power supply	0 V to 32 V	2 A(1)

(1) The rated current correspond to 2-channel full scale (30 W each), which most likely is adequate for a standard 2.1 channel amplifier design.

The recommended TAS5142 power-up sequence is shown in the figure below. For proper TAS5142 operation, the $\overline{\text{RESET}}$ signal should be kept low during power up. $\overline{\text{RESET}}$ is pulled low during power up for 200 ms by the onboard reset generator (U908).

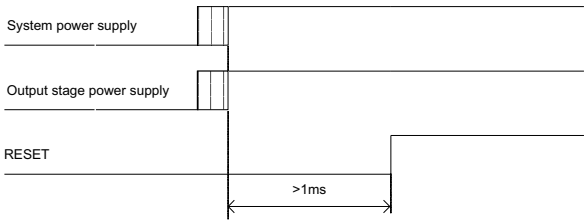
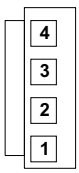


Figure 2-1. Recommended Power-Up Sequence



(PCB connector top view)

Figure 2-2. J901 Pin Numbers

Table 2-2. J901 Pin Description

PIN NO.	NET-NAME AT SCHEMATICS	DESCRIPTION
1	PVDD	Output-stage power supply
2	—	System power supply
3	GND	Ground
4	GND	Ground

2.2 Loudspeaker Connectors (J101 … J106)

CAUTION

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g., through an oscilloscope).

(PCB connector top view)

Figure 2-3. J101 . . . J106 Pin Numbers

Table 2-3. J101 . . . J106 Pin Description

PIN NO.	NET-NAME AT SCHEMATICS	DESCRIPTION
1	OUT-1	Speaker negative output
2	OUT-2	Speaker positive output

2.3 Control Interface (J40)

This interface connects the TAS5086-5142V6EVM board to a TI input-USB board.

Table 2-4. J40 Pin Description

PIN NO.	NET-NAME AT SCHEMATICS	DESCRIPTION
1	GND	Ground
2	RESERVED	—
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional). Activate $\overline{\text{MUTE}}$ before $\overline{\text{RESET}}$ for quiet reset.
5	$\overline{\text{BKND-ERR}}$	Backend error (or soft reset) provides reduced click and pop reset, without resetting I^2C volume register settings.
6	$\overline{\text{MUTE}}$	Ramp volume from any setting to noiseless soft mute. Mute can also be activated by I^2C.
7	$\overline{\text{PDN}}$	Power down. TAS5086 will go to power-down state when activated.
8	RESERVED	—
9	RESERVED	—
10	SDA	I^2C data clock

Table 2-4. J40 Pin Description (continued)

PIN NO.	NET-NAME AT SCHEMATICS	DESCRIPTION
11	GND	Ground
12	SCL	I^2C bit clock
13	RESERVED	—
14	RESERVED	—
15	RESERVED	—
16	RESERVED	—
17	GND	Ground
18	RESERVED	—
19	RESERVED	—
20	$\overline{SD}$	Shutdown error reporting for all channels. Activated if TAS5142 has high current or high temperature. See Chapter 3, *Protection.*
21	RESERVED	—
22	$\overline{OTW}$	Temperature warning. Activated if TAS5142 has reached temperature warning level.
23	RESERVED	—
24	RESERVED	—
25	GND	Ground
26	GND	Ground
27	RESERVED	—
28	RESERVED	—
29	RESERVED	—
30	RESERVED	—
31	GND	Ground
32	GND	Ground
33	+5V	+5Vdc power supply (output)
34	+5V	+5Vdc power supply (output)

2.4 Digital Audio Interface (J60)

The digital audio interface contains digital audio signal data (I^2S), clocks, etc. Please see the *TAS5086 Data Manual* for signal timing and details not explained in this document.

Table 2-5. J60 Pin Description

PIN NO.	NET-NAME AT SCHEMATICS	DESCRIPTION
1	GND	Ground
2	MCLK	Master clock input. Low jitter system clock for PWM generation and reclocking. Ground connection from source to TAS5086 must be a low impedance connection.
3	GND	Ground
4	SDIN1	I^2S data 1, channel 1 and 2
5	SDIN2	I^2S data 2, channel 3 and 4
6	SDIN3	I^2S data 3
7	SDIN4	I^2S data 4
8	—	Reserved
9	—	Reserved
10	GND	Ground
11	SCLK	I^2S bit clock
12	GND	Ground
13	LRCLK	I^2S left-right clock
14	GND	Ground
15	—	Reserved
16	GND	Ground

Protection

This chapter describes the short-circuit protection and fault-reporting circuitry of the TAS5142 device.

3.1 Short-Circuit Protection and Fault-Reporting Circuitry

The TAS5142 is a self-protecting device that provides device fault reporting (including high-temperature protection and short-circuit protection). The TAS5142 is configured in back-end auto-recovery mode and, therefore, resets automatically after all errors. This means that the device will restart itself after an error occasion and report through the $\overline{SD}$ signal.

3.2 Device Fault Reporting

The $\overline{OTW}$ and $\overline{SD}$ outputs from the TAS5142 indicate fault conditions. Please refer to the *TAS5142 Data Manual* for a description of these pins.

Table 3-1. TAS5142 Warning/Error Signal Decoding

$\overline{OTW}$	$\overline{SD}$	DEVICE CONDITION
0	0	High-temperature error and/or high-current error
0	1	High-temperature warning
1	0	Undervoltage lockout or high-current error
1	1	Normal operation, no errors/warnings

The temperature warning signal is an open collector connected to pin 22 ($\overline{OTW}$) in the control interface connector.

The shutdown signal is an open collector connected to pin 20 ($\overline{SD}$) in the control interface connector.

The shutdown signals, together with the temperature warning signal, give chip state information as described in Table 3-1. Device fault-reporting outputs are open-drain outputs.

Related Documentation from Texas Instruments

The following is a list of documents that have detailed descriptions of the integrated circuits used in the design of the TAS5508-5142V6EVM. This information can be obtained at the URL http://www.ti.com.

- TAS5086 data sheet (SLES131)
- TAS5142 data sheet (SLES126)
- UA78M12 data sheet (SLVS059)
- TPS3801K33 data sheet (SLVS219)
- TLV320DAC23 data sheet (SLES001)
- TLV2217-33 data sheet (SLVS067)

Additional documents

- TAS5086-5142V6EVM Application Report (SLEA056)
- PC Configuration Tool for TAS5086 (TAS5086 GUI ver. 4.0 or later)
- General Application Notes

4.1 Trademarks

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 to 32 V and the output voltage range of 15 V to 20 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75ï½C. The EVM is designed to operate properly with certain components above 75ï½C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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