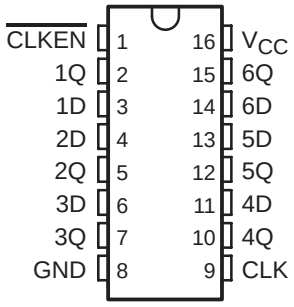
- **Contains Six D-Type Flip-Flops With Single-Rail Outputs**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Buffered Common Enable Input**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The SN74F378 is a positive-edge-triggered D-type flip-flop with a clock enable ($\overline{\text{CLKEN}}$) input. The SN74F378 is similar to the SN74F174 but features a common clock enable instead of a common clear.

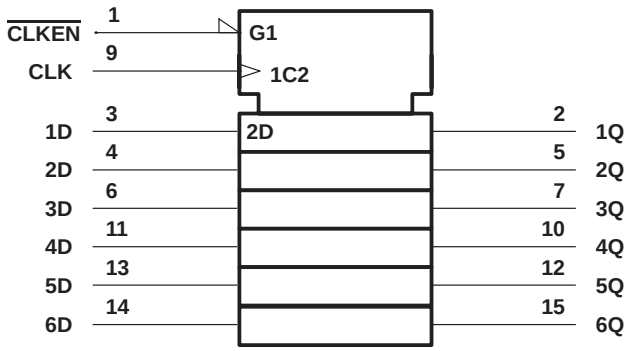
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74F378 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

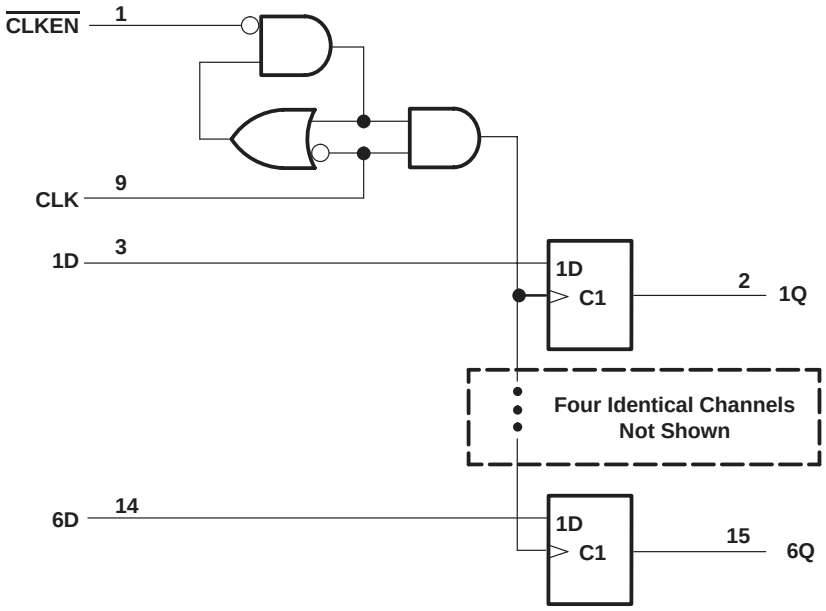
INPUTS			OUTPUT
$\overline{\text{CLKEN}}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −1.2 V to 7 V
Input current range . . . . . −30 mA to 5 mA
Voltage range applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = − 18 mA			− 1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 1 mA	2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = − 1 mA	2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			− 0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	− 60		− 150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 2		30	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open, all data inputs and the enable input grounded, and the clock input at 4.5 V after being momentarily grounded.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	110	0	110	MHz
t_w	Pulse duration	CLK high	4		4		ns
		CLK low	6		6		
t_{su}	Setup time before CLK↑	Data high or low	5		5		ns
		$\overline{\text{CLKEN}}$ high	3.5		3.5		
		$\overline{\text{CLKEN}}$ low	5		5		
t_h	Hold time after CLK↑	Data high or low	1		1		ns
		$\overline{\text{CLKEN}}$ high or low	0		0		

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			110	125		110		MHz
t_{PLH}	CLK	Any Q	3.3	4.5	6.1	3.1	6.7	ns
t_{PHL}			3	4.2	6	2.9	6.1	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74F378D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74F378DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74F378N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

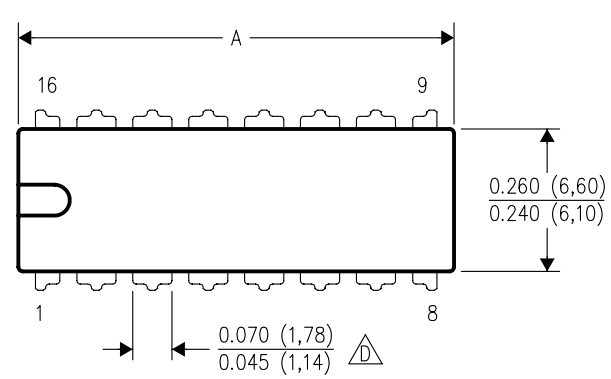
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

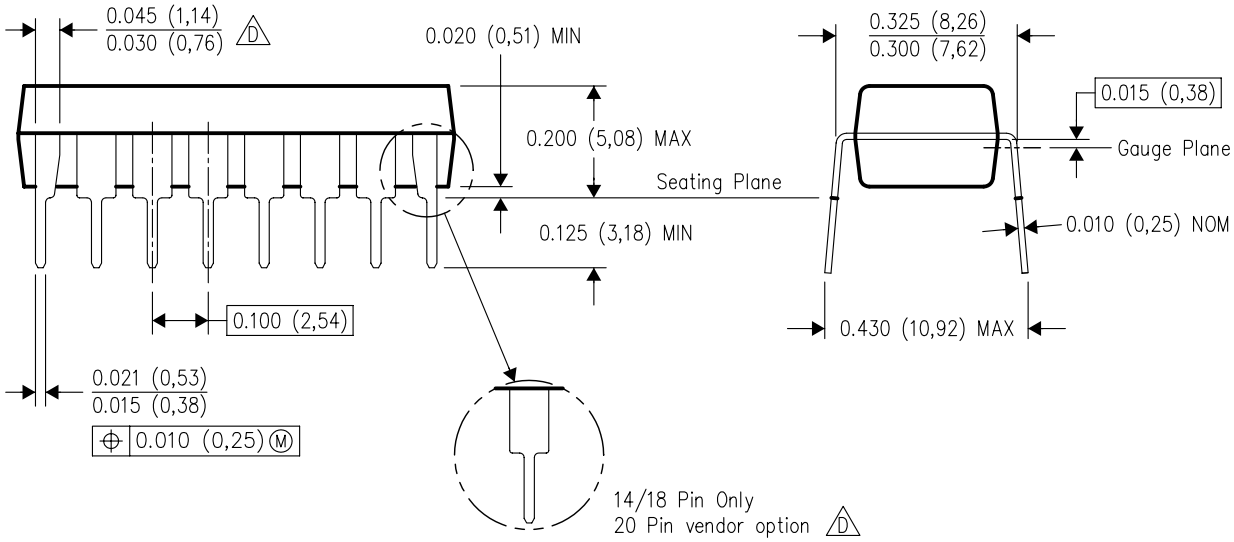
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



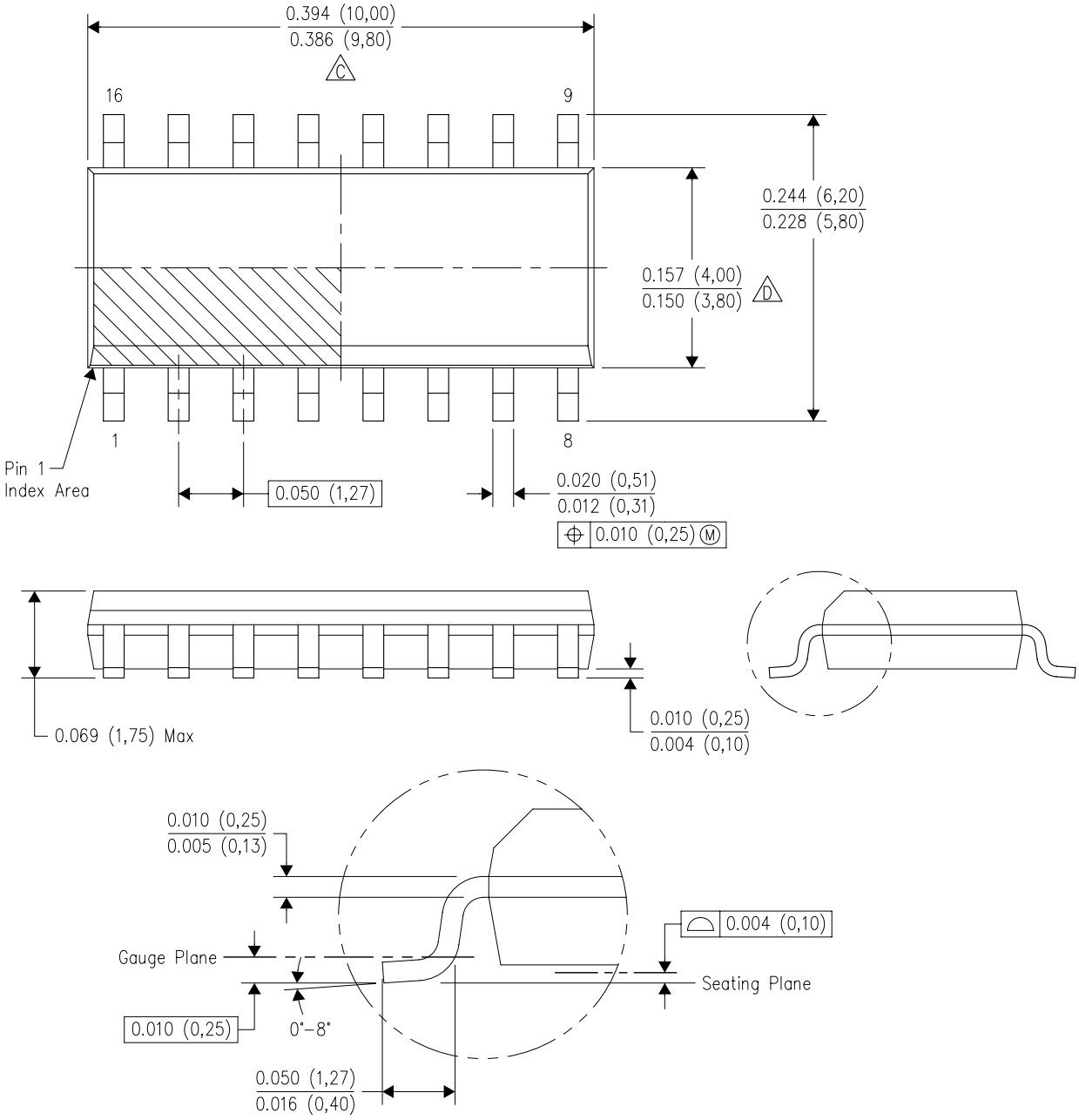
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.