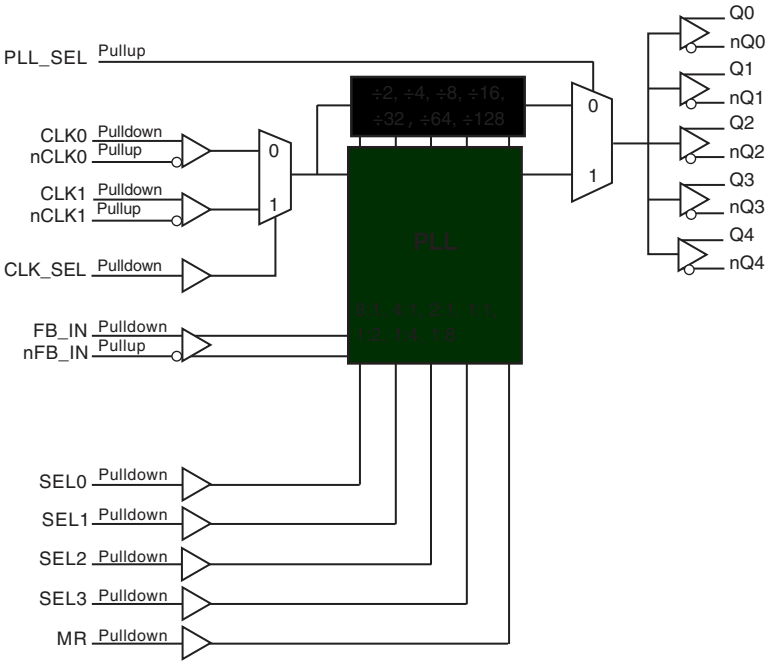
## General Description

The 8735-31 is a highly versatile 1:5 Differential -to-3.3V LVPECL Clock Generator. The 8735-31 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 15.625MHz to 350MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

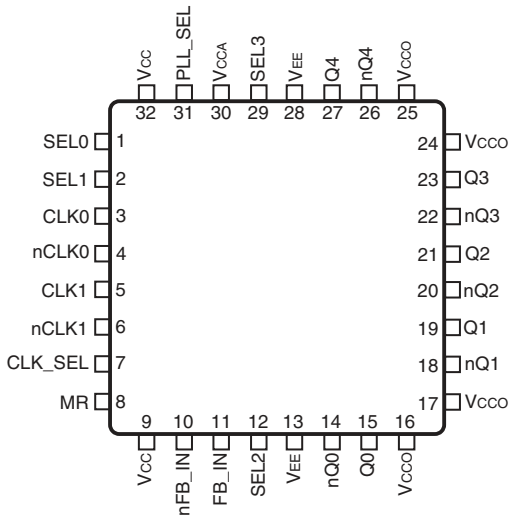
## Features

- Five differential 3.3V LVPECL output pairs
- Selectable differential clock inputs
- CLKx/nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Output frequency range: 15.625MHz to 350MHz
- Input frequency range: 15.625MHz to 350MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 60ps (maximum)
- Output skew: 35ps (maximum)
- Static phase offset: 55ps ± 125ps
- Full 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram




## Pin Assignment




**8735-31**
**32-Lead LQFP**
**7mm x 7mm x 1.4mm package body**
**Y Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2, 12, 29 | SEL0, SEL1, SEL2, SEL3 | Input | Pulldown | Determines output divider values in Table 3. LVCMOS / LVTTL interface levels. |
| 3 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 4 | nCLK0 | Input | Pullup | Inverting differential clock input. |
| 5 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 6 | nCLK1 | Input | Pullup | Inverting differential clock input. |
| 7 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK1/nCLK1. When LOW, selects CLK0/nCLK0. LVCMOS / LVTTL interface levels. |
| 8 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels. |
| 9, 32 | $V_{CC}$ | Power | | Core supply pins. |
| 10 | nFB_IN | Input | Pullup | Inverting differential feedback input to phase detector for regenerating clocks with “zero delay.” |
| 11 | FB_IN | Input | Pulldown | Non-inverted differential feedback input to phase detector for regenerating clocks with “zero delay.” |
| 13, 28 | $V_{EE}$ | Power | | Negative supply pins. |
| 14, 15 | nQ0, Q0 | Output | | Differential output pair. LVPECL interface levels. |
| 16, 17, 24, 25 | $V_{CCO}$ | Power | | Output supply pins. |
| 18, 19 | nQ1, Q1 | Output | | Differential output pair. LVPECL interface levels. |
| 20, 21 | nQ2, Q2 | Output | | Differential output pair. LVPECL interface levels.. |
| 22, 23 | nQ3, Q3 | Output | | Differential output pair. LVPECL interface levels. |
| 26, 27 | nQ4, Q4 | Output | | Differential output pair. LVPECL interface levels. |
| 30 | $V_{CCA}$ | Power | | Analog supply pin. |
| 31 | PLL_SEL | Input | Pullup | PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

# Function Tables

**Table 3A. Control Input Function Table**

| Inputs | | | | | Outputs PLL_SEL = 1 PLL Enable Mode |
|---|---|---|---|---|---|
| SEL3 | SEL2 | SEL1 | SEL0 | Reference Frequency Range (MHz) | Q0:Q4, nQ0:nQ4 |
| 0 | 0 | 0 | 0 | 125 - 350 | ÷1 |
| 0 | 0 | 0 | 1 | 62.5 - 175 | ÷1 |
| 0 | 0 | 1 | 0 | 31.25 - 87.5 | ÷1 |
| 0 | 0 | 1 | 1 | 15.625 - 43.75 | ÷1 |
| 0 | 1 | 0 | 0 | 125 - 350 | ÷2 |
| 0 | 1 | 0 | 1 | 62.5 - 175 | ÷2 |
| 0 | 1 | 1 | 0 | 31.25 - 87.5 | ÷2 |
| 0 | 1 | 1 | 1 | 125 - 350 | ÷4 |
| 1 | 0 | 0 | 0 | 62.5 - 175 | ÷4 |
| 1 | 0 | 0 | 1 | 125 - 350 | ÷8 |
| 1 | 0 | 1 | 0 | 62.5 - 175 | x2 |
| 1 | 0 | 1 | 1 | 31.25 - 87.5 | x2 |
| 1 | 1 | 0 | 0 | 15.625 - 43.75 | x2 |
| 1 | 1 | 0 | 1 | 31.25 - 87.5 | x4 |
| 1 | 1 | 1 | 0 | 15.625 - 43.75 | x4 |
| 1 | 1 | 1 | 1 | 15.625 - 43.75 | x8 |

**Table 3B. PLL Bypass Function Table**

| Inputs | | | | Outputs<br>PLL_SEL = 0<br>PLL Bypass Mode |
|---|---|---|---|---|
| **SEL3** | **SEL2** | **SEL1** | **SEL0** | **Q0:Q4, nQ0:nQ4** |
| 0 | 0 | 0 | 0 | ÷8 |
| 0 | 0 | 0 | 1 | ÷8 |
| 0 | 0 | 1 | 0 | ÷8 |
| 0 | 0 | 1 | 1 | ÷16 |
| 0 | 1 | 0 | 0 | ÷16 |
| 0 | 1 | 0 | 1 | ÷16 |
| 0 | 1 | 1 | 0 | ÷32 |
| 0 | 1 | 1 | 1 | ÷32 |
| 1 | 0 | 0 | 0 | ÷64 |
| 1 | 0 | 0 | 1 | ÷128 |
| 1 | 0 | 1 | 0 | ÷4 |
| 1 | 0 | 1 | 1 | ÷4 |
| 1 | 1 | 0 | 0 | ÷8 |
| 1 | 1 | 0 | 1 | ÷2 |
| 1 | 1 | 1 | 0 | ÷4 |
| 1 | 1 | 1 | 1 | ÷2 |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$<br>Continuos Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 150 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 15 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK_SEL, SEL[0:3], MR | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | PLL_SEL | $V_{CC} = V_{IN} = 3.465V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK_SEL, SEL[0:3], MR | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | PLL_SEL | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |

**Table 4C. Differential DC Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | FB_IN, CLK0, CLK1 | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | nFB_IN, nCLK0, nCLK1 | $V_{CC} = V_{IN} = 3.465V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | FB_IN, CLK0, CLK1 | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | nFB_IN, nCLK0, nCLK1 | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE} + 0.5$ | | $V_{CC} – 0.85$ | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as $V_{IH}$.

**Table 4D. LVPECL DC Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO} – 1.4$ | | $V_{CCO} – 0.9$ | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO} – 2.0$ | | $V_{CCO} – 1.7$ | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} – 2V$.

**Table 5. Input Frequency Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | CLK0/nCLK0, CLK1/nCLK1 | PLL_SEL = 1 | 15.625 | | 350 | MHz |
| | | | PLL_SEL = 0 | | | 700 | MHz |

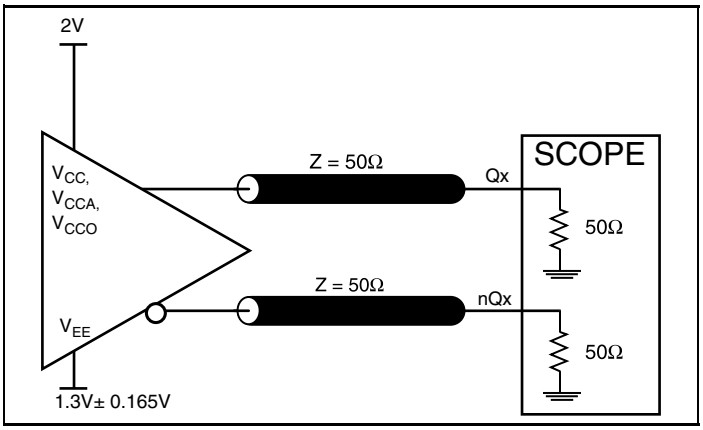
## AC Electrical Characteristics

**Table 6. AC Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

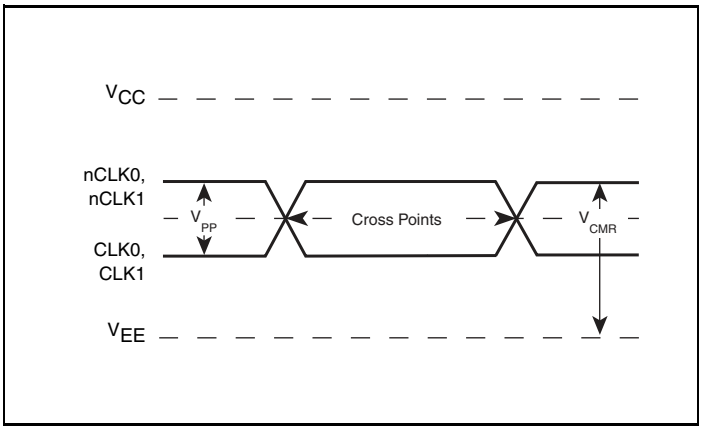
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 350 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | PLL_SEL = 0, f ≤ 350MHz | 3.8 | | 5.1 | ns |
| *t*sk(o) | Output Skew; NOTE 2, 3 | | | | 35 | ps |
| *t*sk(Ø) | Static Phase Offset; NOTE 3, 4 | PLL_SEL = 1 | -70 | 55 | +180 | ps |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 3 | | | | 60 | ps |
| $t_L$ | PLL Lock Time | | | | 1 | ms |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 200 | | 750 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.

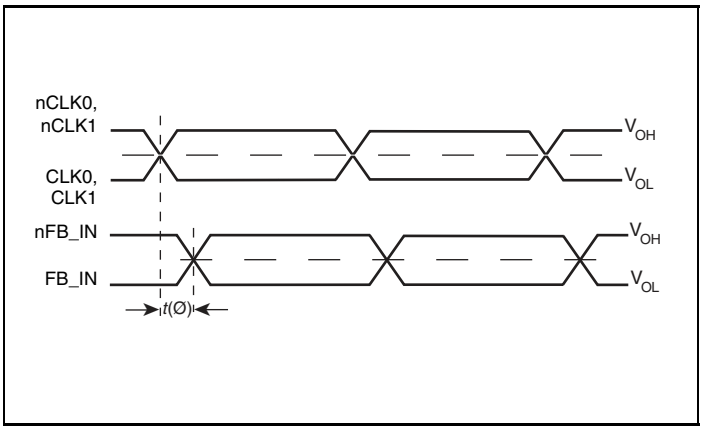
# Parameter Measurement Information



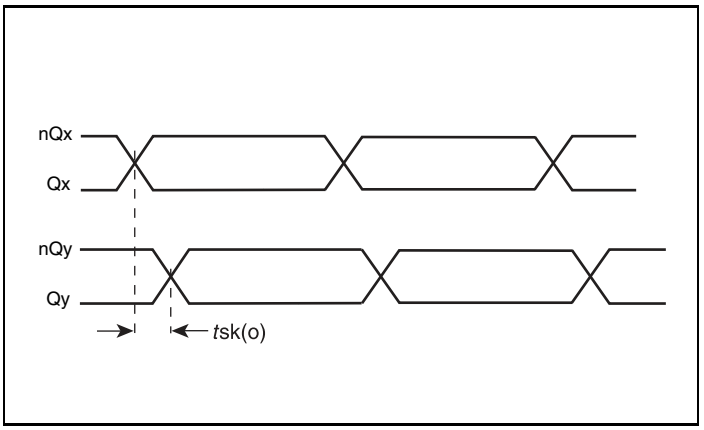

**3.3V Output Load AC Test Circuit**



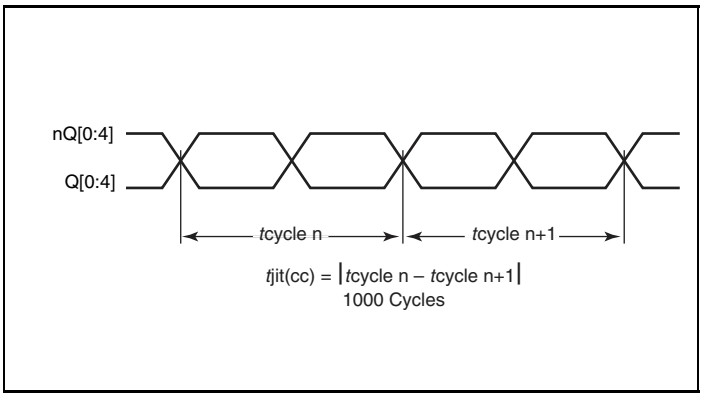

**Differential Input Level**



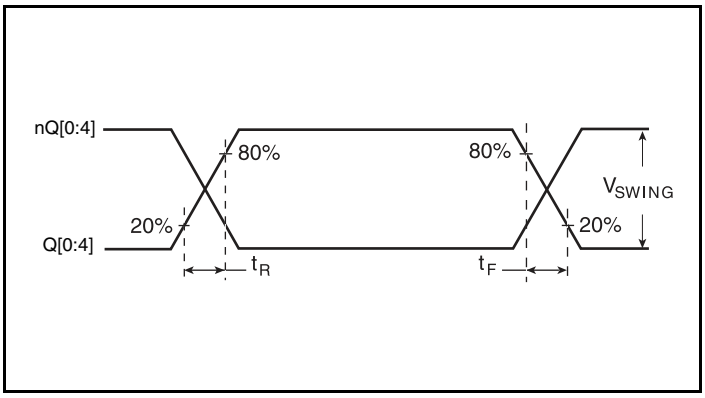

**Phase Jitter and Static Phase Offset**




**Output Skew**

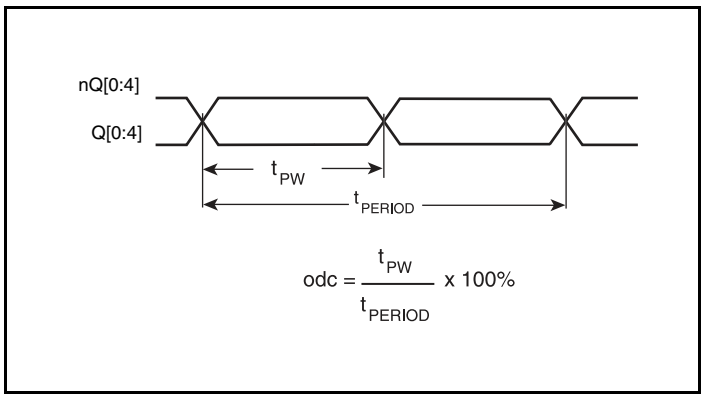



**Cycle-to-Cycle Jitter**

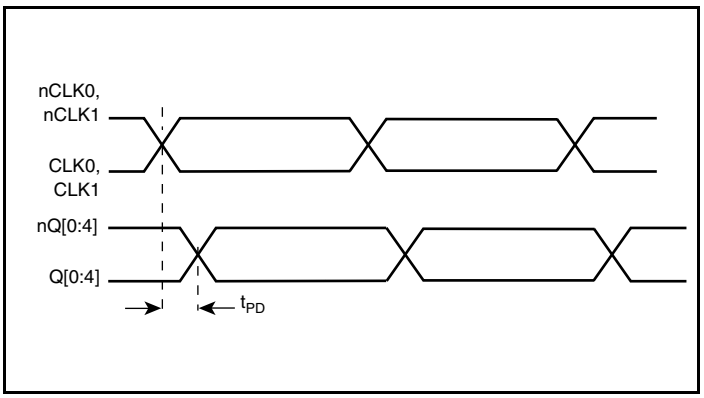



**Output Rise/Fall Time**

## Parameter Measurement Information, continued




**Output Duty Cycle/Pulse Width/Period**




**Propagation Delay**

# Application Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### FB_IN/nFB_IN Inputs

For applications not requiring the use of the differential input, both FB_IN and nFB_IN can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from FB_IN to ground.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter perform- ance, power supply isolation is required. The 8735-31 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC,}$ $V_{CCA}$ and $V_{CCO}$ should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic $V_{CC}$ pin and also shows that $V_{CCA}$ requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the $V_{CCA}$ pin. The 10Ω resistor can also be replaced by a ferrite bead.

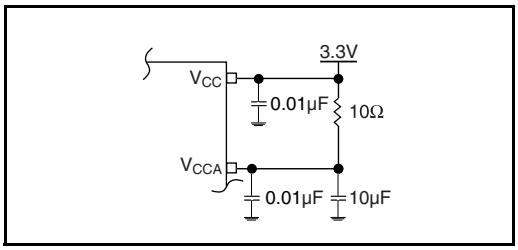



**Figure 1. Power Supply Filtering**

## Wiring the Differential Input to Accept Single Ended Levels

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

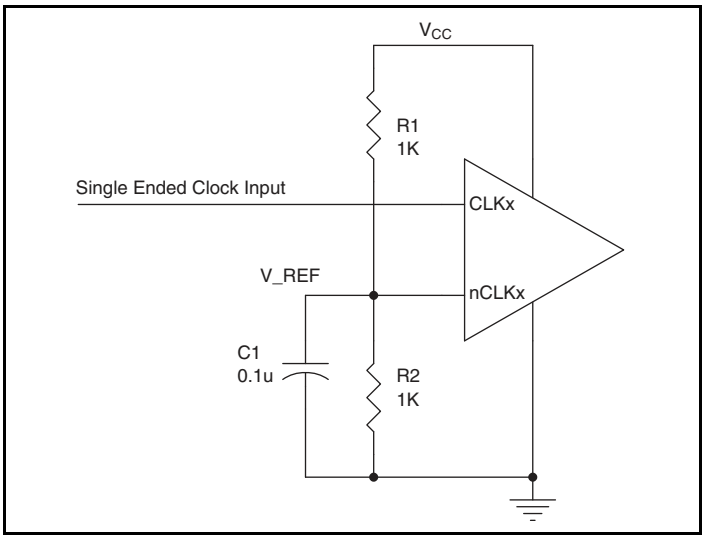



**Figure 2. Single-Ended Signal Driving Differential Input**

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

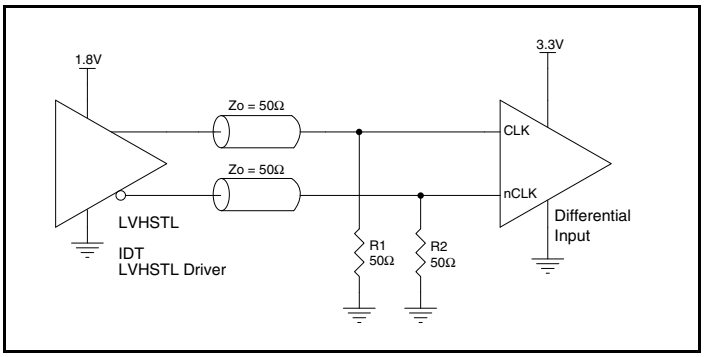



**Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver**

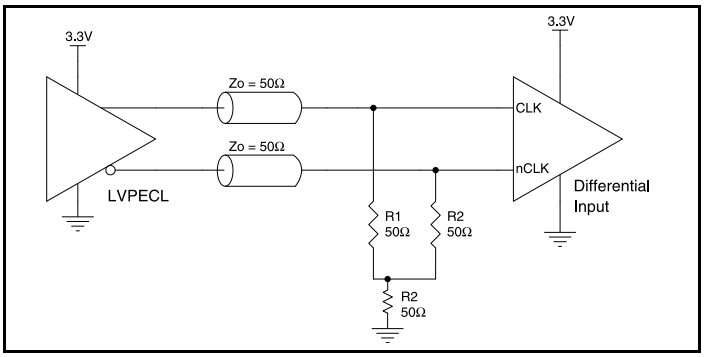



**Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

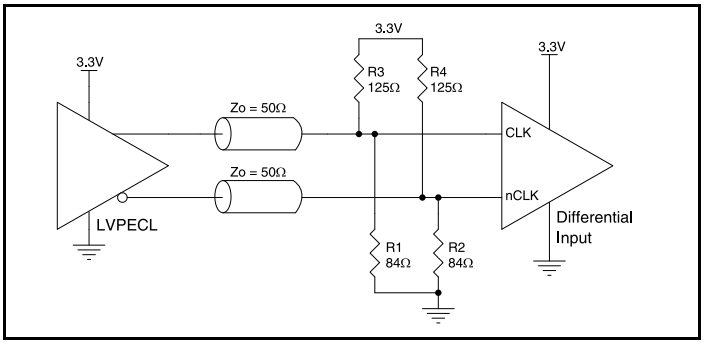



**Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

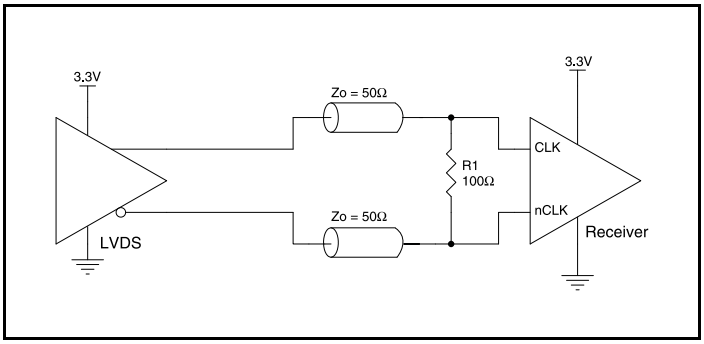



**Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**

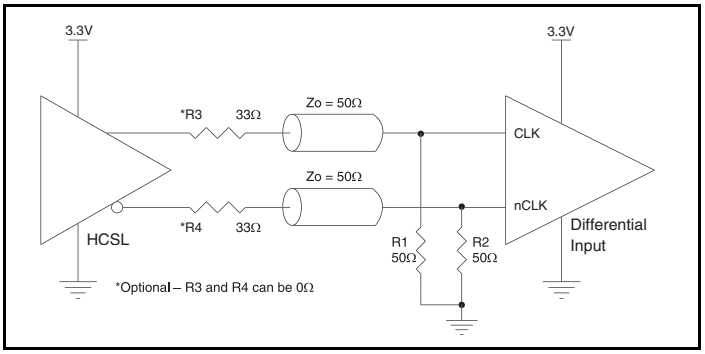



**Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver**

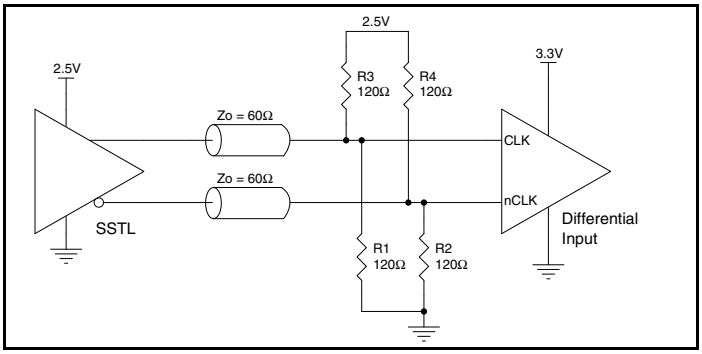



**Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

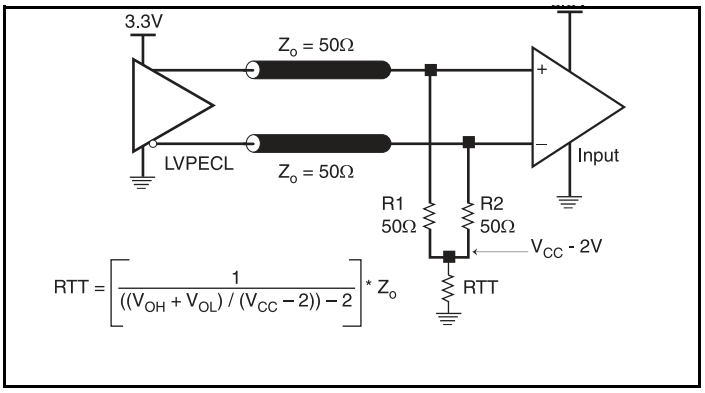



**Figure 4A. 3.3V LVPECL Output Termination**

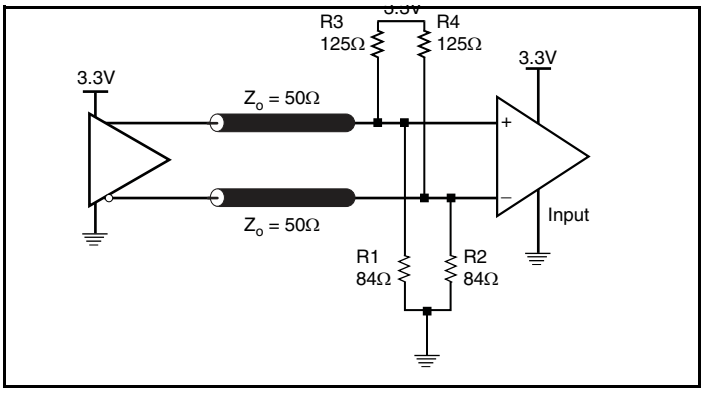
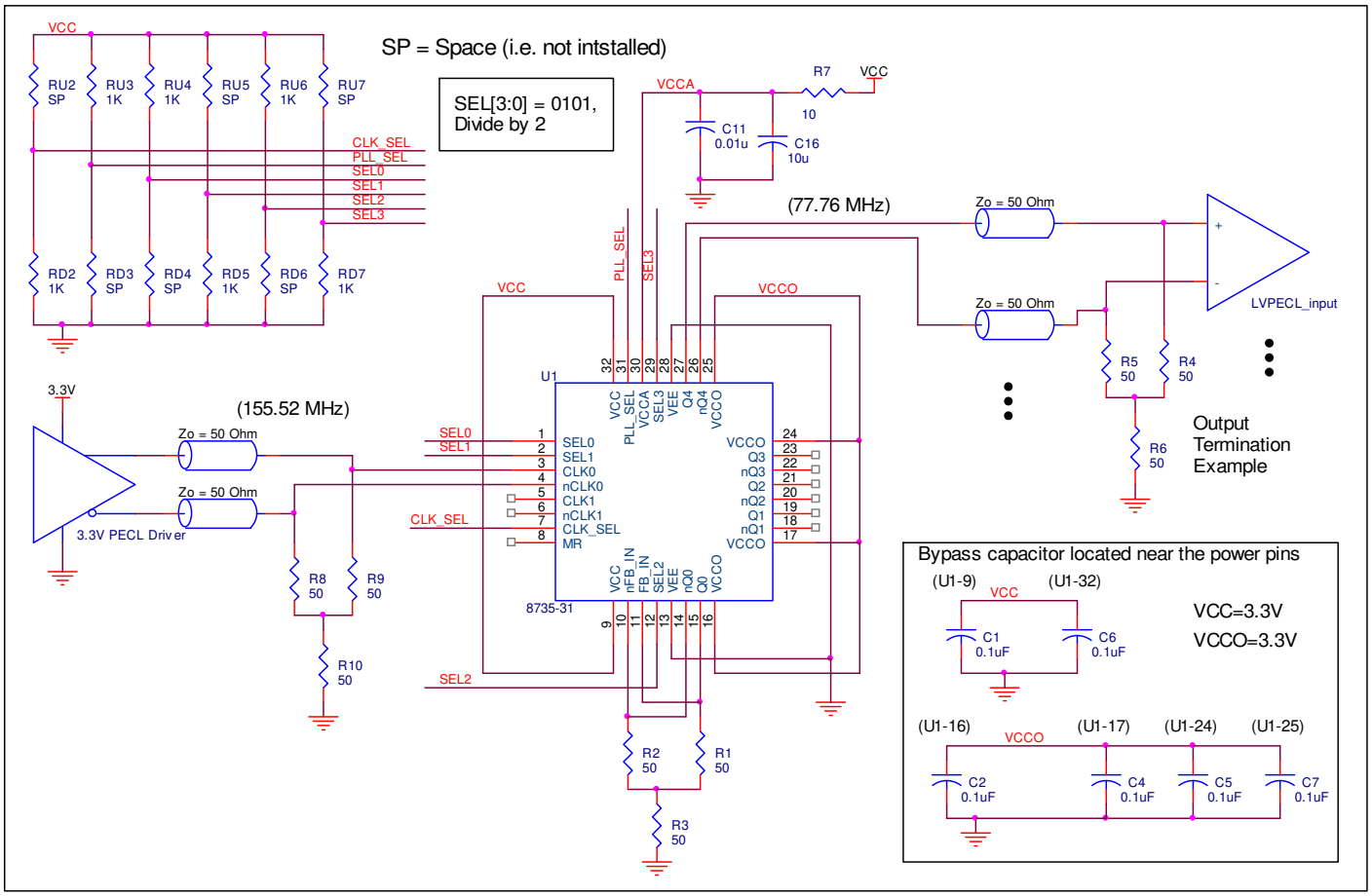



**Figure 4B. 3.3V LVPECL Output Termination**

## Layout Guideline

The schematic of the 8735-31 layout example is shown in *Figure 5A*. The 8735-31 recommended PCB board layout for this example is shown in *Figure 5B*. This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

**Figure 5A. 8735-31 LVPECL Zero Delay Buffer Schematic Example**



The following component footprints are used in this layout example. All the resistors and capacitors are size 0603.

### Power and Grounding

Place the decoupling capacitors C1, C6, C2, C4, C5, and C7, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the $V_{CCA}$ pin as possible.

### Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

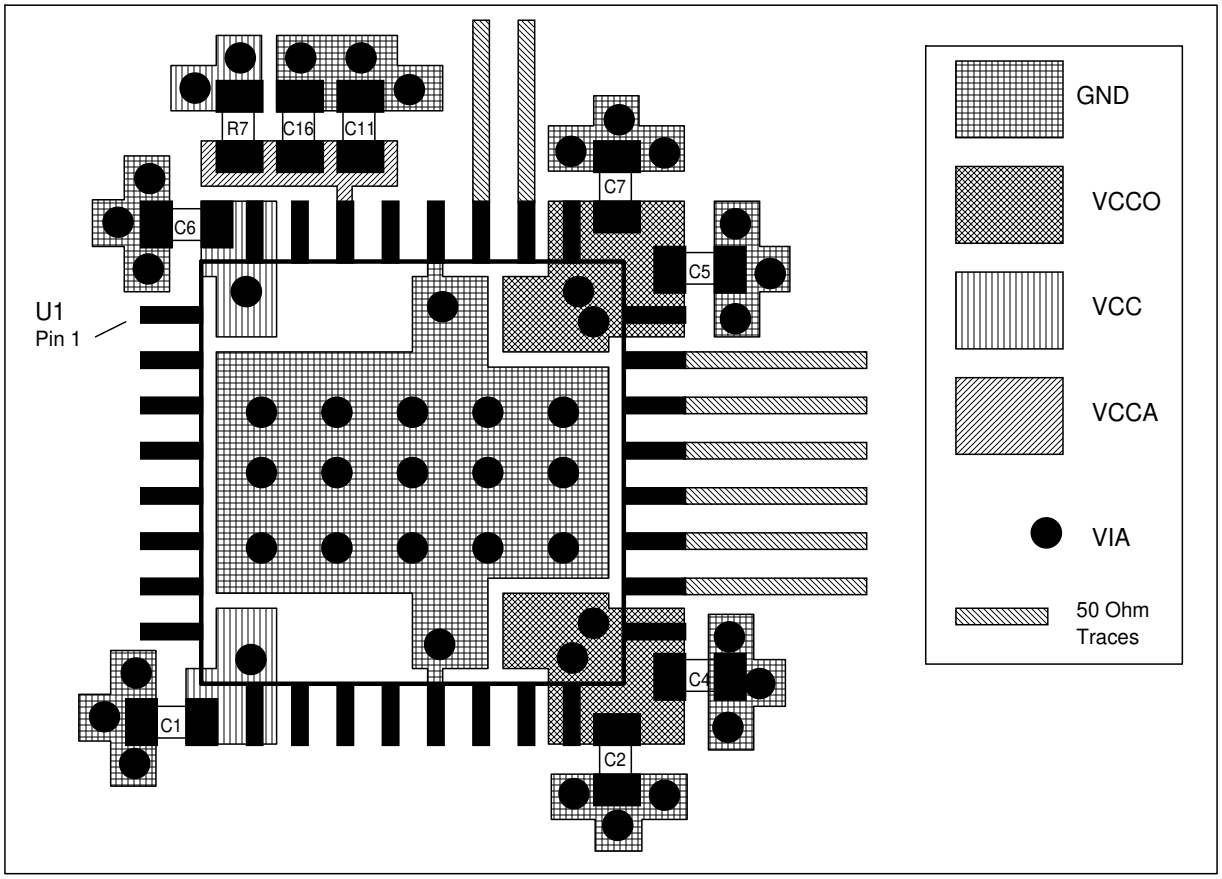



**Figure 5B. PCB Board Layout for 8735-31**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 8735-31.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8735-31 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{CC\_MAX}$ = 3.465V * 150mA = **519.75mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded output pair**
  If all outputs are loaded, the total power is 5 * 30mW = **150mW**

**Total Power**$_{\_MAX}$ = (3.465V, with all outputs switching) = 519.75mW + 150mW = **669.75mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.670W * 42.1°C/W = 98.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 32 Lead LQFP, Forced Convection**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

**3. Calculations and Equations.**

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

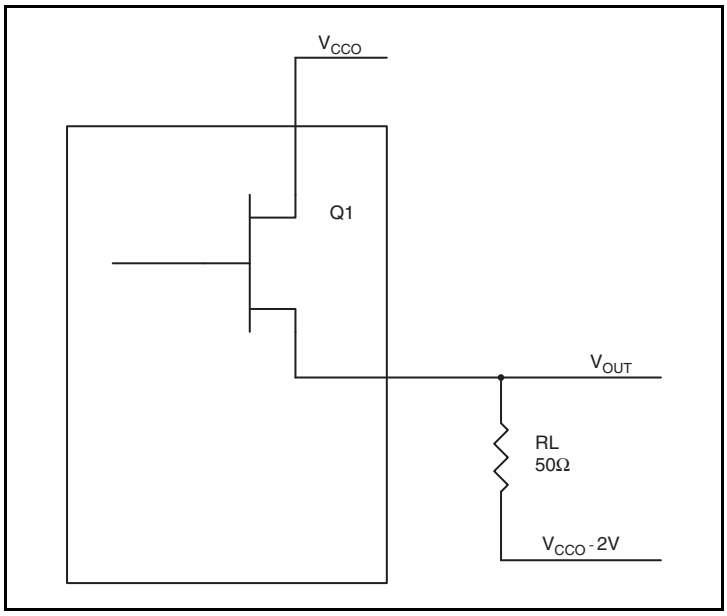



**Figure 6. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

## Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead LQFP**

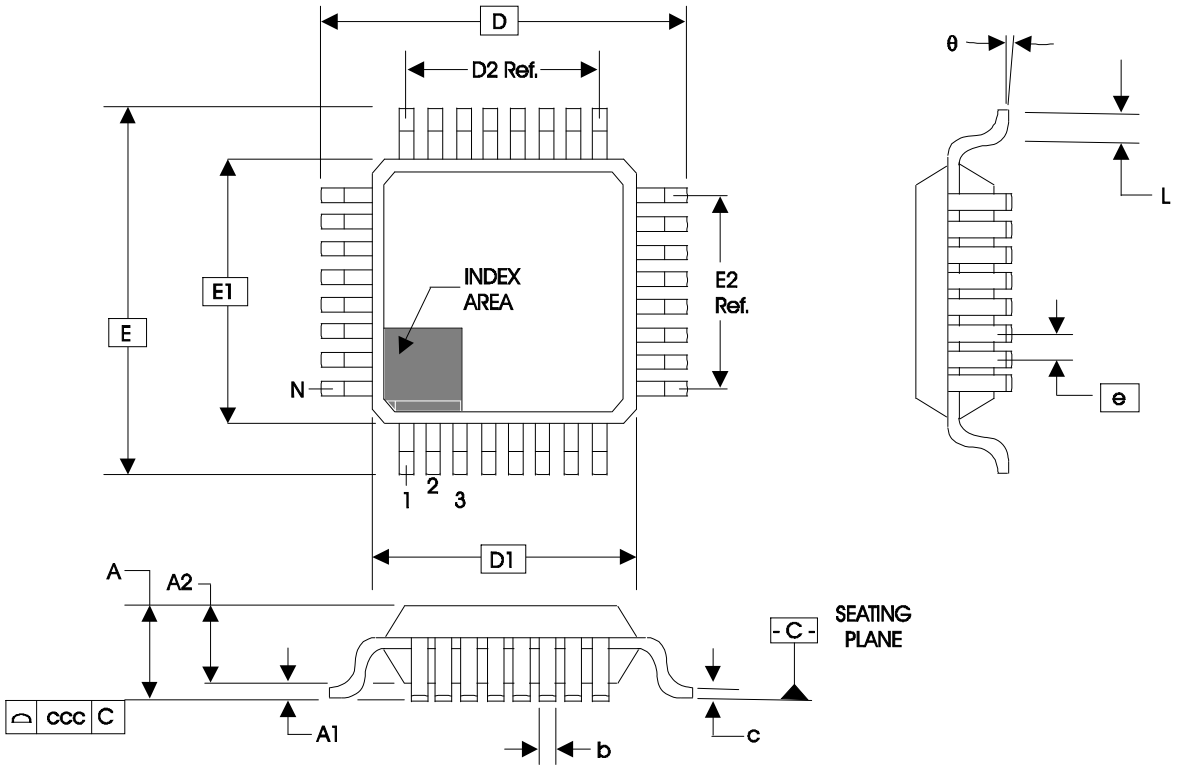
| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

## Transistor Count

The transistor count for 8735-31 is: 2969

# Package Outline and Package Dimensions

### Package Outline - M Suffix for 32 Lead LQFP




### Table 6. Package Dimensions for 32 Lead LQFP

| JEDEC Variation: BBC - HD<br>All Dimensions in Millimeters | | | |
|---|---|---|---|
| **Symbol** | **Minimum** | **Nominal** | **Maximum** |
| **N** | | 32 | |
| **A** | | | 1.60 |
| **A1** | 0.05 | 0.10 | 0.15 |
| **A2** | 1.35 | 1.40 | 1.45 |
| **b** | 0.30 | 0.37 | 0.45 |
| **c** | 0.09 | | 0.20 |
| **D & E** | | 9.00 Basic | |
| **D1 & E1** | | 7.00 Basic | |
| **D2 & E2** | | 5.60 Ref. | |
| **e** | | 0.80 Basic | |
| **L** | 0.45 | 0.60 | 0.75 |
| θ | 0° | | 7° |
| **ccc** | | | 0.10 |

Reference Document: JEDEC Publication 95, MS-026

# Ordering Information

**Table 10. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8735AY-31LF | ICS8735AY31LF | “Lead-Free” 32 Lead LQFP | Tray | 0°C to 70°C |
| 8735AY-31LFT | ICS8735AY31LF | “Lead-Free” 32 Lead LQFP | Tape & Reel | 0°C to 70°C |

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | T10 | 16 | Ordering Information Table - added Lead-Free marking. | 12/19/07 |
| A | T10 | 9<br>11<br>19 | Added *Recommendations for Unused Input and Output Pins section.*<br>Updated *Differential Clock input Interface section.*<br>Ordering Information Table - deleted “ICS” from Part/Order Number. | 2/11/08 |
| B | | 1 | Pin Assignment -due to format conversion dated February 11, 2008 datasheet, corrected typo on pin 19 from nQ1 to Q1 and, pin 10 from FB_IN to nFB_IN. | 2/18/09 |
| B | T10 | 19 | Ordering Information - removed leaded devices.<br>Updated datasheet format. | 7/16/15 |
| B | T10 | 1<br>19 | Features Section - removed reference to leaded packages.<br>Ordering Information - Deleted LF note below table.<br>Updated header and footer. | 1/27/16 |

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