

Fully-Integrated, Fixed-Frequency, Low-Jitter Crystal Oscillator Clock Generator

FEATURES

- Single 3.3-V Supply
- High-Performance Clock Generator, Incorporating Crystal Oscillator Circuitry with Integrated Frequency Synthesizer
- Low Output Jitter: As low as 380 fs (RMS integrated between 10 kHz to 20 MHz)
- Low Phase Noise at 312.5 MHz:
 - Less than -120 dBc/Hz at 10 kHz and -147 dBc/Hz at 10-MHz offset from carrier
- Supports Crystal or LVCMOS Input Frequencies at 31.25 MHz, 33.33 MHz, and 35.42 MHz
- Output Frequencies: 100 MHz, 106.25 MHz, 125 MHz, 156.25 MHz, 212.5 MHz, 250 MHz, and 312.5 MHz
- Differential Low-Voltage Positive Emitter Coupled Logic (LVPECL) Outputs
- Fully-Integrated Voltage-Controlled Oscillator (VCO): Runs from 1.75 GHz to 2.35 GHz
- Typical Power Consumption: 300 mW
- Chip Enable Control Pin
- Available in 4-mm × 4-mm QFN-24 Package
- ESD Protection Exceeds 2 kV (HBM)
- Industrial Temperature Range: -40°C to $+85^{\circ}\text{C}$

APPLICATIONS

- Low-Cost, Low-Jitter Frequency Multiplier

DESCRIPTION

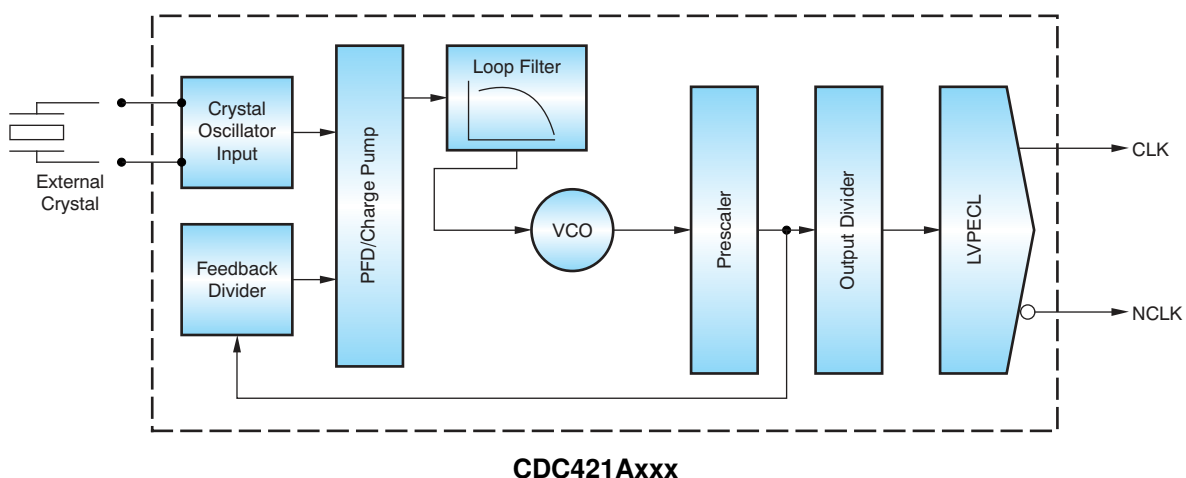
The CDC421Axxx is a high-performance, low-phase-noise clock generator. It has an integrated low-noise, LC-based voltage-controlled oscillator (VCO) that operates within the 1.75 GHz to 2.35 GHz frequency range. It has an integrated crystal oscillator that operates in conjunction with an external AT-cut crystal to produce a stable frequency reference for a phase-locked loop (PLL)-based frequency synthesizer. The output frequency (f_{OUT}) is proportional to the frequency of the input crystal (f_{XTAL}).

The device operates in 3.3-V supply environment and is characterized for operation from -40°C to $+85^{\circ}\text{C}$. The CDC421Axxx is available in a QFN-24 4-mm × 4-mm package.

The CDC421Axxx differs from the CDC421xxx in the following ways:

- **Device Startup**

The CDC421Axxx has an improved startup circuit to enable correct operation for all power-supply ramp times.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS⁽¹⁾

| PRODUCT | INPUT FREQUENCY OR CRYSTAL VALUE (MHz) | OUTPUT FREQUENCY FOR SPECIFIED INPUT FREQUENCY (MHz) | PACKAGE-LEAD | PACKAGE MARKING | ORDERING INFORMATION | TRANSPORT MEDIA, QUANTITY |
|------------|--|--|--------------|-----------------|----------------------|---------------------------|
| CDC421A100 | 33.3333 | 100.00 | QFN-24 | 421A100 | CDC421A100RGET | Tape and reel, 250 |
| | | | | | CDC421A100RGER | Tape and reel, 2500 |
| CDC421A106 | 35.4167 | 106.25 | QFN-24 | 421A106 | CDC421A106RGET | Tape and reel, 250 |
| | | | | | CDC421A106RGER | Tape and reel, 2500 |
| CDC421A125 | 31.2500 | 125.00 | QFN-24 | 421A125 | CDC421A125RGET | Tape and reel, 250 |
| | | | | | CDC421A125RGER | Tape and reel, 2500 |
| CDC421A156 | 31.2500 | 156.25 | QFN-24 | 421A156 | CDC421A156RGET | Tape and reel, 250 |
| | | | | | CDC421A156RGER | Tape and reel, 2500 |
| CDC421A212 | 35.4167 | 212.50 | QFN-24 | 421A212 | CDC421A212RGET | Tape and reel, 250 |
| | | | | | CDC421A212RGER | Tape and reel, 2500 |
| CDC421A250 | 31.2500 | 250.00 | QFN-24 | 421A250 | CDC421A250RGET | Tape and reel, 250 |
| | | | | | CDC421A250RGER | Tape and reel, 2500 |
| CDC421A312 | 31.2500 | 312.50 | QFN-24 | 421A312 | CDC421A312RGET | Tape and reel, 250 |
| | | | | | CDC421A312RGER | Tape and reel, 2500 |

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | CDC421Axxx | UNIT |
|------------------|---|---------------------------------|------|
| V _{CC} | Supply voltage ⁽²⁾ | -0.5 to 4.6 | V |
| V _I | Voltage range for all other input pins ⁽²⁾ | -0.5 to V _{CC} to +0.5 | V |
| I _O | Output current for LVPECL | -50 | mA |
| ESD | Electrostatic discharge (HBM) | 2 | kV |
| T _A | Specified free-air temperature range (no airflow) | -40 to +85 | °C |
| T _J | Maximum junction temperature | +125 | °C |
| T _{STG} | Storage temperature range | -65 to +150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating condition* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

| | | MIN | NOM | MAX | UNIT |
|-----------------|---|-----|------|------|------|
| V _{CC} | Supply voltage | 3.0 | 3.30 | 3.60 | V |
| T _A | Ambient temperature (no airflow, no heatsink) | -40 | | +85 | °C |

ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | CDC421Axxx | | | UNIT |
|----------------------|------------------------------------|--|---------------------|---------------------|---------|
| | | MIN | TYP | MAX | |
| V_{CC} | Supply voltage | 3.00 | 3.30 | 3.60 | V |
| I_{VCC} | Total current | | 91 | 110 | mA |
| LVPECL OUTPUT | | | | | |
| f_{CLK} | Output frequency | | 100 | 312.5 | MHz |
| V_{OH} | LVPECL high-level output voltage | | $V_{CC} - 1.20$ | $V_{CC} - 0.81$ | V |
| V_{OL} | LVPECL low-level output voltage | | $V_{CC} - 2.17$ | $V_{CC} - 1.36$ | V |
| $ V_{OD} $ | LVPECL differential output voltage | | 407 | 1076 | mV |
| t_R | Output rise time | 20% to 80% of $V_{OUT(PP)}$ | | 230 | ps |
| t_F | Output fall time | 20% to 80% of $V_{OUT(PP)}$ | | 230 | ps |
| | Duty cycle of the output waveform | | 45 | 55 | % |
| t_j | RMS jitter | 10 kHz to 20 MHz | | 1 | ps, RMS |
| LVCMOS INPUT | | | | | |
| $V_{IL, CMOS}$ | Low-level CMOS input voltage | $V_{CC} = 3.3 V$ | | $0.3 \times V_{CC}$ | V |
| $V_{IH, CMOS}$ | High-level CMOS input voltage | $V_{CC} = 3.3 V$ | $0.7 \times V_{CC}$ | | V |
| $I_{L, CMOS}$ | Low-level CMOS input current | $V_{CC} = V_{CC, max}, V_{IL} = 0.0 V$ | | -200 | μA |
| $I_{H, CMOS}$ | High-level CMOS input current | $V_{CC} = V_{CC, min}, V_{IH} = 3.7 V$ | | 200 | μA |

FUNCTIONAL BLOCK DIAGRAM

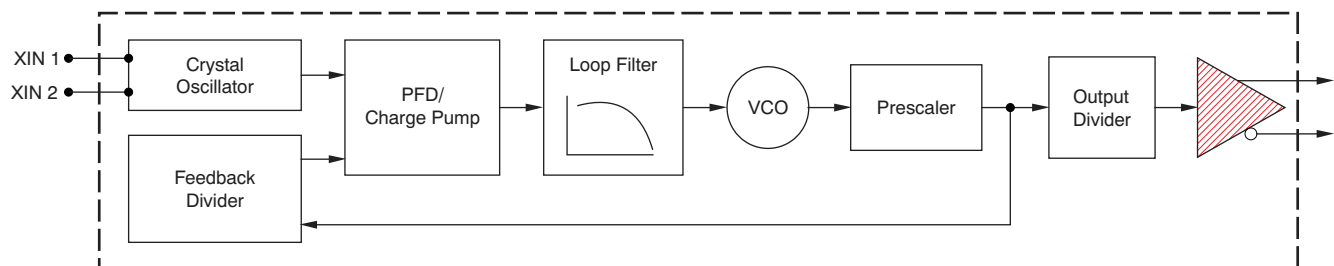
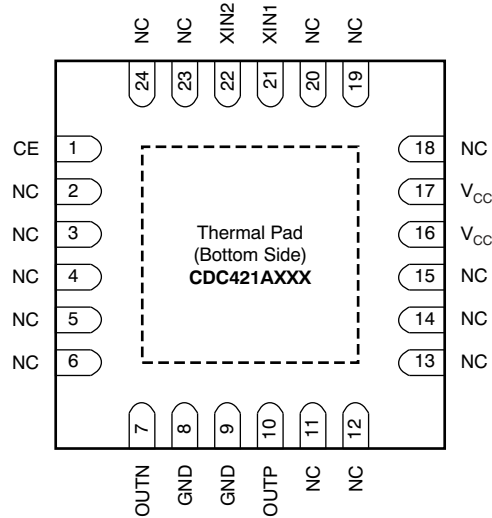


Figure 1. CDC421Axxx: High-Level Block Diagram

DEVICE INFORMATION

**RGE PACKAGE
QFN-24
(TOP VIEW)**



CDC421Axxx Pin Descriptions

| TERMINAL | | TYPE | ESD PROTECTION | DESCRIPTION |
|-----------------|---------------------------|--------|----------------|---|
| NAME | NO. | | | |
| V _{CC} | 16, 17 | Power | Y | 3.3-V power supply |
| GND | 8, 9 | Ground | Y | Ground |
| XIN1 | 21 | I | Y | In crystal input mode, connect XIN1 to one end of the crystal and XIN2 to the other end of the crystal. In LVC MOS single-ended driven mode, XIN1 (pin 21) acts as input reference and XIN2 should connect to GND. |
| XIN2 | 22 | I | N | |
| CE | 1 | I | Y | Chip enable (LVC MOS input) CE = 1 enables the device and the outputs. CE = 0 disables all current sources (LVPECLP = LVPECLN = Hi-Z). |
| OUTP | 10 | O | Y | High-speed positive differential LVPECL output. (Outputs are enabled by CE pin.) |
| OUTN | 7 | O | Y | High-speed negative differential LVPECL output. (Outputs are enabled by CE pin.) |
| NC | 2–6, 11–15, 18–20, 23, 24 | — | Y | TI test pin. Do not connect; leave floating. |

JITTER CHARACTERISTICS IN INPUT CLOCK MODE

Jitter characterization tests are performed using an LVCMOS input signal driving the CDC421Axxx device, as Figure 2 illustrates.

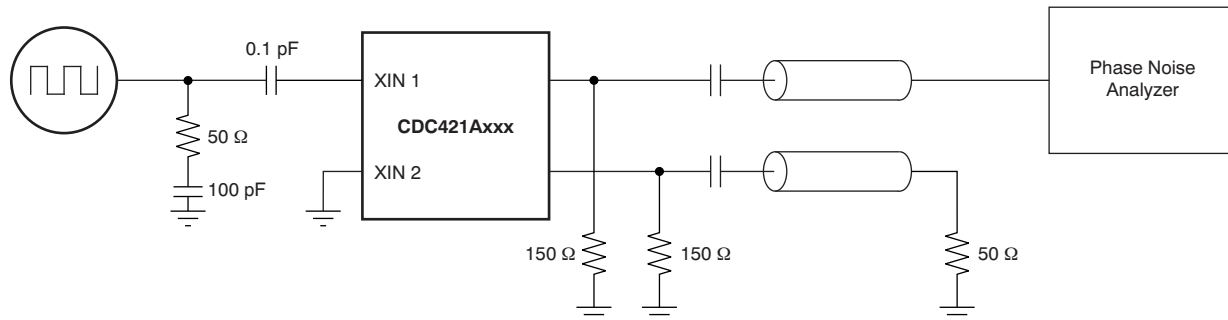


Figure 2. Jitter Test Configuration for an LVTTTL Input Driving CDC421Axxx

When the CDC421Axxx is referenced by an external, clean LVCMOS input of 31.25 MHz, 33.33 MHz, and 35.4167 MHz, Table 1 to Table 7 list the measured SSB phase noise of all the outputs supported by the CDC421Axxx device (100 MHz, 106.25 MHz, 125 MHz, 156.25 MHz, 212.5 MHz, 250 MHz, and 312.5 MHz) from 100 Hz to 20 MHz from the carrier.

Table 1. Phase Noise Data with LVCMOS Input of 33.3333 MHz and LVPECL Output at 100.00 MHz⁽¹⁾

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-------|-----|--------|
| phn ₁₀₀ | Phase noise at 100 Hz | | -111 | | dBc/Hz |
| phn _{1k} | Phase noise at 1 kHz | | -121 | | dBc/Hz |
| phn _{10k} | Phase noise at 10 kHz | | -131 | | dBc/Hz |
| phn _{100k} | Phase noise at 100 kHz | | -133 | | dBc/Hz |
| phn _{1M} | Phase noise at 1 MHz | | -142 | | dBc/Hz |
| phn _{10M} | Phase noise at 10 MHz | | -149 | | dBc/Hz |
| phn _{20M} | Phase noise at 20 MHz | | -149 | | dBc/Hz |
| J _{RMS} | RMS jitter integrated from 12 kHz to 20 MHz | | 507 | | fs |
| T _j | Total jitter | | 35.33 | | ps |
| D _j | Deterministic jitter | | 11.54 | | ps |

(1) Phase noise specifications under following conditions: input frequency = 33.3333 MHz, output frequency = 100.00 MHz.

Table 2. Phase Noise Data with LVCMOS Input of 35.4167 MHz and LVPECL Output at 106.25 MHz⁽¹⁾

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-------|-----|--------|
| phn ₁₀₀ | Phase noise at 100 Hz | | -112 | | dBc/Hz |
| phn _{1k} | Phase noise at 1 kHz | | -121 | | dBc/Hz |
| phn _{10k} | Phase noise at 10 kHz | | -125 | | dBc/Hz |
| phn _{100k} | Phase noise at 100 kHz | | -129 | | dBc/Hz |
| phn _{1M} | Phase noise at 1 MHz | | -142 | | dBc/Hz |
| phn _{10M} | Phase noise at 10 MHz | | -151 | | dBc/Hz |
| phn _{20M} | Phase noise at 20 MHz | | -151 | | dBc/Hz |
| J _{RMS} | RMS jitter integrated from 12 kHz to 20 MHz | | 530 | | fs |
| T _j | Total jitter | | 30.39 | | ps |
| D _j | Deterministic jitter | | 11 | | ps |

(1) Phase noise specifications under following conditions: input frequency = 35.4167 MHz, output frequency = 106.25 MHz.

Table 3. Phase Noise Data with LVCMOS Input of 31.2500 MHz and LVPECL Output at 125.00 MHz⁽¹⁾

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-------|-----|--------|
| phn ₁₀₀ | Phase noise at 100 Hz | | -108 | | dBc/Hz |
| phn _{1k} | Phase noise at 1 kHz | | -118 | | dBc/Hz |
| phn _{10k} | Phase noise at 10 kHz | | -127 | | dBc/Hz |
| phn _{100k} | Phase noise at 100 kHz | | -130 | | dBc/Hz |
| phn _{1M} | Phase noise at 1 MHz | | -139 | | dBc/Hz |
| phn _{10M} | Phase noise at 10 MHz | | -147 | | dBc/Hz |
| phn _{20M} | Phase noise at 20 MHz | | -147 | | dBc/Hz |
| J _{RMS} | RMS jitter integrated from 12 kHz to 20 MHz | | 529 | | fs |
| T _j | Total jitter | | 47.47 | | ps |
| D _j | Deterministic jitter | | 25.2 | | ps |

(1) Phase noise specifications under following conditions: input frequency = 31.2500 MHz, output frequency = 125.00 MHz.

Table 4. Phase Noise Data with LVCMOS Input of 31.2500 MHz and LVPECL Output at 156.25 MHz⁽¹⁾

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-------|-----|--------|
| phn ₁₀₀ | Phase noise at 100 Hz | | -106 | | dBc/Hz |
| phn _{1k} | Phase noise at 1 kHz | | -117 | | dBc/Hz |
| phn _{10k} | Phase noise at 10 kHz | | -126 | | dBc/Hz |
| phn _{100k} | Phase noise at 100 kHz | | -128 | | dBc/Hz |
| phn _{1M} | Phase noise at 1 MHz | | -139 | | dBc/Hz |
| phn _{10M} | Phase noise at 10 MHz | | -147 | | dBc/Hz |
| phn _{20M} | Phase noise at 20 MHz | | -147 | | dBc/Hz |
| J _{RMS} | RMS jitter integrated from 12 kHz to 20 MHz | | 472 | | fs |
| T _j | Total jitter | | 31.54 | | ps |
| D _j | Deterministic jitter | | 9.12 | | ps |

(1) Phase noise specifications under following conditions: input frequency = 31.2500 MHz, output frequency = 156.25 MHz.

Table 5. Phase Noise Data with LVCMOS Input of 35.4167 MHz and LVPECL Output at 212.50 MHz⁽¹⁾

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-------|-----|--------|
| phn ₁₀₀ | Phase noise at 100 Hz | | -105 | | dBc/Hz |
| phn _{1k} | Phase noise at 1 kHz | | -115 | | dBc/Hz |
| phn _{10k} | Phase noise at 10 kHz | | -119 | | dBc/Hz |
| phn _{100k} | Phase noise at 100 kHz | | -123 | | dBc/Hz |
| phn _{1M} | Phase noise at 1 MHz | | -135 | | dBc/Hz |
| phn _{10M} | Phase noise at 10 MHz | | -148 | | dBc/Hz |
| phn _{20M} | Phase noise at 20 MHz | | -148 | | dBc/Hz |
| J _{RMS} | RMS jitter integrated from 12 kHz to 20 MHz | | 512 | | fs |
| T _j | Total jitter | | 33.96 | | ps |
| D _j | Deterministic jitter | | 13.78 | | ps |

(1) Phase noise specifications under following conditions: input frequency = 35.4167 MHz, output frequency = 212.50 MHz.

Table 6. Phase Noise Data with LVCMOS Input of 31.2500 MHz and LVPECL Output at 250.00 MHz⁽¹⁾

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-------|-----|--------|
| phn ₁₀₀ | Phase noise at 100 Hz | | -105 | | dBc/Hz |
| phn _{1k} | Phase noise at 1 kHz | | -112 | | dBc/Hz |
| phn _{10k} | Phase noise at 10 kHz | | -121 | | dBc/Hz |
| phn _{100k} | Phase noise at 100 kHz | | -124 | | dBc/Hz |
| phn _{1M} | Phase noise at 1 MHz | | -134 | | dBc/Hz |
| phn _{10M} | Phase noise at 10 MHz | | -148 | | dBc/Hz |
| phn _{20M} | Phase noise at 20 MHz | | -149 | | dBc/Hz |
| J _{RMS} | RMS jitter integrated from 12 kHz to 20 MHz | | 420 | | fs |
| T _j | Total jitter | | 36.98 | | ps |
| D _j | Deterministic jitter | | 18.52 | | ps |

(1) Phase noise specifications under following conditions: input frequency = 31.2500 MHz, output frequency = 250.00 MHz.

Table 7. Phase Noise Data with LVCMOS Input of 31.2500 MHz and LVPECL Output at 312.50 MHz⁽¹⁾

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-------|-----|--------|
| phn ₁₀₀ | Phase noise at 100 Hz | | -102 | | dBc/Hz |
| phn _{1k} | Phase noise at 1 kHz | | -111 | | dBc/Hz |
| phn _{10k} | Phase noise at 10 kHz | | -120 | | dBc/Hz |
| phn _{100k} | Phase noise at 100 kHz | | -123 | | dBc/Hz |
| phn _{1M} | Phase noise at 1 MHz | | -135 | | dBc/Hz |
| phn _{10M} | Phase noise at 10 MHz | | -147 | | dBc/Hz |
| phn _{20M} | Phase noise at 20 MHz | | -147 | | dBc/Hz |
| J _{RMS} | RMS jitter integrated from 12 kHz to 20 MHz | | 378 | | fs |
| T _j | Total jitter | | 29.82 | | ps |
| D _j | Deterministic jitter | | 11 | | ps |

(1) Phase noise specifications under following conditions: input frequency = 31.2500 MHz, output frequency = 312.50 MHz.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CDC421A100RGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 100 | Samples |
| CDC421A100RGET | ACTIVE | VQFN | RGE | 24 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 100 | Samples |
| CDC421A106RGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 106 | Samples |
| CDC421A106RGET | ACTIVE | VQFN | RGE | 24 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 106 | Samples |
| CDC421A125RGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 125 | Samples |
| CDC421A125RGET | ACTIVE | VQFN | RGE | 24 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 125 | Samples |
| CDC421A156RGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 156 | Samples |
| CDC421A156RGET | ACTIVE | VQFN | RGE | 24 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 156 | Samples |
| CDC421A212RGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 212 | Samples |
| CDC421A212RGET | ACTIVE | VQFN | RGE | 24 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 212 | Samples |
| CDC421A250RGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 250 | Samples |
| CDC421A250RGET | ACTIVE | VQFN | RGE | 24 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 250 | Samples |
| CDC421A312RGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 312 | Samples |
| CDC421A312RGET | ACTIVE | VQFN | RGE | 24 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 421A 312 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDC421A100RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A100RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A106RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A106RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A125RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A125RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A156RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A156RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A212RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A212RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A250RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A250RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A312RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDC421A312RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

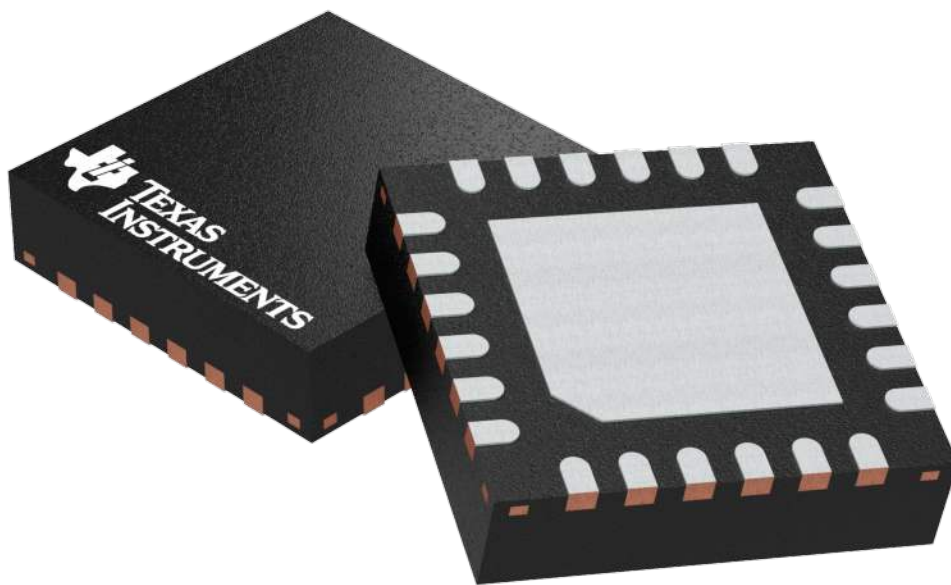
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDC421A100RGER | VQFN | RGE | 24 | 3000 | 356.0 | 356.0 | 35.0 |
| CDC421A100RGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| CDC421A106RGER | VQFN | RGE | 24 | 3000 | 356.0 | 356.0 | 35.0 |
| CDC421A106RGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| CDC421A125RGER | VQFN | RGE | 24 | 3000 | 356.0 | 356.0 | 35.0 |
| CDC421A125RGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| CDC421A156RGER | VQFN | RGE | 24 | 3000 | 356.0 | 356.0 | 35.0 |
| CDC421A156RGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| CDC421A212RGER | VQFN | RGE | 24 | 3000 | 356.0 | 356.0 | 35.0 |
| CDC421A212RGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| CDC421A250RGER | VQFN | RGE | 24 | 3000 | 356.0 | 356.0 | 35.0 |
| CDC421A250RGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| CDC421A312RGER | VQFN | RGE | 24 | 3000 | 356.0 | 356.0 | 35.0 |
| CDC421A312RGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |

RGE 24

GENERIC PACKAGE VIEW

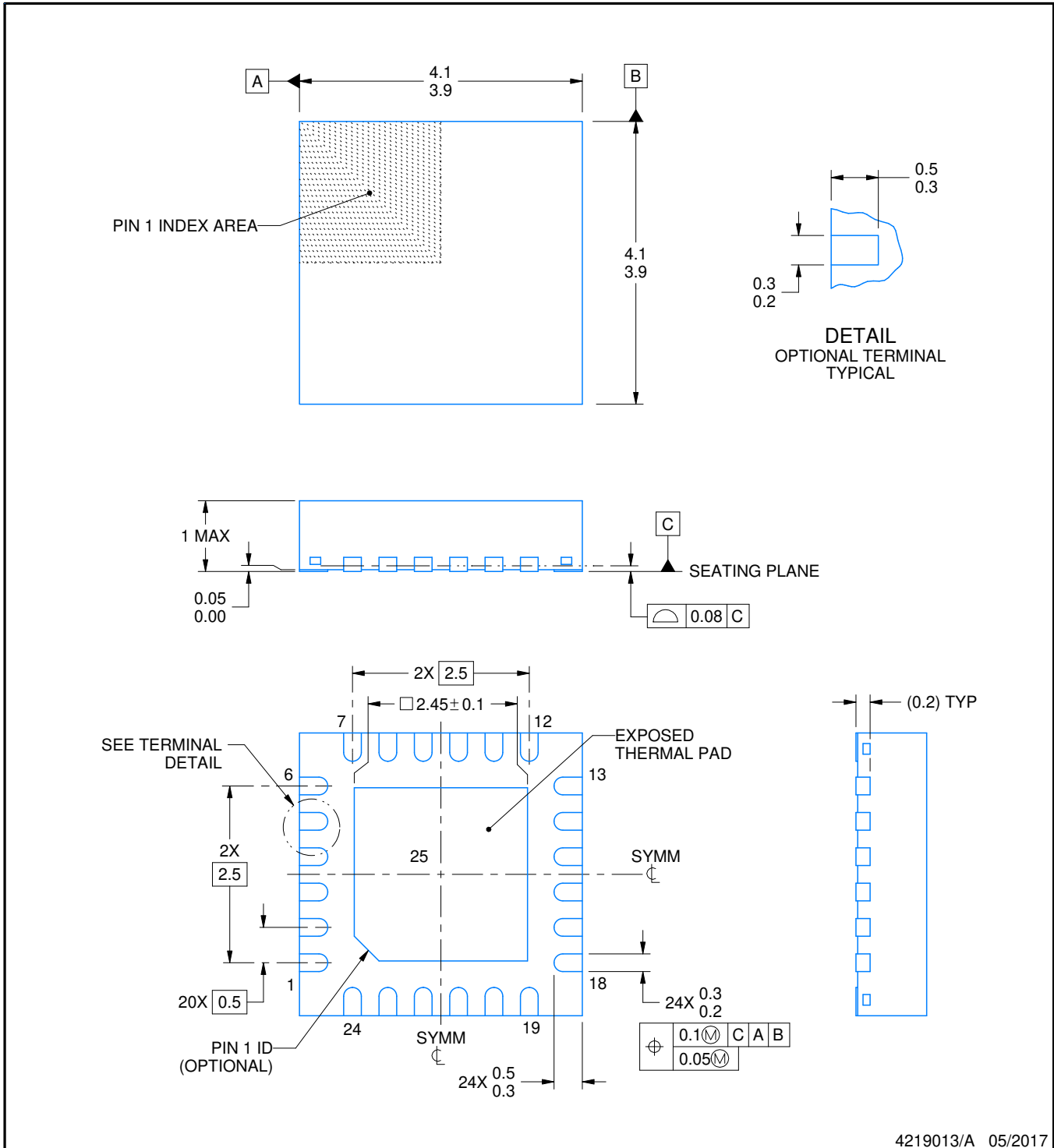
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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NOTES:

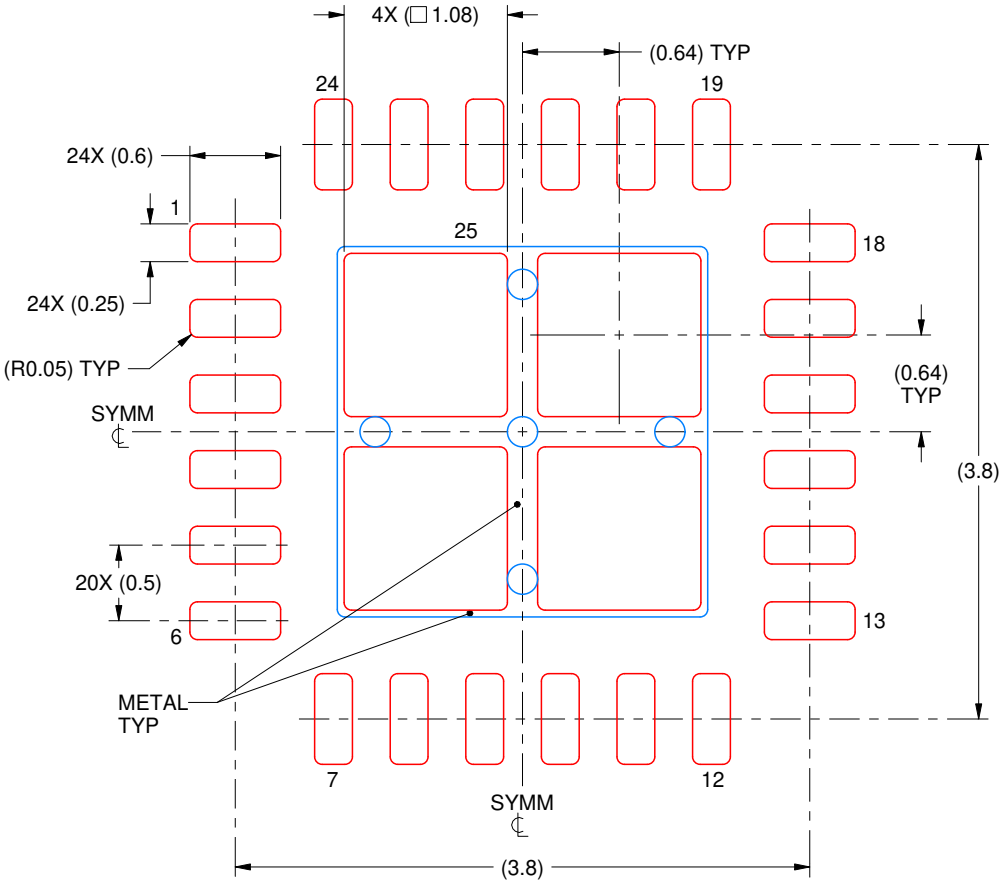
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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