- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Unregulated Battery Operation Down To 2.7 V**
- **Buffered Clock and Direct-Clear Inputs**
- **Individual Data Input to Each Flip-Flop**

- **I_{off} Supports Partial-Power-Down-Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

SN54LVTH273 . . . J PACKAGE
SN74LVTH273 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)

```
         ___
 CLR [ 1      20 ] VCC
  1Q [ 2      19 ] 8Q
  1D [ 3      18 ] 8D
  2D [ 4      17 ] 7D
  2Q [ 5      16 ] 7Q
  3Q [ 6      15 ] 6Q
  3D [ 7      14 ] 6D
  4D [ 8      13 ] 5D
  4Q [ 9      12 ] 5Q
 GND [ 10     11 ] CLK
```
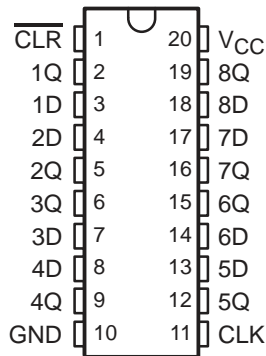
SN54LVTH273 . . . FK PACKAGE
(TOP VIEW)

```
        1D  1Q  CLR VCC 8Q
         3   2   1  20  19
 2D [ 4                18 ] 8D
 2Q [ 5                17 ] 7D
 3Q [ 6                16 ] 7Q
 3D [ 7                15 ] 6Q
 4D [ 8                14 ] 6D
         9  10  11  12  13
        4Q  GND CLK 5Q  5D
```
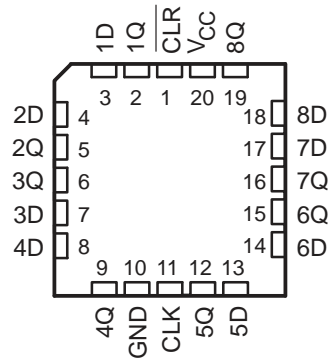
description/ordering information

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH273 devices are positive-edge-triggered flip-flops with a direct-clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – DW	Tube	SN74LVTH273DW	LVTH273
		Tape and reel	SN74LVTH273DWR	
	SOP – NS	Tape and reel	SN74LVTH273NSR	LVTH273
	SSOP – DB	Tape and reel	SN74LVTH273DBR	LXH273
	TSSOP – PW	Tube	SN74LVTH273PW	LXH273
		Tape and reel	SN74LVTH273PWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54LVTH273J	SNJ54LVTH273J
	LCCC – FK	Tube	SNJ54LVTH273FK	SNJ54LVTH273FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

## description/ordering information (continued)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q_0

logic diagram (positive logic)
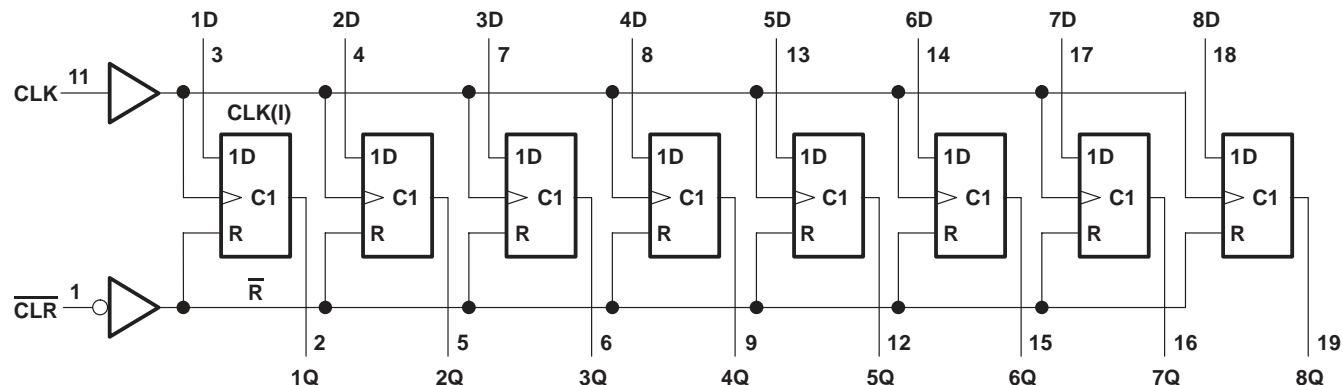
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the power-off state, V_O (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O: SN54LVTH273 .... 96 mA
                                     SN74LVTH273 .... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH273 .... 48 mA
                                       SN74LVTH273 .... 64 mA
Input clamp current, I_{IK} (V_I < 0) .... –50 mA
Output clamp current, I_{OK} (V_O < 0) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package .... 70°C/W
                                    DW package .... 58°C/W
                                    NS package .... 60°C/W
                                    PW package .... 83°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		SN54LVTH273 MIN	SN54LVTH273 MAX	SN74LVTH273 MIN	SN74LVTH273 MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

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3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH273 MIN	TYP†	MAX	SN74LVTH273 MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = −24 mA	2						
			I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	µA
	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	−75			−75			
		V_{CC} = 3.6 V‡,	V_I = 0 to 3.6 V						500 −750	
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
ΔI_{CC}§		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			4			4		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH273 V_{CC} = 3.3 V ± 0.3 V MIN	MAX	V_{CC} = 2.7 V MIN	MAX	SN74LVTH273 V_{CC} = 3.3 V ± 0.3 V MIN	MAX	V_{CC} = 2.7 V MIN	MAX	UNIT
f_{clock}	Clock frequency			150				150			MHz
t_w	Pulse duration		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	Data high or low before CLK↑	2.3		2.7		2.3		2.7		ns
		$\overline{CLR}$ high before CLK↑	2.3		2.7		2.3		2.7		
t_h	Hold time, data high or low after CLK↑		0		0		0		0		ns

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH273 V_{CC} = 3.3 V $\pm$ 0.3 V		SN54LVTH273 V_{CC} = 2.7 V		SN74LVTH273 V_{CC} = 3.3 V $\pm$ 0.3 V			SN74LVTH273 V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150				150					MHz
t_{PLH}	CLK	Any Q	1.6	5		5.6	1.7	3.2	4.9		5.5	ns
t_{PHL}	CLK	Any Q	1.8	4.9		5.2	1.9	3.2	4.8		5.1	ns
t_{PHL}	$\overline{CLR}$	Any Q	1.5	4.4		4.8	1.6	2.7	4.3		4.7	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
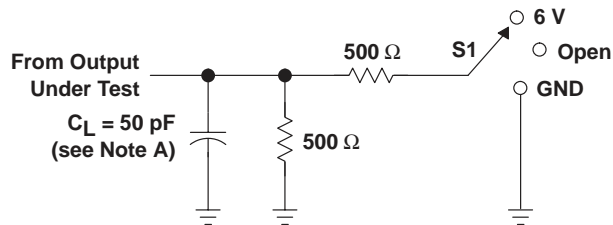
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION
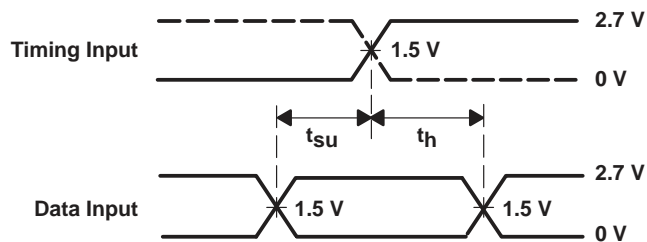
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
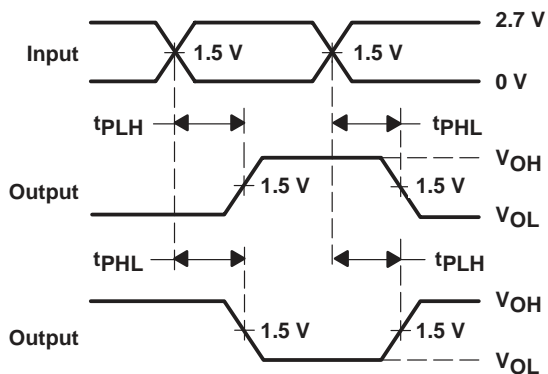
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
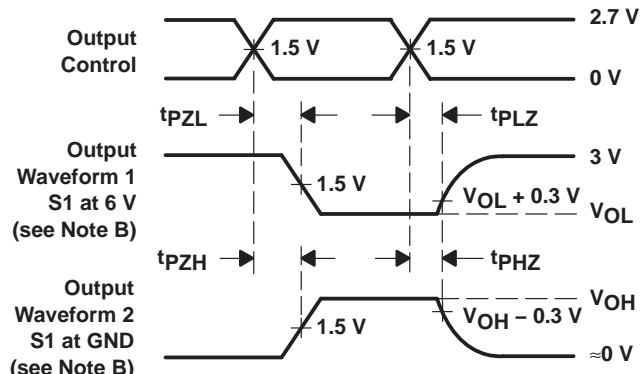
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
   D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVTH273DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH273	Samples
SN74LVTH273DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH273	Samples
SN74LVTH273DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH273	Samples
SN74LVTH273DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH273	Samples
SN74LVTH273NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH273	Samples
SN74LVTH273PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH273	Samples
SN74LVTH273PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LXH273	Samples
SN74LVTH273PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH273	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVTH273 :

● Enhanced Product : SN74LVTH273-EP

NOTE: Qualified Version Definitions:

   ● Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVTH273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVTH273NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVTH273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVTH273PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH273DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LVTH273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVTH273NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVTH273PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LVTH273PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVTH273DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVTH273PW	PW	TSSOP	20	70	530	10.2	3600	3.5

C SEATING PLANE

0.1 C

6.6 / 6.2 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

2X 5.85

6.6 / 6.4 NOTE 3

10

11

20X 0.30 / 0.19

B

4.5 / 4.3 NOTE 4

⊕ 0.1 Ⓜ C A B

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25 GAGE PLANE

0.15 / 0.05

0.75 / 0.50

0° -8°

DETAIL A
TYPICAL

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

1

20X (0.45)

SYMM

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

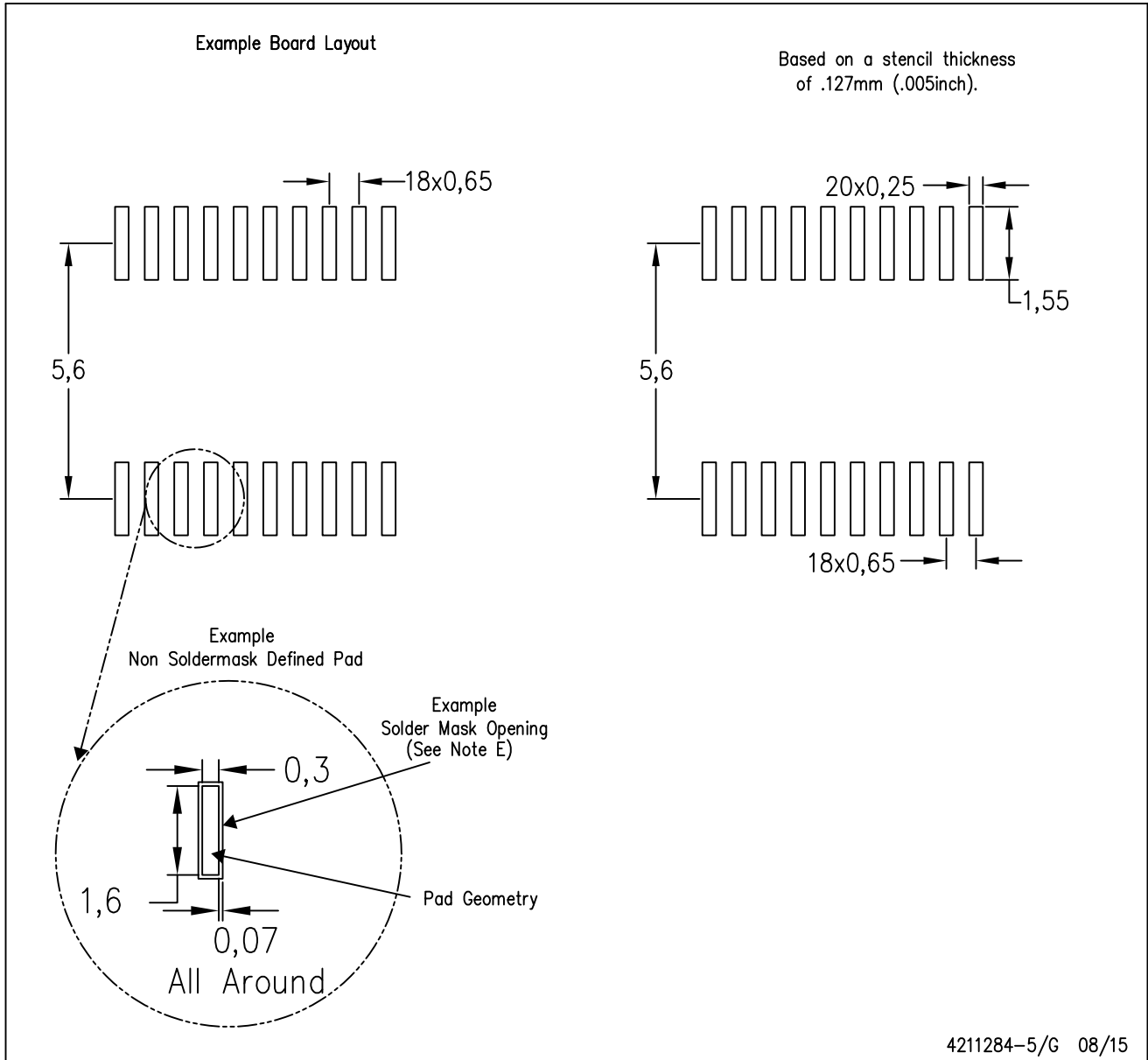8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
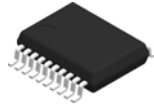
PW (R-PDSO-G20) PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284-5/G 08/15

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
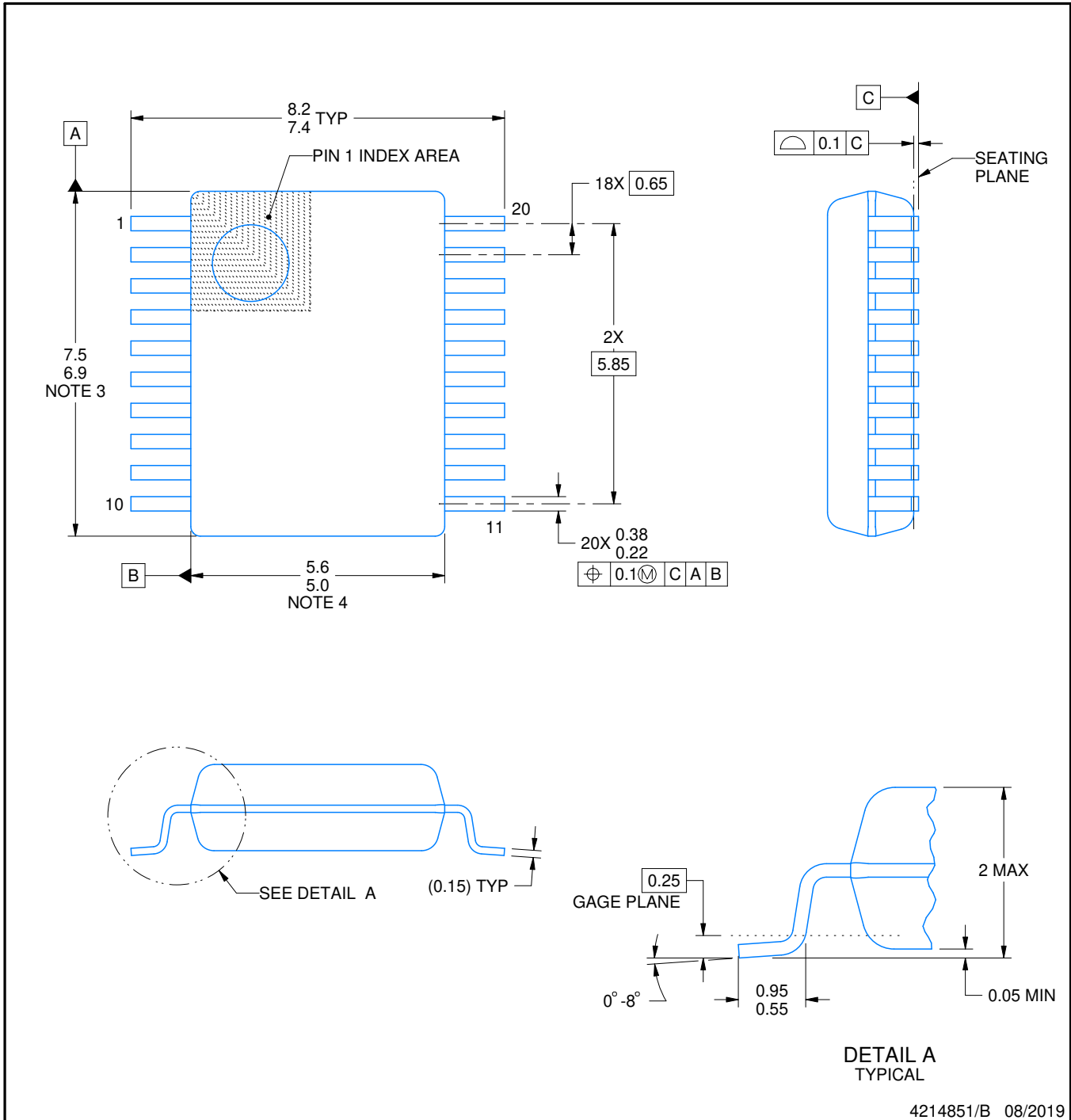E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
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8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

20

18X [0.65]

2X [5.85]

7.5
6.9
NOTE 3

10

11

20X 0.38 / 0.22

⊕ 0.1 Ⓜ C A B

B

5.6
5.0
NOTE 4

C

⌒ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95
0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4214851/B   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
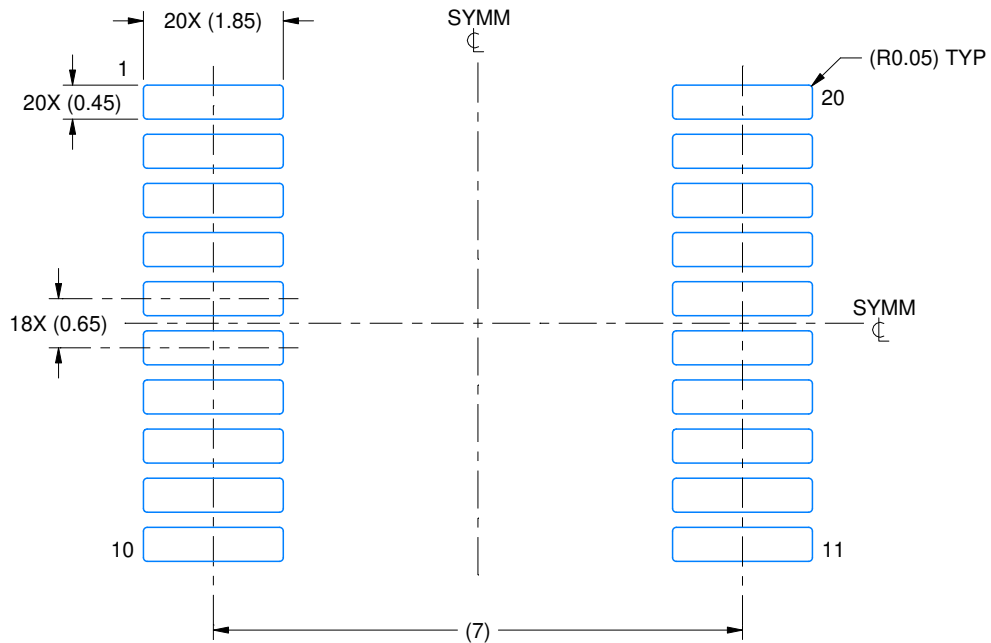5. Reference JEDEC registration MO-150.

DB0020A

20X (1.85)
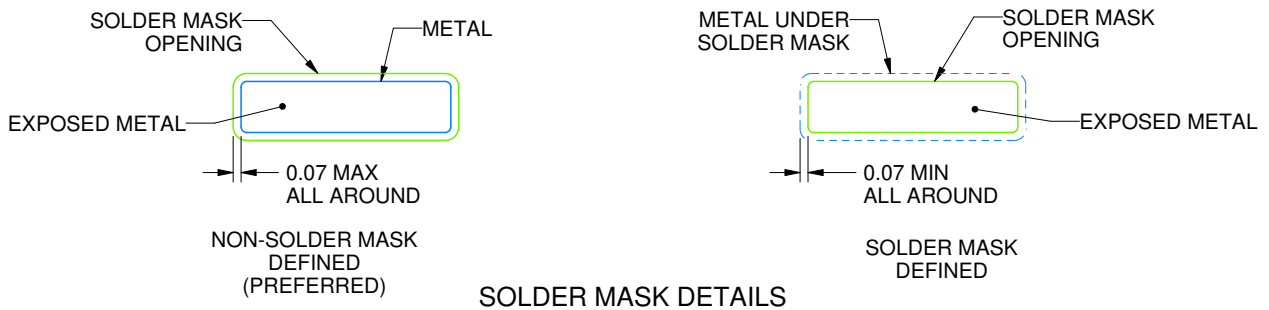
1

20X (0.45)

(R0.05) TYP

20

SYMM

18X (0.65)

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

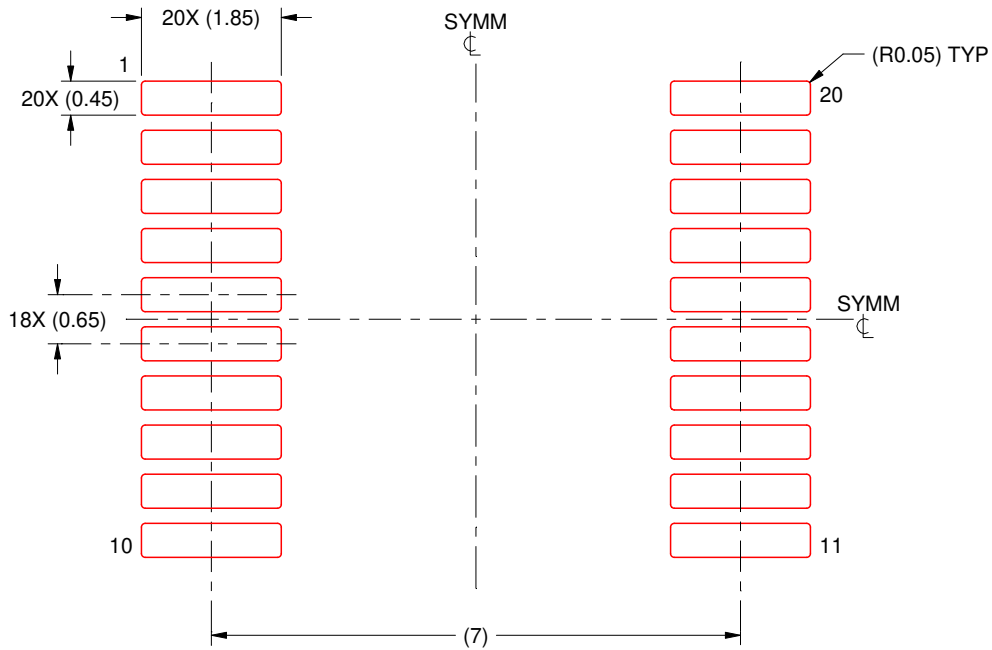**SOLDER MASK DETAILS**

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DB0020A

SSOP - 2 mm max height

20X (1.85)

1

20X (0.45)

SYMM

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
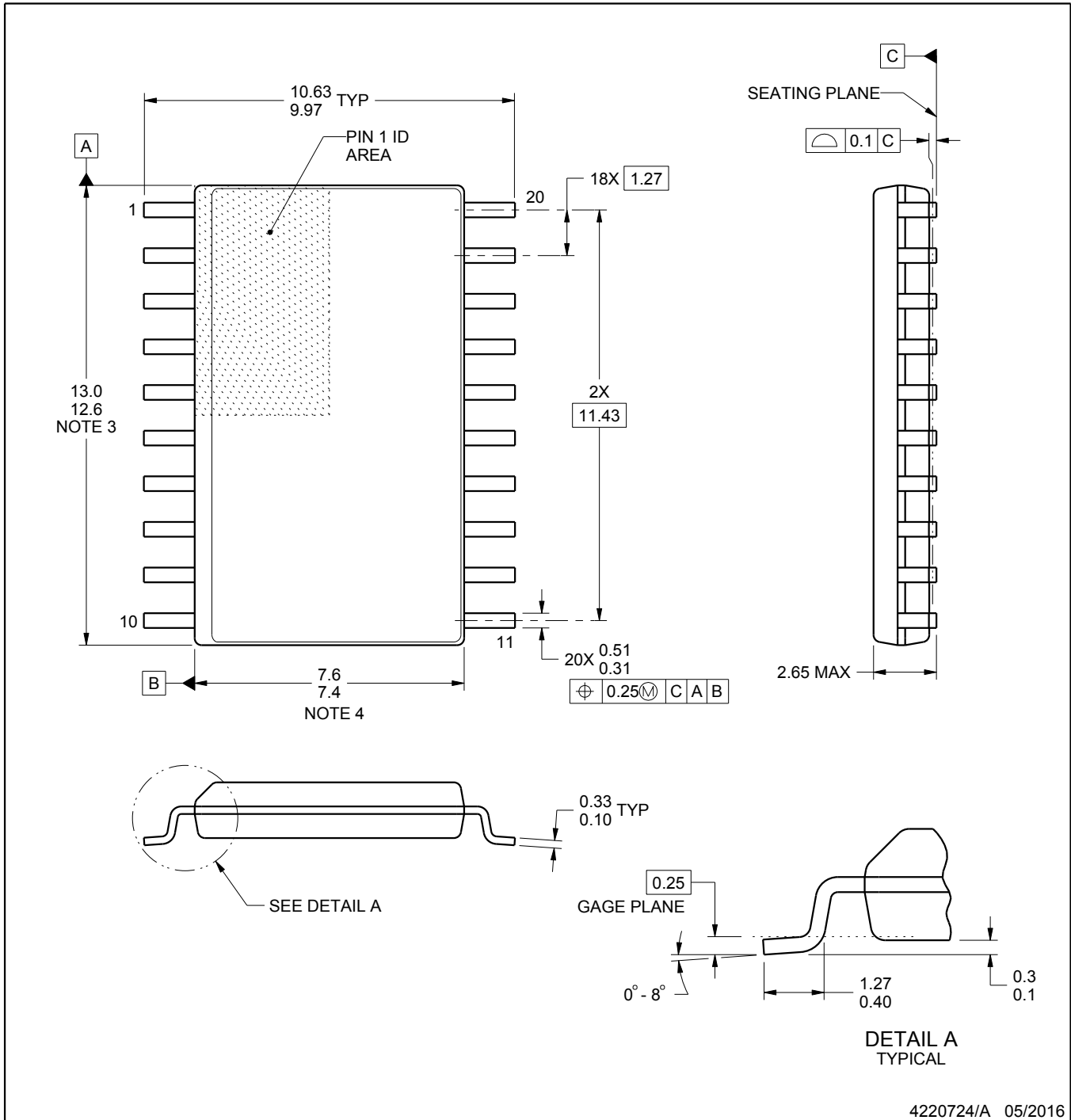   C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

20

18X 1.27

2X 11.43

13.0 / 12.6 NOTE 3

10

11

B

7.6 / 7.4
NOTE 4

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25
GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

TEXAS INSTRUMENTS
www.ti.com

20X (2)

SYMM

1

20X (0.6)

20

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
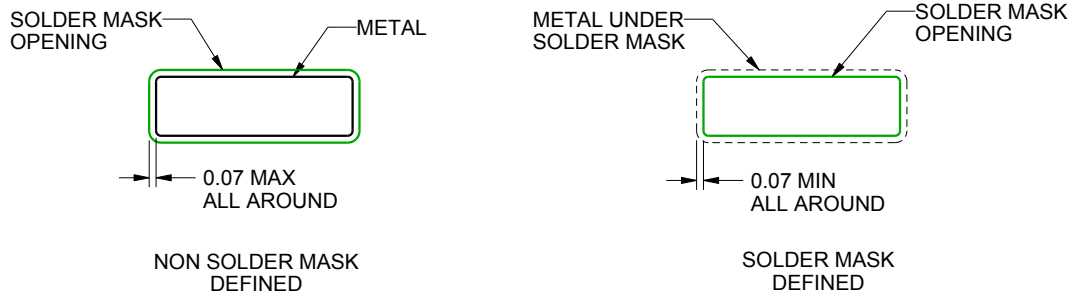
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

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7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

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