19-6025; Rev 0; 9/11

EVALUATION KIT AVAILABLE

MAX3711

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

General Description

The MAX3711 limiting amplifier and laser driver provides a highly integrated, low-cost, high-performance PMD solution.

The low-jitter laser diode driver provides transmit average power control (APC) of laser bias current as well as an integrated modulation current control loop (extinction ratio control, or ERC). The ERC eliminates the need for temperature lookup tables (LUTs) controlling the modulation current.

The low-noise limiting amplifier maximizes optical sensitivity and has adjustable SD/LOS threshold plus programmable output levels. The differential CML output stage features a slew-rate adjustment for 1.25Gbps operation. Integrated bias current monitor and Tx power monitor enable a low-cost implementation of modules with digital diagnostics.

A novel auto-calibration mode enables low-cost fiber optic module production. An integrated 3-wire digital interface controls the laser driver and limiting amplifier functions, and enables communication with a low-cost controller.

The MAX3711 is offered in a small, 4mm x 4mm, 24-pin TQFN package with exposed pad, and operates over the -40°C to +95°C temperature range.

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- **Simplifies Module Manufacturing**
  - **Enables Single-Temperature Module Testing**
  - **Production Laser Auto-Calibration Mode**
- **Improved Performance**
  - **Integrated APC Loop (Operates Up to 3.125Gbps)**
  - **Integrated ERC Loop (Operates Up to 2.7Gbps)**
  - **1.3mV_{P-P} Receiver Sensitivity**
- **Flexibility**
  - **LVDS, LVPECL, and CML Compatible High-Speed I/Os**
  - **Programmable I/O Polarity**
  - **3-Wire Digital Interface**
- **Safety and Reliability**
  - **Integrated Safety Features with FAULT Mask Register**
  - **Supports SFP MSA and SFF-8472 Digital Diagnostic**
  - **Selectable Analog Monitor of Laser Power or BIAS Current at BMON Pin**

Applications

OC-3 to OC-48 SFP/SFF Transceivers

Ethernet SFP/SFF Transceivers

CPRI/OBSAI SFP/SFF Transceivers

CWDM SFP Transceivers

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

ABSOLUTE MAXIMUM RATINGS

V_{CCX}, V_{CCTO}, V_{CCD} .... -0.3V to 4.0V
Voltage Range at DISABLE, SDA, SCL, CSEL,
FAULT, LOS, MDREF .... -0.3V to (V_{CC} + 0.3V)
Voltage Range at RIN+, RIN- .... (V_{CC} - 1.7V) to (V_{CC} + 0.3V)
Voltage Range at ROUT+, ROUT- .... (V_{CC} - 2V) to (V_{CC} + 0.3V)
Voltage Range at TIN+, TIN- .... -0.3V to (V_{CC} + 0.3V)
Voltage Range at TOUT .... 0.3V to V_{CCTO}
Voltage Range at IOUT .... (V_{CCTO} - 1.8V) to (V_{CCTO} + 1.2V)
Current Range into FAULT, LOS,
MDIN, SDA .... -1mA to +5mA
Current out of ROUT+, ROUT- 40mA
Current into TOUT 180mA
Current into IOUT 120mA
Voltage Range at BMON .... -0.3V to V_{CC}
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8mW/°C above +70°C) 2222mW
Storage Temperature Range .... -55°C to +150°C
Die Attach Temperature .... +400°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = 3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING CONDITIONS						
Power Supply Voltage	V_{CC}		2.97	3.3	3.63	V
POWER SUPPLY						
Power-Supply Current	I_{CC}	Includes Rx CML output current, excludes Tx I_{BIAS} = 20mA, I_{MOD} = 40mA		75	110	mA
POWER-ON RESET						
V_{CC} for Enable High		V_{CCX} connected to V_{CCD}		2.55	2.75	V
V_{CC} for Enable Low		V_{CCX} connected to V_{CCD}	2.3	2.45		V
Rx INPUT SPECIFICATION						
Differential Input Resistance	R_{IN}		75	100	125	Ω
Input Sensitivity	V_{INMIN}	2^{23} - 1 PRBS, 2.5Gbps, TX_EN = 0 (Note 2)		1.3	2	mV_{P-P}
Input Overload	V_{INMAX}	(Note 2)	1.2			V_{P-P}
Differential Input Return Loss	S_{DD11}	Device powered on, f ≤ 2GHz		19		dB
		Device powered on, f ≤ 5GHz		12		dB
Common-Mode Input Return Loss	S_{CC11}	Device powered on, 1GHz ≤ f ≤ 2GHz		11		dB
		Device powered on, 2GHz ≤ f ≤ 5GHz		14		dB
Rx OUTPUT SPECIFICATION						
Differential Output Resistance	$R_{OUTDIFF}$		75	100	125	Ω
Differential Output Return Loss	S_{DD22}	Device powered on, f ≤ 2GHz		19		dB
		Device powered on, 2GHz ≤ f ≤ 5GHz		15		dB
Common-Mode Output Return Loss	S_{CC22}	Device powered on, f ≤ 2GHz		14		dB
		Device powered on, 2GHz ≤ f ≤ 5GHz		10		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = 3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CML Differential Output Voltage		$4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 10d	600	800	1000	mV_{P-P}
CML Differential Output Voltage		$4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 0		410		mV_{P-P}
CML Differential Output Voltage When Disabled		Output AC-coupled, V_{INMAX} at input, SET_CML[3:0] = 10d (Note 2)			5	mV_{P-P}
Data Output Transition Time (20% to 80%) (Note 2)		$4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SLEW_RATE = 1		85	115	ps
Data Output Transition Time (20% to 80%) (Note 2)		$4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SLEW_RATE = 0		140	200	ps
LOS Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ - 10kΩ to V_{CC}	V_{CC} - 0.1			V
LOS Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ - 10kΩ to V_{CC}	0		0.4	V
Rx TRANSFER CHARACTERISTICS						
Deterministic Jitter (Notes 2, 3)	DJ	2.5Gbps, $4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 10d		7	15	ps_{P-P}
Deterministic Jitter (Notes 2, 3)	DJ	1.25Gbps, $4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 10d		10	20	ps_{P-P}
Deterministic Jitter (Notes 2, 3)	DJ	125Mbps, $4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 10d, K28.5 pattern		21		ps_{P-P}
Random Jitter	RJ	Input = $4mV_{P-P}$ at 2.5Gbps, 1111 0000 pattern, SET_CML[3:0] = 10d (Notes 2, 4)		3.5	5	ps_{RMS}
Low-Frequency Cutoff (Simulated Value)		I/O coupling capacitors = 1µF		10		kHz
Small-Signal Bandwidth (Simulated Value)		SLEW_RATE = 1		2.0		GHz
LOS SPECIFICATIONS (Notes 2, 5)						
LOS Hysteresis		$10log(V_{DEASSERT}/V_{ASSERT})$	1.25	2.2		dB
LOS Assert/Deassert Time		(Note 6)	2.3		30	µs
LOS Assert Sensitivity Range		LOS_RANGE = 0	4.6		36	mV_{P-P}
LOS Assert Sensitivity Range		LOS_RANGE = 1	14		115	mV_{P-P}
LOS Assert/Deassert Level (Low Range, LOS_RANGE = 0)		LOS assert, SET_LOS = 5	3	3.8	4.6	mV_{P-P}
LOS Assert/Deassert Level (Low Range, LOS_RANGE = 0)		LOS assert, SET_LOS = 31	18	23	28	mV_{P-P}
LOS Assert/Deassert Level (Low Range, LOS_RANGE = 0)		LOS assert, SET_LOS = 63	36	47	56	mV_{P-P}
LOS Assert/Deassert Level (Low Range, LOS_RANGE = 0)		LOS deassert, SET_LOS = 5	5	6.5	8	mV_{P-P}
LOS Assert/Deassert Level (Low Range, LOS_RANGE = 0)		LOS deassert, SET_LOS = 31	32	39	46	mV_{P-P}
LOS Assert/Deassert Level (Low Range, LOS_RANGE = 0)		LOS deassert, SET_LOS = 63	64	80	95	mV_{P-P}

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = 3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOS Assert/Deassert Level (High Range, LOS_RANGE = 1)		LOS assert	SET_LOS = 5	9	11.5	14	mV_{P-P}
			SET_LOS = 31	55	68	80	
			SET_LOS = 63	115	138	160	
		LOS deassert	SET_LOS = 5	15	19	23	
			SET_LOS = 31	97	117	136	
			SET_LOS = 63	197	238	278	
Tx INPUT SPECIFICATIONS							
Differential Input Resistance					13		kΩ
Internal Common-Mode Bias Voltage		For AC-coupled operation			1.3		V
Differential Input Voltage		DC-coupled, 100Ω, differential resistors, Figure 1 and Figure 3		0.2		1.6	V_{P-P}
Common-Mode Input Voltage Range		DC-coupled, Figure 1 and Figure 3		1.125		V_{CC} - V_{IN}/2.5	V
DISABLE Input Current		DISABLE = V_{CC}				10	µA
		DISABLE = GND			33	60.5	
DISABLE Input High Voltage	V_{IH}			1.8		V_{CC}	V
DISABLE Input Low Voltage	V_{IL}			0		0.8	V
DISABLE Input Hysteresis	V_{HYST}				80		mV
DISABLE Input Impedance	R_{PULL}	Pullup resistor		60	100	138	kΩ
Tx OUTPUT SPECIFICATIONS							
FAULT Output High Voltage	V_{OH}	R_{FAULT} is 4.7kΩ - 10kΩ to V_{CC}		V_{CC} - 0.1			V
FAULT Output Low Voltage	V_{OL}	R_{FAULT} is 4.7kΩ - 10kΩ to V_{CC}		0		0.4	V
LASER MODULATOR							
Maximum Modulation-On Current				85			mA
Minimum Modulation-On Current						5	mA
Modulation Current DAC Stability		10mA ≤ I_{MOD} ≤ 85mA (Notes 2, 7)			1	4	%
Modulation Current Rise/Fall Time (Note 2)		20% to 80%, 10mA ≤ I_{MOD} ≤ 85mA, R_{LOAD} = 12Ω, TRF[1:0] = 11b			65	120	ps
		20% to 80%, 10mA ≤ I_{MOD} ≤ 85mA, R_{LOAD} = 12Ω, TRF[1:0] = 00b			72		
Compliance Voltage at TOUT	V_{TOUT}	Instantaneous voltage, 10mA ≤ I_{MOD} ≤ 85mA		0.6		2.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = 3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Deterministic Jitter (Notes 2, 3)	DJ	10mA ≤ I_{MOD} ≤ 85mA, 2.5Gbps		15	40	ps_{P-P}
		10mA ≤ I_{MOD} ≤ 85mA, 1.25Gbps		15		
		10mA ≤ I_{MOD} ≤ 85mA, 125Mbps, K28.5 pattern		20		
Random Jitter (Notes 2, 4)	RJ	10mA ≤ I_{MOD} ≤ 20mA, 1111 0000 pattern		1.2	1.65	ps_{RMS}
		20mA ≤ I_{MOD} ≤ 85mA, 1111 0000 pattern		1	1.45	
BIAS GENERATOR						
Maximum Bias Current		Current into TOUT	70			mA
Minimum Bias Current		Current into TOUT			1	mA
Bias Current DAC Stability		2mA ≤ I_{BIAS} ≤ 70mA, V_{TOUT} = 2V (Notes 2, 7)		1	4	%
Bias Current Monitor Current Gain	I_{BIAS}/ I_{BMON}	External resistor to GND defines voltage gain, I_{BIAS} = 1.5mA	54	58	72	A/A
		External resistor to GND defines voltage gain, I_{BIAS} = 5.7mA	54	65	73	
		External resistor to GND defines voltage gain, I_{BIAS} = 39mA	64	72	80	
		External resistor to GND defines voltage gain, I_{BIAS} = 70mA	64	72	80	
Compliance Voltage Range at BMON	V_{BMON}		0		1.8	V
BMON Current Gain Stability (as Bias Monitor)		2mA ≤ I_{BIAS} ≤ 70mA (Notes 2, 7)		2	5	%
LASER CONTROL SPECIFICATIONS						
APC Loop Stability (1.25Gbps, 2^{23} - 1 PRBS Pattern) (Note 8)		$I_{MDINAVG}$ = 50µA, K_{MD} x SE = 0.005		0.1		10log(dB)
		$I_{MDINAVG}$ = 2mA, K_{MD} x SE = 0.05		0.1		
APC Loop Stability (2.5Gbps, 2^{23} - 1 PRBS Pattern) (Note 8)		$I_{MDINAVG}$ = 50µA, K_{MD} x SE = 0.005		0.1		10log(dB)
		$I_{MDINAVG}$ = 2mA, K_{MD} x SE = 0.05		0.1		
ERC Loop Stability (1.25Gbps, 2^{23} - 1 PRBS Pattern, e_R = 11dB) (Note 8)		$I_{MDINAVG}$ = 50µA, K_{MD} x SE = 0.005		0.5		10log(dB)
		$I_{MDINAVG}$ = 2mA, K_{MD} x SE = 0.05		0.5		
ERC Loop Stability (2.5Gbps, 2^{23} - 1 PRBS Pattern, e_R = 11dB) (Note 8)		$I_{MDINAVG}$ = 50µA, K_{MD} x SE = 0.005		1.3		10log(dB)
		$I_{MDINAVG}$ = 2mA, K_{MD} x SE = 0.05		1.1		
MDIN Bias Voltage	V_{MDIN}			1.2		V
MD Average Current Range	$I_{MDINAVG}$	Average current into MDIN	50		2000	µA
Programmable Extinction Ratio Range	e_R	P1/P0 (DPC closed-loop operation)	5	16	24	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = 3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MD Current Monitor/BMON Activation Time		From the rising edge of the final SCL clock of the 3-wire cycle to 90% of steady state at BMON		100		ns
SAFETY FEATURES						
Fault Threshold Voltage at TOUT	V_{TOUT}	Fault always occurs for V_{TOUT} < 0.35V, fault never occurs for $V_{TOUT} \geq$ 0.55V	0.35		0.55	V
Fault Threshold Voltage at MDIN	V_{MDIN}	Fault always occurs for V_{MDIN} < 0.3V, fault never occurs for $V_{MDIN} \geq$ 0.5V	0.3		0.5	V
Fault Threshold Voltage at IOUT		Fault always occurs for V_{IOUT} < V_{CCTO} - 1.7V, fault never occurs for $V_{IOUT} \geq$ V_{CCTO} - 1.45V, V_{CCTO} = 3.3V	V_{CCTO} - 1.7		V_{CCTO} - 1.45	V
Fault Threshold Voltage at V_{CCTO}		Fault always occurs for V_{CCTO} < 2V; fault never occurs for $V_{CCTO} \geq$ 2.95V	2		2.95	V
Maximum Laser Current in Disable State		Combined total current into TOUT during fault, DISABLE = 1, or TX_EN = 0			100	µA
Tx TIMING SPECIFICATIONS						
DPC Loop Initialization Time	$t_{APCINIT}$	I_{BIAS} = 40mA and I_{MOD} = 60mA, I_{BIAS_INT} = 8mA, time from restart to I_{BIAS} and I_{MOD} at 90% of steady state		3		µs
DISABLE Assert Time	t_{OFF}	Time from rising edge of DISABLE input signal to I_{BIAS} and I_{MOD} at 10% of steady state (Note 2)		30	100	ns
DISABLE Negate Time	t_{ON}	Time from falling edge of DISABLE input signal to I_{BIAS} and I_{MOD} at 90% of steady state (Note 2)		200	300	ns
Fault Assert Time	t_{FAULT}	Time from fault condition to FAULT high, $C_{FAULT} \leq$ 20pF, R_{FAULT} is 4.7kΩ - 10kΩ to V_{CC} (Note 2)		2.5	10	µs
DISABLE to Reset		Minimum required time DISABLE must be held high to reset a fault		100		ns
Rx OUTPUT LEVEL DAC						
Full-Scale Voltage	V_{FS}	SET_CML[3:0] = 15d	820	1000		mV_{P-P}
Resolution		4 bits		40		mV_{P-P}
LOS THRESHOLD DAC						
Full-Scale Voltage		LOS_RANGE = 0		47		mV_{P-P}
		LOS_RANGE = 1		138		
Resolution		LOS_RANGE = 0		0.75		mV_{P-P}
		LOS_RANGE = 1		2.2		
Integral Nonlinearity		SET_LOS[5:0] = 5d to 63d		±0.7		LSB

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = 3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS CURRENT DAC						
Full-Scale Current	I_{FS_BIAS}	I_{BIAS} = (12 + BIASREG[9:0]) x LSB_BIAS	70	78		mA
Resolution	LSB_BIAS	10-bit DAC		75		µA
MODULATION CURRENT DAC						
Full-Scale Current	I_{FS_MOD}	I_{MOD} = (20 + MODREG[8:0]) x LSB_MOD	85	89		mA
Resolution	LSB_MOD	9-bit DAC		167		µA
3-WIRE DIGITAL INTERFACE						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			80		mV
Input Leakage Current	I_{IL}, I_{IH}	Voltage at pin 0V to V_{CC}, internal pullup or pulldown 75kΩ typical			85	µA
Output High Voltage	V_{OH}	External pullup of 4.7kΩ to V_{CC}	V_{CC} - 0.1			V
Output Low Voltage	V_{OL}	External pullup of 4.7kΩ to V_{CC}			0.4	V
3-WIRE DIGITAL INTERFACE TIMING (Figure 6)						
SCL Clock Frequency	f_{SCL}				1	MHz
SCL Pulse-Width High	t_{CH}		0.5			µs
SCL Pulse-Width Low	t_{CL}		0.5			µs
SDA Setup Time	t_{DS}			100		ns
SDA Hold Time	t_{DH}			100		ns
SCL Rise to SDA Propagation Time	t_D			5		ns
CSEL Pulse-Width Low	t_{CSW}		500			ns
CSEL Leading Time Before the First SCL Edge	t_L			500		ns
CSEL Trailing Time After the Last SCL Edge	t_T			500		ns
SDA, SCL External Load	C_B	Total bus capacitance on one line			20	pF

Note 1: Specifications at T_A = -40°C and T_A = +95°C are guaranteed by design and characterization, .
Note 2: Guaranteed by design and characterization, T_A = -40°C to +95°C.
Note 3: The data input transition time is controlled by 4th-order Bessel filter with f_{-3dB} = 0.75 x 1.25GHz and f_{-3dB} = 0.75 x 2.5GHz, respectively. The deterministic jitter caused by this filter is not included in the DJ. A 2^{23} - 1 PRBS equivalent pattern was used.
Note 4: RJ was tested without input filter.
Note 5: For all Rx LOS specifications LOS_LOWBW = 1 for 1.25Gbps operation and LOS_LOWBW = 0 for 2.5Gbps operation.
Note 6: Measurement includes an input AC-coupling capacitor of 0.1µF. The signal at the RIN input is switched between two amplitudes: Signal_ON and Signal_OFF.
1) Receiver operates at sensitivity level plus 1dB power penalty

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = 3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

a) Signal_OFF = 0
Signal_ON = 10log(min_assert_level) + 8dB
b) Signal_ON = 10log(max_deassert_level) + 1dB
Signal_OFF = 0
2) Receiver operates at overload
Signal_OFF = 0
Signal_ON = 1.2V_{P-P}
max_deassert_level and min_assert_level are measured for one SET_LOS setting

Note 7: Stability is defined [$I_{MEASURED}$) - ($I_{REFERENCE}$)]/($I_{REFERENCE}$) over the listed current range temperature and supply variation. Reference current measured at V_{CC} = 3.3V and T_A = +25°C. Measured current is measured at V_{CC} = 3.3V ±5% and T_A = -40°C to +95°C.

Note 8: K_{MD} is the laser diode to monitor diode gain in A/W. SE is the laser's slope efficiency.

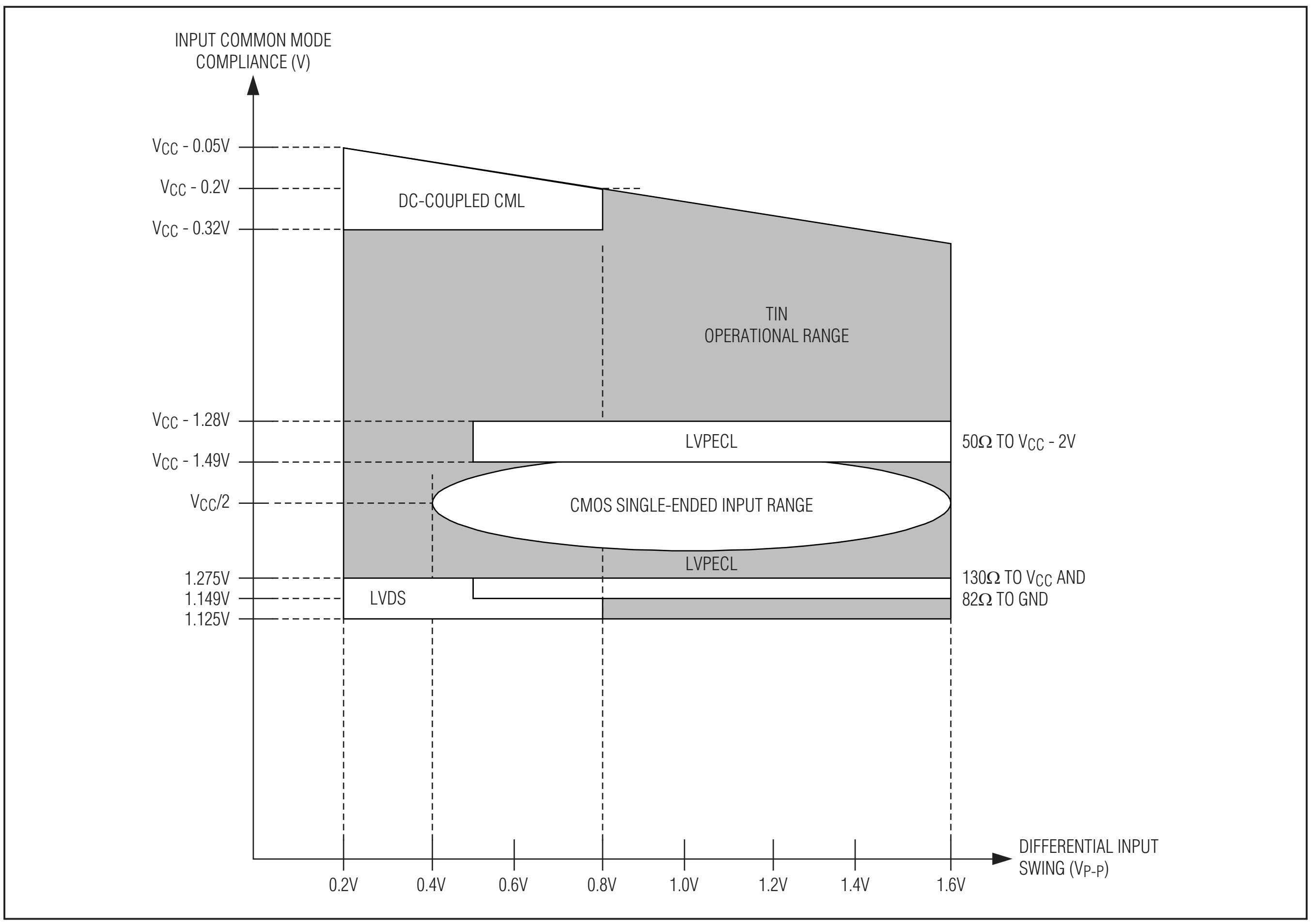


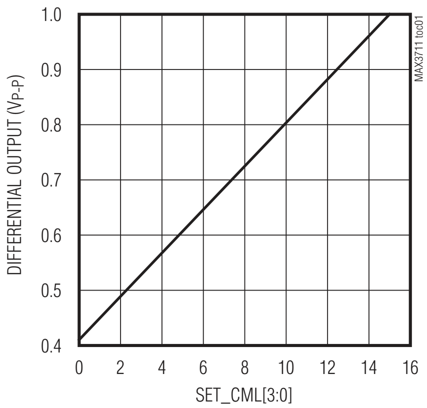
Figure 1. TIN Input Voltage Diagram

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

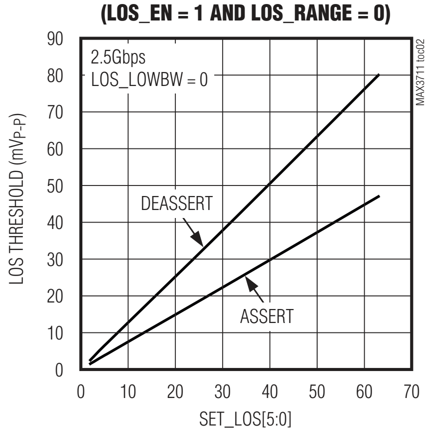
Typical Operating Characteristics

(Typical values are at V_{CC} = 3.3V, T_A = +25°C, data pattern = 2^{23} - 1 PRBS, unless otherwise noted.)

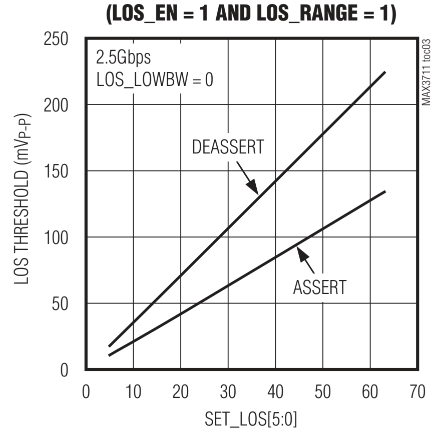
DIFFERENTIAL Rx OUTPUT SWING vs. SET_CML



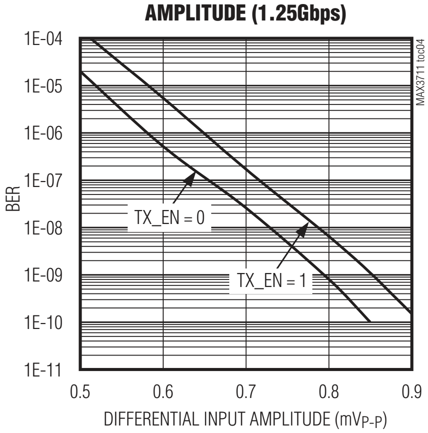
Rx INPUT-BASED LOS THRESHOLD vs. SET_LOS (LOS_EN = 1 AND LOS_RANGE = 0)



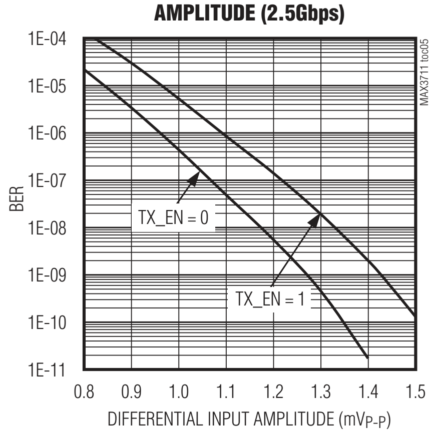
Rx INPUT-BASED LOS THRESHOLD vs. SET_LOS (LOS_EN = 1 AND LOS_RANGE = 1)



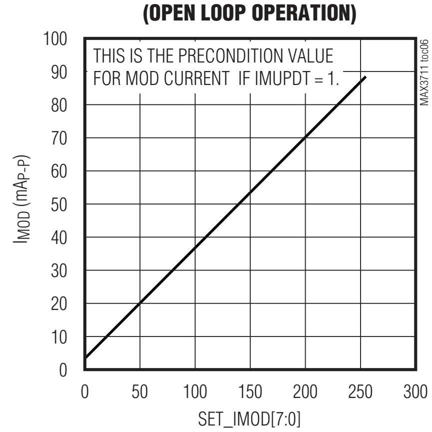
BIT-ERROR RATE vs. DIFFERENTIAL INPUT AMPLITUDE (1.25Gbps)



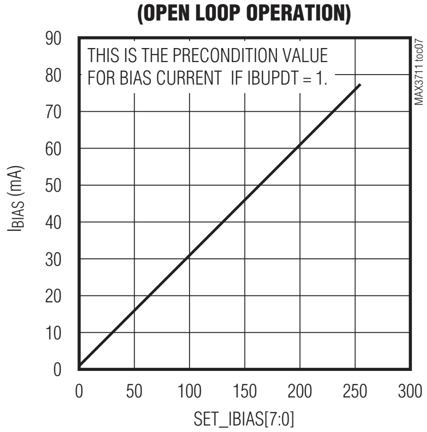
BIT-ERROR RATE vs. DIFFERENTIAL INPUT AMPLITUDE (2.5Gbps)



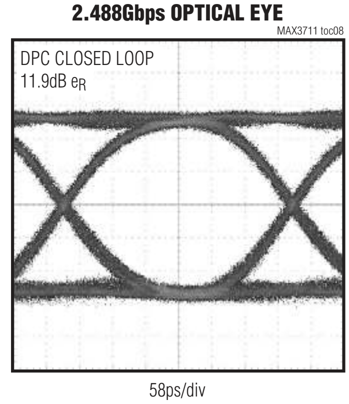
I_{MOD} CURRENT vs. SET_IMOD[7:0] (OPEN LOOP OPERATION)



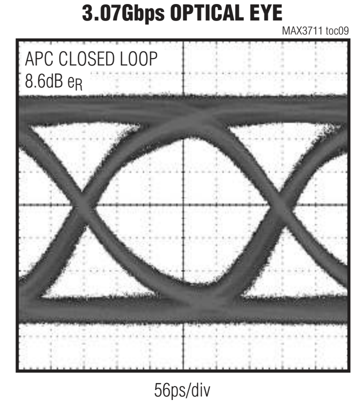
I_{BIAS} CURRENT vs. SET_IBIAS[7:0] (OPEN LOOP OPERATION)



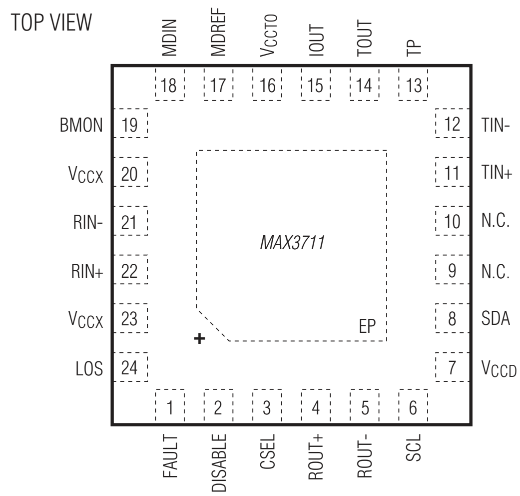
2.488Gbps OPTICAL EYE



3.07Gbps OPTICAL EYE

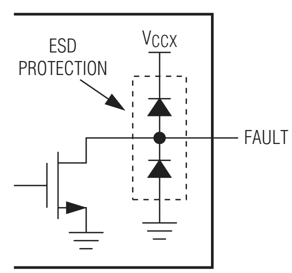
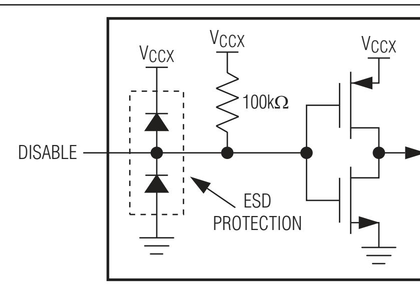


Pin Configuration



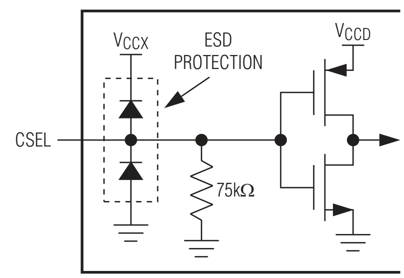
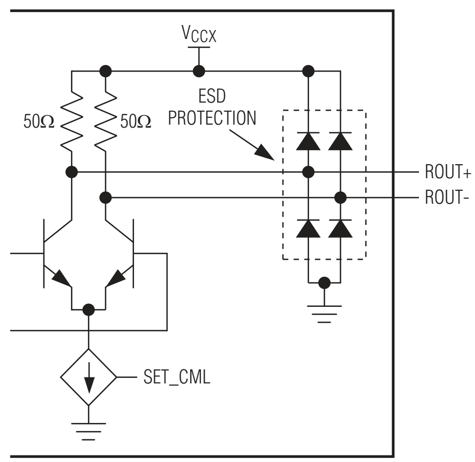
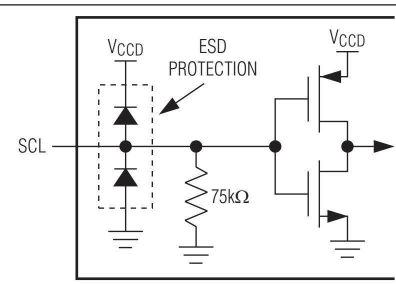
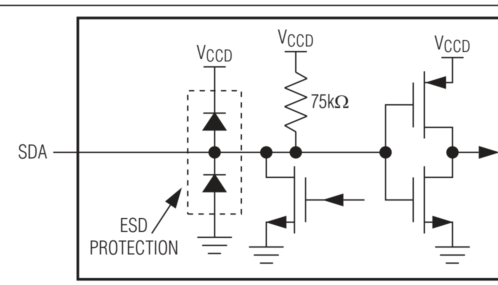
TQFN
(4mm x 4mm)

Pin Description

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
1	FAULT	Transmitter Fault, Open-Drain. Logic-high indicates a fault condition has been detected (FAULT_POL = 1). It remains high even after the fault condition has been removed. A logic-low occurs when the fault condition has been removed and the fault latch has been cleared by toggling the DISABLE signal, or by setting MODECTRL = 68h. FAULT should be pulled up to 3.3V supply through a 4.7kΩ to 10kΩ resistor. Note that pulling up the pin to a supply voltage above V_{CCX} can turn on the ESD protection diode.	
2	DISABLE	Transmitter Disable Input, TTL/CMOS. Set to logic-low for normal operation (DIS_POL = 1). Logic-high or open disables both the modulation current and the bias current. Internally pulled up by a 100kΩ resistor to V_{CCX}.	

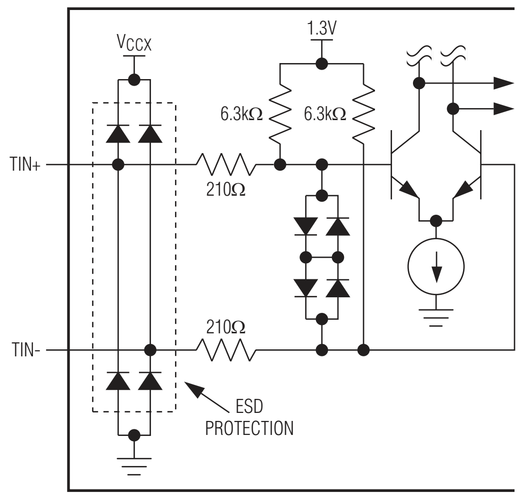
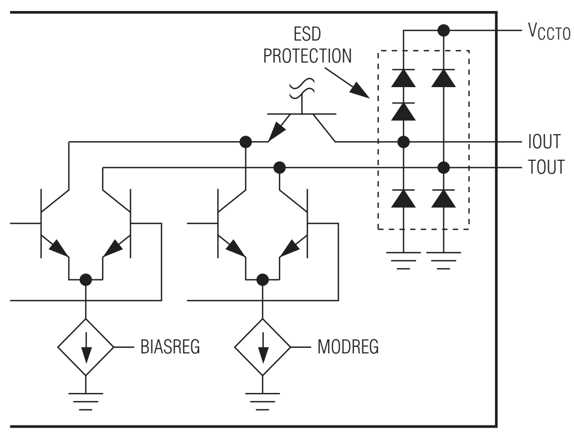
125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Pin Description (continued)

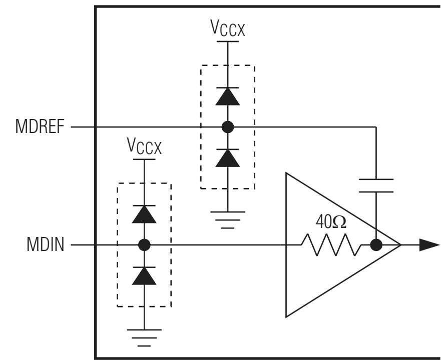
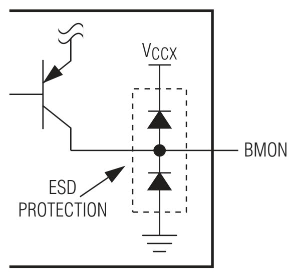
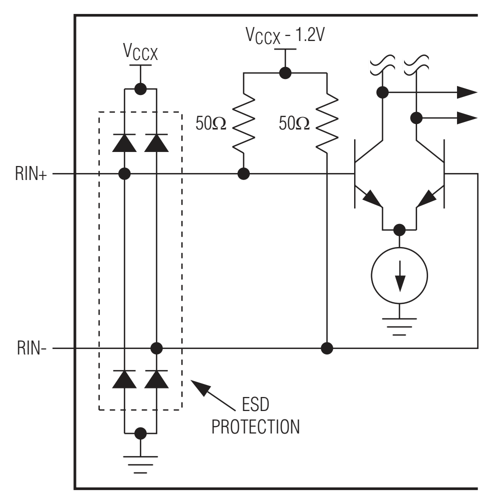
PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
3	CSEL	Chip-Select Input, CMOS. Setting CSEL to logic-high starts a cycle. Setting CSEL to logic-low ends the cycle and resets the control state machine. Internally pulled down by a 75kΩ resistor to ground.	
4, 5	ROUT+, ROUT-	Differential Receiver Data Output, CML. This output has 50Ω terminations to V_{CC}. Polarity is set by the RX_POL bit.	
6	SCL	Serial-Clock Input, CMOS. Internally pulled down by a 75kΩ resistor to ground.	
7	V_{CCD}	Power Supply. Provides supply voltage to the digital block.	—
8	SDA	Serial-Data Bidirectional Input, CMOS. Open-drain output. This pin has a 75kΩ internal pullup, but it requires an external 4.7kΩ to 10kΩ pullup to meet 3-wire timing specifications.	

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

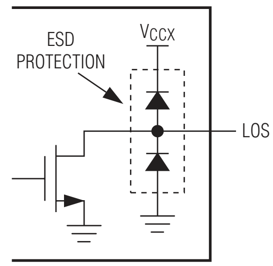
Pin Description (continued)

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
9, 10	N.C.	No Connection. Not internally connected.	—
11, 12	TIN+/TIN-	Differential Transmitter Data Input. This differential 13kΩ input is compatible with LVDS, PECL, and CML input levels. The polarity is set by the TX_POL bit.	
13	TP	Test Pin. Leave pin unconnected.	—
14	TOUT	Noninverting Laser Diode Modulation and Bias Current Output. Connect to the cathode of the laser diode. A differential 1 at TIN± results in current flow at the laser.	
15	IOUT	Inverting Laser Diode Modulation and Bias Current Output. Connect to the anode of the laser diode.	
16	V_{CCTO}	Power-Supply Connection. Provides supply voltage to the transmitter output.	—

Pin Description (continued)

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
17	MDREF	Monitor Diode Reference. Connect this to a filtered V_{CCTO}.	
18	MDIN	Monitor Diode Input. Connect this pin to the anode of the monitor diode. MDIN can be left open for open-loop operation. Keep capacitance minimized at this pin.	
19	BMON	Bias Current/Laser Power Monitor Output. Current out of this pin develops a ground-referenced voltage across external resistor(s) that is proportional to the laser bias current or MDIN pin current. The current sourced by this pin is typically 1/72 the laser bias current.	
20, 23	V_{CCX}	Transceiver Power Supply. Provides supply voltage to the receiver and transmitter cores.	—
21, 22	RIN-, RIN+	Differential Receiver Data Input. Contains 100Ω differential termination on-chip. Connect these inputs to the TIA outputs using 1µF coupling capacitors.	

Pin Description (continued)

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
24	LOS	Receiver Loss-of-Signal (LOS) Output, Open Drain. This output goes to a logic-high when the level of the input signal drops below the SET_LOS register threshold. Polarity is set by LOS_POL. All LOS circuitry can be disabled by setting LOS_EN = 0. The LOS output is pulled up to host V_{CC} with a 4.7kΩ to 10kΩ resistor.	
—	EP	Exposed Pad. Ground. This is the only electrical connection to ground on the MAX3711 and must be soldered to circuit board ground for proper thermal and electrical performance (see the *Exposed-Pad Package and Thermal Considerations* section).	—

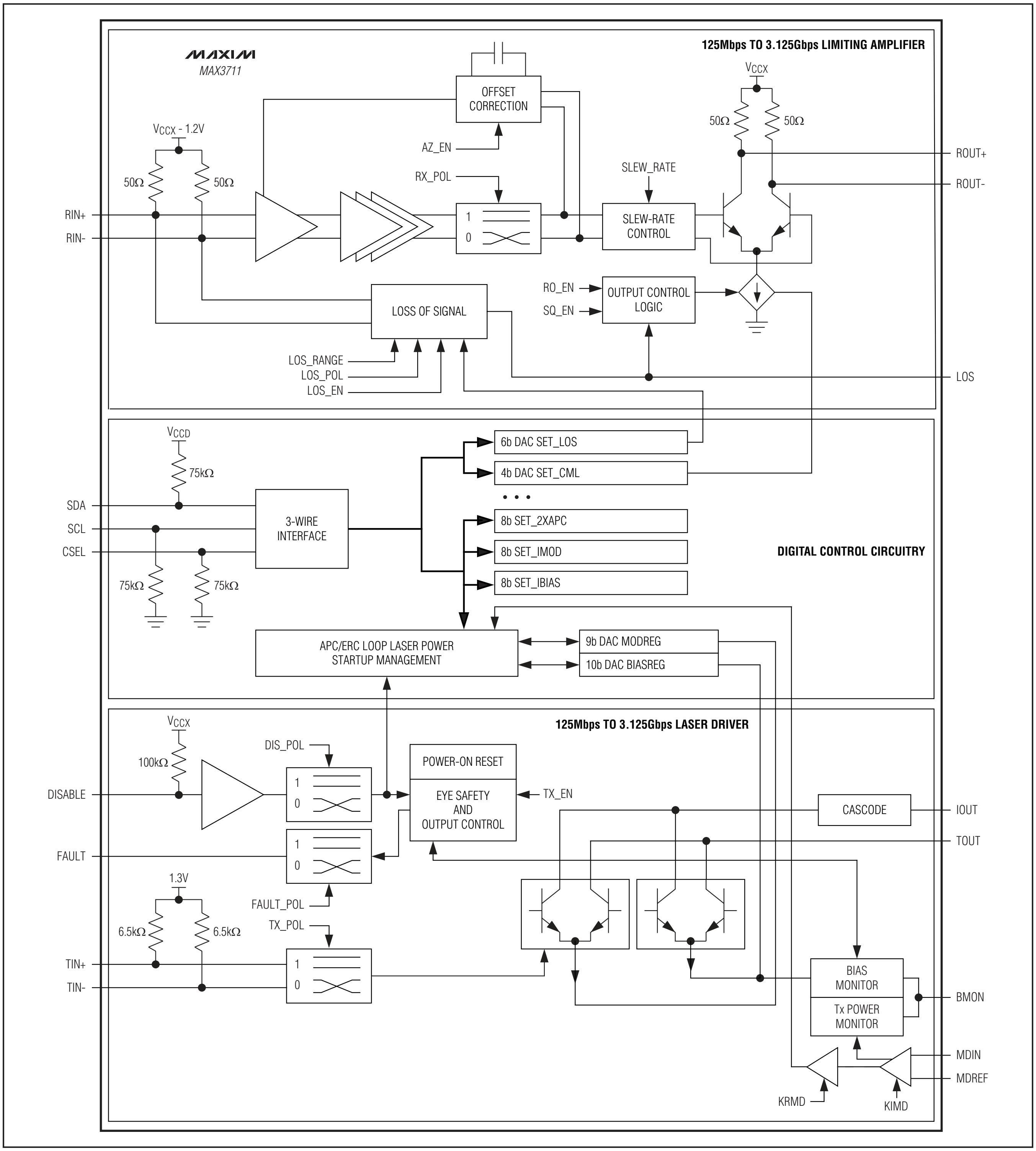


Figure 2. Functional Diagram

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Detailed Description

The MAX3711 combines a high-gain limiting amplifier with a laser driver. The limiting amplifier includes offset cancellation and programmable signal-detect threshold. The laser driver includes average power and extinction ratio control, average or peak laser power measurement capability, overcurrent limiting, bias current/MD current monitor, and fault detection. A 3-wire serial control interface enables an external controller to set all parameters necessary for operation of the limiting amplifier and laser diode driver. The interface enables real-time laser bias and/or modulation current control and provides operation and status readouts.

The features and performance are specifically designed to be compatible with low-cost microcontrollers. The MAX3711 includes all the logic required for laser protection, control loop operation, and monitor diode current measurement.

1.25Mbps to 3.125Gbps Limiting Amplifier Block Description

Limiting Amplifier

The limiting amplifier consists of a multistage amplifier, offset-correction circuit, output buffer, and loss-of-signal/ signal-detect circuitry. Its low noise (1.3mV$_{P-P}$ typical sensitivity) and high gain can provide 0.3dB to 0.5dB of additional sensitivity in typical 2.5Gbps applications. Programmable configuration options (LOS threshold, LOS polarity, CML output with adjustable level, slew rate, and output polarity) enhance layout flexibility and ROSA compatibility.

High-Speed Input Signal Path

The inputs, RIN±, have an internal 100Ω differential termination and should be AC-coupled to the transimpedance amplifier.

Offset Cancellation

The limiting amplifier has approximately 68dB of gain, which makes it very susceptible to both DC offsets and pulse-width distortion in the signal from the transimpedance amplifier. A low-frequency feedback loop provides offset cancellation to compensate for these effects; the nominal small-signal low-frequency cutoff of the offset cancellation loop is 10kHz when 1μF AC-coupling capacitors are used.

Loss-of-Signal Circuitry (LOS)

This block detects amplitude of the incoming signal and compares it against a preset threshold, which is controlled by SET_LOS[5:0]. The programming range of the LOS assert level is 3.8mV$_{P-P}$ to 138mV$_{P-P}$.

Changing the LOS threshold during operation (i.e., without executing a reset) does not cause a glitch or incorrect LOS output. The detector has 2dB of hysteresis to control chatter at the LOS output. The LOS output polarity is controlled by the LOS_POL bit. The entire LOS circuit block can be disabled by setting LOS_EN = 0.

Output Drivers

The CML data outputs, ROUT±, are terminated with 50Ω to V_{CCX}. The differential output level can be programmed through the SET_CML[3:0] register between 410mV$_{P-P}$ and 1000mV$_{P-P}$, and the output polarity can be inverted. Serial commands can also be used to manually disable the output (to its common-mode voltage, i.e., near zero differential voltage DC), or cause the limiting amp to automatically disable the output under an LOS condition (squelch through the SQ_EN bit). The output slew rate can be optimized for either 2.5Gbps or low data-rate operation by setting the SLEW_RATE bit.

1.25Mbps to 3.125Gbps Laser Driver Block Description

The laser driver consists of TIN± differential high-speed input buffers, TIN± polarity switch buffers, DISABLE TTL/CMOS input buffer, combined laser modulator and bias generator, monitor diode current input buffer with calibration features, analog bias current monitor, analog transmit power monitor, APC and ERC loop circuitry, eye-safety monitoring, and FAULT output buffer.

Differential High-Speed Input Buffers

The high-speed laser driver data inputs, TIN±, are compatible with LVDS, LVPECL, and CML outputs. TIN± should be DC-coupled with external differential termination of 100Ω placed close to the input pins. The TIN± inputs can also be DC-coupled to an LVDS output using 100Ω differential termination. The polarity of TIN± can be inverted by the TX_POL bit.

Laser Modulator and Bias Generator

The laser modulator provides DC coupled current into the cathode of the laser diode at the TOUT pin. The modulation current amplitude is set by MODREG[8:0].

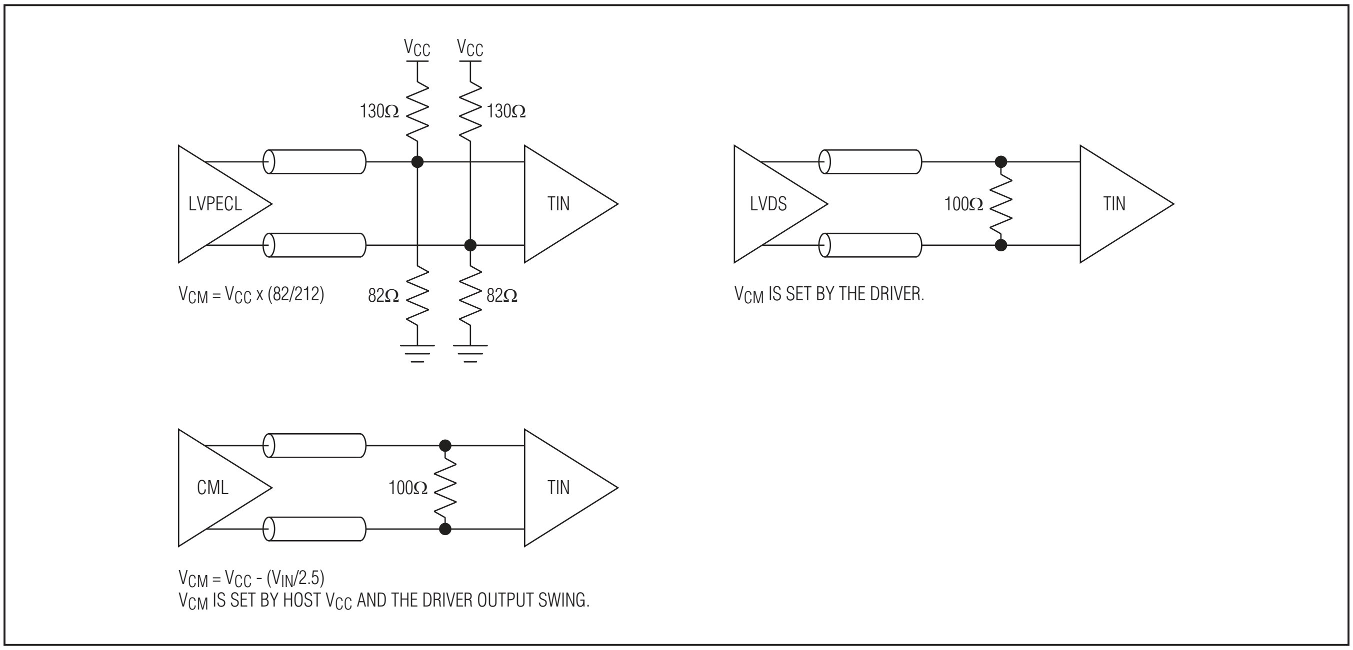


Figure 3. Interfacing to the MAX3711 TIN± Inputs

The modulation current DAC guarantees modulation amplitudes up to 85mA.

The amplitude of the laser bias current is controlled by BIASREG[9:0]. The laser bias current DAC guarantees values up to 70mA.

Note that TOUT and IOUT are not differential in the general sense; TOUT must be connected to the laser diode cathode and the cascoded IOUT pin must be connected to the laser diode anode.

Monitor Diode Current Input Buffer

The input stage covers a large input signal range by having adjustable gain settings. The KIMD[1:0] bits set the current gain. This is followed by an adjustable transimpedance amplifier (TIA). The TIA gain settings are programmed by the KRMD[2:0] bits. The input has high bandwidth, allowing the MAX3711 to monitor not only average laser power, but also extinction ratio.

MDIN current is mirrored at the BMON output and selected by setting MDMON_EN = 1 and MON_SEL = 1. In this mode, the current sourced by BMON is scaled by K_{IMD}, where the value K_{IMD} is set by the KIMD[1:0] bits. The high bandwidth of the MDIN–BMON path enables tuning of the laser-to-monitor diode external components to minimize crosstalk and to optimize filtering on the MDIN signal.

Average Power and Extinction Ratio Control Circuitry

The MAX3711 includes full closed-loop control of laser average power and extinction ratio. Figure 4 shows the dual power control, or DPC, loop. Operation is as follows:

The monitor diode (MD) is connected to the MDIN pin, and the MD current is amplified by a gain set by the KIMD[1:0] and KRMD[2:0] bits.

The output of the MDIN input buffer is sent through a programmable filter, controlled by the CPRG[4:0], MDLBW[1:0], and MDRNG bits.

The filter output is fed to a 10MS/s analog-to-digital converter (ADC), where the peak values of both the high current and the low current (proportional to the high power and low power of the laser) are determined and converted to 16-bit digital words, MD0REGH[7:0] and MD0REGL[7:0], and MD1REGH[7:0] and MD1REGL[7:0]. The values are MD0[15:8] = MD0REGH[7:0], MD0[7:0] = MD0REGL[7:0], MD1[15:8] = MD1REGH[7:0], MD1[7:0] = MD1REGL[7:0]. The number of averages used to generate MD1[15:0] and MD0[15:0] is determined by MDAVG_CNT.

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

To monitor average transmitter power, use the following equation:

$$P_{AVG} = 0.00292 \times \frac{\frac{MD0[15:0]}{8} + MD1[15:0]}{512 \times KIMD \times KRMD \times K_{MD}}$$

where K_{MD} is the laser diode to monitor diode gain in A/W.

For example, if K_{MD} = 0.1, KIMD[1:0] = 00 (gain = 1), KRMD[2:0] = 000 (gain = 2800Ω), MD0[15:0] = 35750d, and MD1[15:0] = 44680d, the calculated P_{AVG} = 1mW.

Returning to the main forward path of the DPC, MD1[15:0] and MD0[15:0] are used to compute the average power and extinction ratio at the MDIN input in the "COMPUTATION" block (Figure 4). These values are compared with the target values of average power (SET_2XAPC[7:0]) and extinction ratio (ERSET[3:0] bits). If the error magnitude is greater than the value set by THRSHLD, then the output registers BIASREG[9:0] and MODREG[8:0] are updated with the error value. The update value is limited by the BIASINC[3:0] and MODINC[3:0] registers.

The IBIASMAX[7:0] and IMODMAX[7:0] values are used to limit BIASREG[9:2] and MODREG[8:1]. Note only the upper 8 bits of the output current registers are compared.

The "CONTROL" block (Figure 4) controls the updating and startup behavior of the entire DPC.

The bits APC_EN and DPC_EN control the operating mode of the DPC:

Full DPC Mode. DPC_EN = 1, APC_EN = X: BIASREG[9:0] and MODREG[8:0] are controlled based on the SET_2XAPC[7:0] register and ERSET[3:0] targets.

APC Only Mode. DPC_EN = 0, APC_EN = 1: The BIASREG[9:0] register is controlled based on the SET_2XAPC[7:0] target and MODREG[8:0] is controlled directly through SET_IMOD[7:0]. MODINC[4:0] is used to adjust the lower bits of MODREG[8:0] using two's complement to increase or decrease its value.

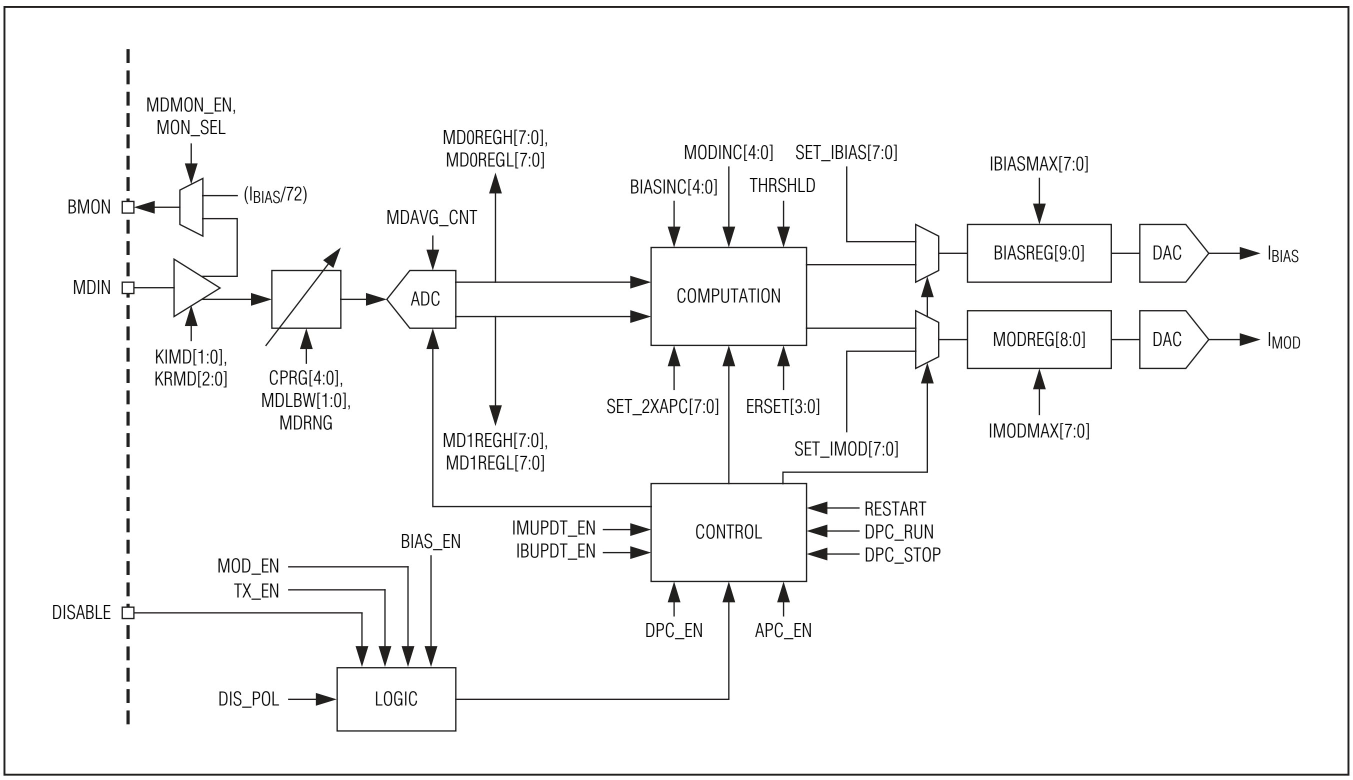


Figure 4. DPC Loop Diagram

Open Loop Mode. DPC_EN = 0, APC_EN = 0: The BIASREG[9:2] register is controlled directly by SET_IBIAS[7:0] and MODREG[8:1] is controlled directly by SET_IMOD[7:0]. Registers BIASINC[4:0] and MODINC[4:0] are used to adjust the lower bits of BIASREG[9:0] and MODREG[8:0] using two's complement.

The DPC acquisition mode is controlled by several bits: RESTART, IBUPDT_EN, IMUPDT_EN, DPC_RUN, and DPC_STOP.

Anytime the DPC FSM is reset (through an unmasked fault or if RESTART is issued), BIASREG[9:2] and MODREG[8:1] are optionally reinitialized to SET_IBIAS[7:0] and SET_IMOD[7:0], respectively. Reinitialization is accomplished by setting bit IBUPDT_EN (for BIASREG[9:0]) or IMUPDT_EN (for MODREG[8:0]) to 1.

The bit RESTART resets the state machine, sets DPC_RUN = 1, and reinitializes BIASREG[9:2] and MODREG[8:1], subject to IBUPDT_EN and IMUPDT_EN, respectively. The state machine then moves to a coarse acquisition mode, a binary-search mode, and finally a steady-state mode where averaging begins. In steady-state mode, the SSMODE status bit is set high and RESTART is reset.

In coarse acquisition mode, the BIASREG[9:0] step size is 2 x BIASINC[3:0] and the MODREG[8:0] step size is 2 x MODINC[3:0]. An update is made every 200ns.

The bit DPC_STOP prevents the DPC from updating the output registers, while DPC_RUN allows the DPC to operate. If a 1 is written to DPC_STOP, DPC_RUN is reset to 0. If a 1 is written to DPC_RUN, DPC_STOP is reset to 0. Writing a 0 to either bit has no affect. If the state machine is not in steady state, setting DPC_STOP = 1 forces it into steady state. Note that the loop no longer updates BIASREG[9:0] and MODREG[8:0] since DPC_STOP is high.

Power-On Reset (POR)

A power-on-reset circuit provides proper startup sequencing and ensures that the laser is off while the supply voltage is ramping or below a specified threshold (~2.55V). The serial interface can also be used to command a manual reset at any time by setting SOFTRESET = 1, which is identical to a power-on reset. When using SOFTRESET, the MAX3711 transmitter must be disabled, either by the DISABLE pin or by setting TX_EN = 0. Either power-on or soft reset requires approximately 50µs to complete. The recommended POR procedure is as follows:

- POR sets all registers to their defaults.
- Controller initiates 3-wire communication after POR with MAX3711 by repeatedly reading out the LVFLAG (V_{CCTO} flag) bit until the 1-to-0 transition occurs (V_{CCTO} is needed for the Tx output and DPC only).
- Controller writes/initializes all registers (see the DPC startup procedure).

BMON Functions

The BMON pin can be selected to either provide a monitor of the laser bias current or the MDIN pin current. It sources 1/72 of the laser bias current when the MON_SEL bit is 0 (default). A resistor to ground sets the full-scale voltage range and can be monitored by an external ADC. When BMON is set to replicate the MDIN current (MON_SEL = 1 and MDMON_EN = 1), the pin sources a KIMD[1:0]-scaled MD current.

Eye Safety Circuitry

The eye safety circuitry consists of fault detection, faults, and fault masking. Certain pins of the device are monitored for conditions that indicate non-standard operation (Figure 5).

A fault disables the transmitter's bias and modulation current DACs and the Tx circuitry remains in a fault state until cleared by toggling DISABLE, cycling power, or writing 68h to MODECTRL[7:0]. Faults are maskable, meaning that by setting the mask bits high, specific faults do not cause the device to become disabled. Faults are indicated by the TXINLOS, FMD, FIOUT, LVFLAG, and FTOUT bits. Note that a fault at MDIN (indicated by FMD) can be masked, but still causes the DPC to stop operation, regardless of the mask. In this condition, the DPC must be started to resume operation (set DPC_RUN = 1 or RESTART = 1).

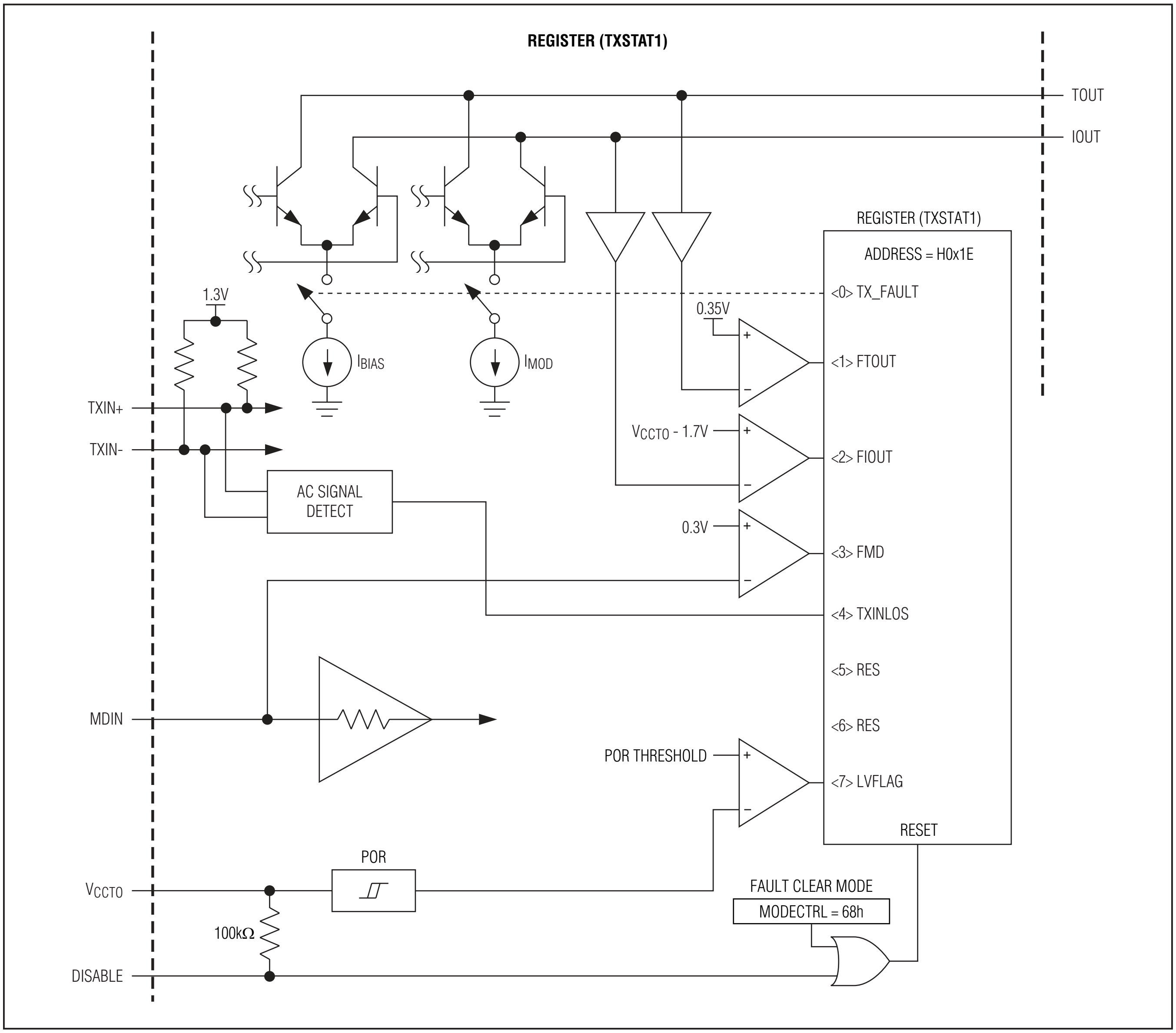


Figure 5. Eye Safety Circuitry

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Table 1. Circuit Response to Single-Point Faults

PIN	NAME	SHORT TO V_{CC}	SHORT TO GND	OPEN
1	FAULT	No effect, but open-drain nMOS output life can be stressed (Note 1)	No effect (Note 1)	No effect (Note 1)
2	DISABLE	Tx output is off if DIS_POL = 1 (default) No effect if DIS_POL = 0	No effect if DIS_POL = 1 (default) Tx output is off if DIS_POL = 0 (Note 1)	Tx output is off if DIS_POL = 1 (default) No effect if DIS_POL = 0
3	CSEL	No effect (Note 1)	No effect (Note 1)	No effect (Note 1)
4	ROUT+	No effect (Note 1)	No effect (Note 1)	No effect (Note 1)
5	ROUT-	No effect (Note 1)	No effect (Note 1)	No effect (Note 1)
6	SCL	No effect (Note 1)	No effect (Note 1)	No effect (Note 1)
7	V_{CCD}	No effect	POR on	POR on
8	SDA	No effect, but open-drain nMOS output life can be stressed (Note 1)	No effect (Note 1)	No effect (Note 1)
9	N.C.	No effect	No effect	No effect
10	N.C.	No effect	No effect	No effect
11	TIN+	TXINLOS flag asserted	TXINLOS flag is asserted	No effect depending on TIN- amplitude
12	TIN-	TXINLOS flag asserted	TXINLOS flag is asserted	No effect depending on TIN+ amplitude
13	TP	No effect	No effect	No effect
14	TOUT	Laser diode is off	FAULT asserted, laser power exceeds programmed value	FAULT asserted
15	IOUT	No effect	FAULT asserted	FAULT asserted
16	V_{CCTO}	No effect	LVFLAG flag asserted, laser diode is off	LVFLAG asserted, laser diode is off
17	MDREF	No effect	No effect	No effect
18	MDIN	Output current limited by IBIASMAX[7:0] and IMODMAX[7:0]	FMD flag asserted	Output current limited by IBIASMAX[7:0] and IMODMAX[7:0]
19	BMON	No effect	No effect (Note 1)	No effect
20	V_{CCX}	No effect	Board supply collapsed, POR on (Note 2)	No effect (Note 3)—Redundant path
21	RIN-	No effect	No effect	No effect
22	RIN+	No effect	No effect	No effect
23	V_{CCX}	No effect	Board supply collapsed, POR on (Note 2)	No effect (Note 3)—Redundant path
24	LOS	No effect, but open-drain nMOS output life can be stressed	No effect	No effect
—	EP	POR on, I/O device life can be stressed (Note 2)	No effect	POR on

Note 1: Normal—Does not affect laser power.
Note 2: Supply-shorted current is assumed to be primarily on the circuit board (outside this device) and the main supply is collapsed by the short.
Note 3: Normal in functionality, but performance could be affected.
Warning: Shorted to V_{CC} or shorted to ground on some pins can violate the *Absolute Maximum Ratings*.

3-Wire Interface

The MAX3711 implements a proprietary 3-wire digital interface, and an external controller generates the clock. The 3-wire interface consists of an SDA bidirectional data line, an SCL clock signal input, and a CSEL chip-select input (active high). The external master initiates a data transfer by asserting the CSEL pin. Then it generates a clock signal after the CSEL pin has been set to a logic-high. All data transfers are most significant bit (MSB) first.

Protocol

Each nonblock operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). The bus master generates 16 clock cycles to SCL. All operations transfer 8 bits to the MAX3711; the RWN bit determines if the cycle is read or write. See Table 2.

Write Mode (RWN = 0)

The master generates 16 clock cycles at SCL in total. It outputs a total of 16 bits (MSB first) to the SDA line at the falling edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 6 shows the 3-wire interface timing.

Read Mode (RWN = 1)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 8 bits (MSB first) to the SDA line at the falling edge of the clock. The SDA line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 6 shows the 3-wire interface timing.

Table 2. Digital Communication Word Structure

BIT	NAME	DESCRIPTION
15:9	Address	7-Bit Internal Register Address
8	RWN	0: Write; 1: Read
7:0	Data	8-Bit Read or Write Data

Block Write Mode (RWN = 0)

The master initiates the block write mode by writing H0x12 into the MODECTRL[7:0] register. The block write mode starts by stretching the CSEL interval beyond the 16 clock cycles, and it is exited automatically when the master has written into any register other than MODECTRL[7:0] and CSEL has been set to 0. The two different modes of operation are described below:

BLOCK WRITE MODE 1 (STARTS AT ADDRESS H0x01)	
Master sets CSEL to 1	
ADDR H0x00 + RWN = 0	Data H0x12
Data 1 (ADDR H0x01)	Data 2 (ADDR H0x02)
Data 3 (ADDR H0x03)	Data 4 (ADDR H0x04)
. . .	
Data 19 (ADDR H0x13)	Master sets CSEL to 0
BLOCK WRITE MODE 2 (STARTS AT ANY ADDRESS)	
Master sets CSEL to 1	
ADDR H0x00 + RWN = 0	Data H0x12
Master sets CSEL to 0	Master sets CSEL to 1
ADDR H0xN + RWN = 0	Data 1 (ADDR H0xN)
. . .	
Data i (ADDR H0xN + i - 1)	Master sets CSEL to 0

Block Read Mode (RWN = 1)

The master initiates the block read mode by accessing any register address and setting the RWN bit to 1. The block read mode starts by stretching the CSEL interval beyond the 16 clock cycles, and it is exited automatically when the master has set CSEL to 0.

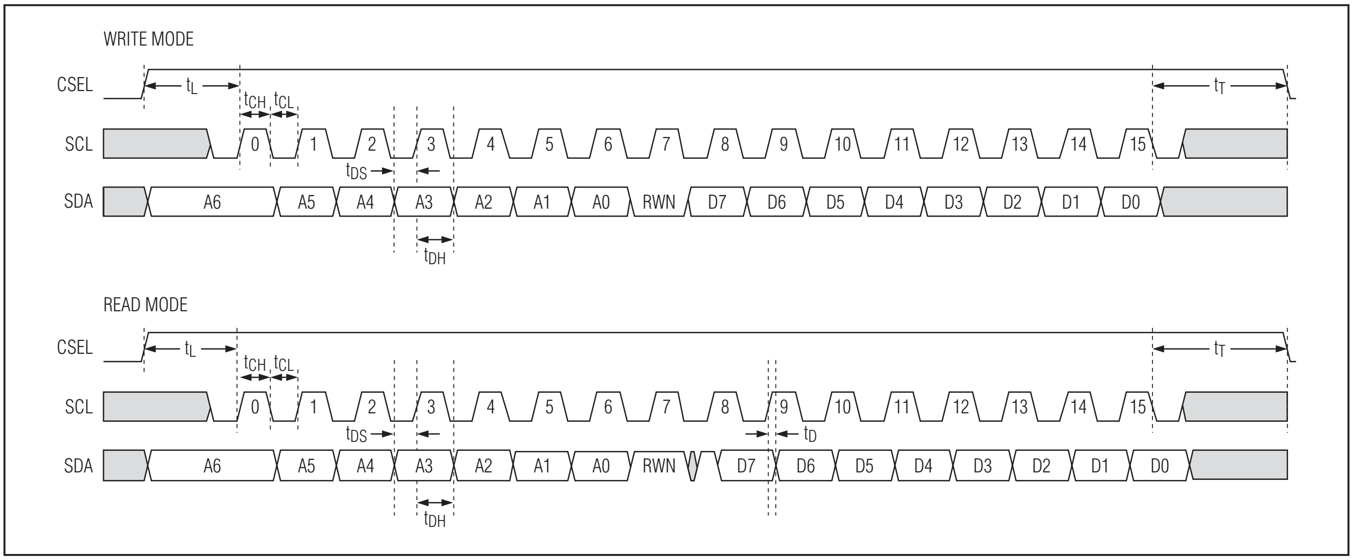


Figure 6. 3-Wire Digital Interface Timing Diagram

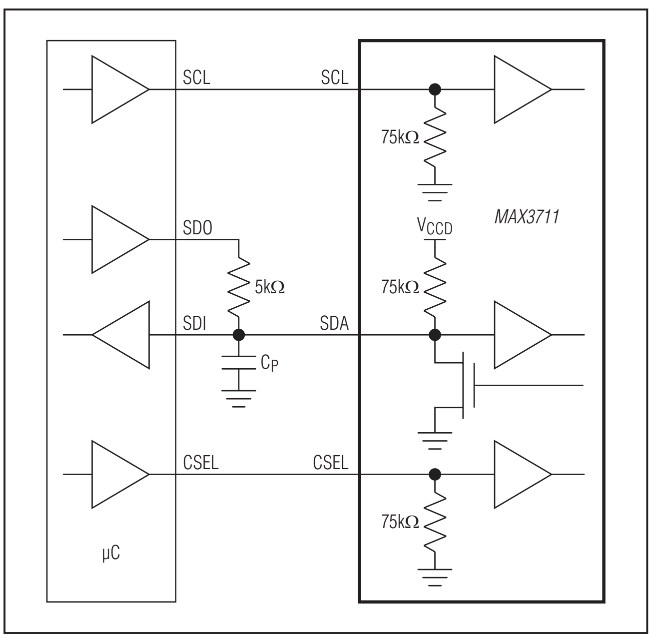


Figure 7. 3-Wire Implementation Recommendation Using a Generic Microcontroller

Mode Control

To speed up the laser control by a factor of two, the MODINC, BIASINC, and APCINC registers can be updated in normal mode. All other registers are read-only in normal mode, which is the default mode.

Setup mode allows the master to write unrestricted data into any register except the status (TXSTAT1, TXSTAT2, DPCSTAT, and RXSTAT) and read-only (BIASREG, MODREG, MD1REGH, MD1REGL, MD0REGH, MD0REGL) registers. To enter the setup mode, H0x12 is written to the MODECTRL register. After the MODECTRL register has been set to H0x12 ,the next operation is unrestricted. The setup mode is automatically exited after the next operation is finished. This sequence must be repeated if further unrestricted settings are necessary.

Fault-clear mode allows the clearing of all faults, and restarts operation of the device. It is activated by writing 68h to the MODECTRL register.

Register Descriptions

Mode Control Register (MODECTRL), Address: H0x00

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MODECTRL [7]	MODECTRL [6]	MODECTRL [5]	MODECTRL [4]	MODECTRL [3]	MODECTRL [2]	MODECTRL [1]	MODECTRL [0]
Read/Write	W	W	W	W	W	W	W	W
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The MODECTRL register sets the device's operational mode.

BIT	NAME	DESCRIPTION
D[7:0]	MODECTRL[7:0]	There are three operational modes for the device: 00h = normal mode (default) 12h = setup mode 68h = fault clear mode

Receiver Control Register 1 (RXCTRL1), Address: H0x01

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	X	X	X	X	LOS_LOWBW	RO_EN
Read/Write	X	X	X	X	X	X	R/W	R/W
POR State	X	X	X	X	X	X	0	1
Reset Upon Read	X	X	X	X	X	X	No	No

The RXCTRL1 register sets the operation of the Rx circuitry.

BIT	NAME	DESCRIPTION
D1	LOS_LOWBW	Sets the bandwidth of the Rx LOS circuitry. 0 = 2.5Gbps (default) 1 = 1.25Gbps
D0	RO_EN	Enables the Rx output stage. 0 = disabled 1 = enabled (default)

Receiver Control Register 2 (RXCTRL2), Address: H0x02

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	LOS_RANGE	LOS_EN	LOS_POL	RX_POL	SQ_EN	RX_EN	SLEW_RATE	AZ_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	1	1	1	0	1	1	1
Reset Upon Read	No	No	No	No	No	No	No	No

The RXCTRL2 register sets the operation of the Rx circuitry.

BIT	NAME	DESCRIPTION
D7	LOS_RANGE	Sets the amplitude range of the Rx LOS circuitry. 0 = 5 to 36mV$_{P-P}$ assert threshold (default) 1 = 14 to 115mV$_{P-P}$
D6	LOS_EN	Enables the LOS circuitry. 0 = disabled 1 = enabled (default)
D5	LOS_POL	Sets the output polarity of the LOS output. 0 = inverse 1 = normal (default)
D4	RX_POL	Sets the output polarity of ROUT. 0 = inverse 1 = normal (default)
D3	SQ_EN	Enables squelch of the output due to input signal below LOS threshold. 0 = disabled (default) 1 = enabled
D2	RX_EN	Enables the entire Rx block circuitry. 0 = disabled 1 = enabled (default)
D1	SLEW_RATE	Sets the slew rate of the Rx output drivers. 0 = slow 1 = normal (default)
D0	AZ_EN	Auto-zero enable. This enables the Rx input offset cancellation loop. 0 = disabled 1 = enabled (default)

CML Output Amplitude Register (SET_CML), Address: H0x03

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	X	X	SET_CML[3]	SET_CML[2]	SET_CML[1]	SET_CML[0]
Read/Write	X	X	X	X	R/W	R/W	R/W	R/W
POR State	X	X	X	X	1	0	1	0
Reset Upon Read	X	X	X	X	No	No	No	No

The SET_CML register sets the amplitude of ROUT.

BIT	NAME	DESCRIPTION
D[3:0]	SET_CML[3:0]	Sets the amplitude of the Rx output driver. Typical values for amplitude: 0000 = 410mV$_{P-P}$ differential output amplitude . . . 1010 = 800mV$_{P-P}$ differential output amplitude (default) . . . 1111 = 1000mV$_{P-P}$ differential output amplitude

LOS Threshold Register (SET_LOS), Address: H0x04

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	SET_LOS[5]	SET_LOS[4]	SET_LOS[3]	SET_LOS[2]	SET_LOS[1]	SET_LOS[0]
Read/Write	X	X	R/W	R/W	R/W	R/W	R/W	R/W
POR State	X	X	0	0	1	1	0	0
Reset Upon Read	X	X	No	No	No	No	No	No

The SET_LOS register adjusts the threshold of the LOS circuitry.

BIT	NAME	DESCRIPTION
D[5:0]	SET_LOS[5:0]	Sets the threshold of the LOS circuitry.

Transmitter Configuration Register (TXCFG), Address: H0x05

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	TRF[1]	TRF[0]	RES	RES	RES	RES	RES	RES
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	1	1	0
Reset Upon Read	No	No	No	No	No	No	No	No

The TXCFG register configures the Tx circuitry.

BIT	NAME	DESCRIPTION
D[7:6]	TRF[1:0]	Adjusts the output rise/fall time of the laser transmitter. 00 = slow (default) 11 = fast
D[5:0]	RES	Reserved 000110 = normal (default)

Transmitter Control Register 1 (TXCTRL1), Address: H0x06

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DPC_STOP	RES	RES	MDRNG	TXSTATMSK [2]	TXSTATMSK [1]	TXSTATMSK [0]	SOFTRES
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	1	1	1	0
Reset Upon Read	No	No	No	No	No	No	No	Yes

The TXCTRL1 register configures the Tx circuitry.

BIT	NAME	DESCRIPTION
D7	DPC_STOP	Halts the APC and DPC loops. The DPC_RUN bit is reset. 0 = no action (default) 1 = halts loops and resets DPC_RUN bit
D[6:5]	RES	Reserved 00 = normal (default)
D4	MDRNG	MD range bit. 0 = fast TOSA MD response (default) 1 = slow TOSA MD response
D3	TXSTATMSK[2]	Sets mask for LVFLAG, FTOUT, and FIOUT. 0 = flags do cause fault condition 1 = flags do not cause fault condition (default)
D2	TXSTATMSK[1]	Sets mask for TXINLOS. 0 = flag do cause fault condition 1 = flag do not cause fault conditon (default)
D1	TXSTATMSK[0]	Sets mask for FMD. 0 = flag do cause fault condition 1 = flag do not cause fault condition (default)
D0	SOFTRES	Resets the contents of the registers to their default values. The device must be disabled (DISABLE pin or TX_EN) to perform a soft reset. 0 = normal (default) 1 = reset

Transmitter Control Register 2 (TXCTRL2), Address: H0x07

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	FAULT_POL	MON_SEL	MDMON_EN	AUX_RSTR	TXLOS_MD	DIS_POL	RES	TX_POL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	1	0	0	0	0	1	1	1
Reset Upon Read	No	No	No	No	No	No	No	No

The TXCTRL2 register configures the Tx circuitry.

BIT	NAME	DESCRIPTION
D7	FAULT_POL	Sets the polarity of the FAULT pin. 0 = inverted 1 = normal (default)
D6	MON_SEL	Sets the BMON pin to output a mirror of BIAS current or MDIN current. 0 = laser bias current mirrored at 1/72 ratio (default) 1 = MDIN current mirrored at BMON
D5	MDMON_EN	Enables BMON output. 0 = laser bias current mirrored (overrides MON_SEL) (default) 1 = MDIN current mirrored at BMON at a ratio of the current gain setting at KIMD
D4	AUX_RSTR	Enables restarting of APC and ERC loops by means of DISABLE pin. 0 = disabled (default) 1 = enabled
D3	TXLOS_MD	Sets output power mode during a loss of signal at TXIN. 0 = output switches to average current value when Tx LOS occurs (default) 1 = output unaffected when Tx LOS occurs
D2	DIS_POL	Sets polarity for DISABLE pin. 0 = inverted 1 = normal (default)
D1	RES	Reserved 1 = normal (default)
D0	TX_POL	Sets Tx data path polarity. 0 = inverted 1 = normal (default)

Transmitter Control Register 3 (TXCTRL3), Address: H0x08

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	RES	DPC_EN	APC_EN	KIMD[1]	KIMD[0]	KRMD[2]	KRMD[1]	KRMD[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The TXCTRL3 register configures the Tx circuitry.

BIT	NAME	DESCRIPTION
D7	RES	Reserved 0 = normal (default)
D6	DPC_EN	Enables dual power control of the laser (closed-loop control of bias and modulation current). 0 = ERC loop disabled (freeze), APC loop mode depends on APC_EN bit (default) 1 = ERC and APC loops enabled
D5	APC_EN	Enables APC loop (closed-loop control of bias current). 0 = disabled (default) 1 = enabled
D[4:3]	KIMD[1:0]	Sets the current gain of the MD input in 3dB steps. 00 = x1 (default) 01 = x0.5 1x = x0.25
D[2:0]	KRMD[2:0]	Sets the transimpedance gain of the MD input in 1.5dB steps. Total MD input stage gain is equal to KIMD gain multiplied by the KRMD gain. 000 = 2800Ω (default) 001 = 1980Ω 010 = 1400Ω 011 = 990Ω 1xx = 700Ω

Transmitter Control Register 4 (TXCTRL4), Address: H0x09

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DINT_EN	ARX_EN	MDAVG_CNT	IBUPDT_EN	IMUPDT_EN	MDLBW[1]	MDLBW[0]	ERSET[3]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	1	1	0	0	0	0	1
Reset Upon Read	No	No	No	No	No	No	No	No

The TXCTRL4 register configures the Tx circuitry.

BIT	NAME	DESCRIPTION
D7	DINT_EN	Routes internal clock signal to the Tx signal path (used in calibration). 0 = normal (default) 1 = routes internal data to the Tx signal path. Note that the data must be running at TIN or the DPC loop freezes.
D6	ARX_EN	Enables auto-ranging for the APC loop. 0 = auto-ranging disabled 1 = auto-ranging enabled; see the *Tracking Error Compensation* section
D5	MDAVG_CNT	Sets the number of MD averages. 0 = DPC updates based on 32 averages in steady state 1 = DPC updates based on 256 averages in steady state (default)
D4	IBUPDT_EN	Sets the way BIASREG[9:0] is written to: APC on: 0 = maintains last value of BIASREG[9:0] in initialization (default) 1 = FAULT/RESTART initializes BIASREG[9:2] with SET_IBIAS[7:0] APC off: 0 = BIASREG can only be changed by writing to BIASINC[4:0] (default) 1 = if IBUPDT_EN is already set to 1 a write to SET_IBIAS[7:0] is passed to BIASREG[9:2]
D3	IMUPDT_EN	Sets the way MODREG[8:0] is written to: ERC on: 0 = maintains last value of MODREG[8:0] in initialization (default) 1 = FAULT/RESTART initializes MODREG[8:1] with SET_IMOD[7:0] ERC off: 0 = MODREG[8:0] can only be changed by writing to MODINC[4:0] (default) 1 = if IMUPDT_EN is already set to 1 a write to SET_IMOD[7:0] is passed to MODREG[8:1]
D[2:1]	MDLBW[1:0]	Controls the bandwidth of the MD input stage. 00 = normal mode (high-frequency signal feedthrough from TOSA is small) (default) 01 = less bandwidth 10 = even less bandwidth 11 = lowest bandwidth (external filter capacitor required on MD input to reduce excessive high-frequency signal feedthrough)
D0	ERSET[3]	Sets range of extinction ratio. 0 = reduced e_R setting (5 to 12) 1 = normal e_R setting (10 to 24) (default)

Transmitter Control Register 5 (TXCTRL5), Address: H0x0A

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	ERSET[2]	ERSET[1]	ERSET[0]	CPRG[4]	CPRG[3]	CPRG[2]	CPRG[1]	CPRG[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The TXCTRL5 register configures the Tx circuitry.

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="2">D[7:5]</td><td rowspan="2">ERSET[2:0]</td><td colspan="2">Sets extinction ratio for closed-loop operation.</td></tr>
<tr><td>If ERSET[3] = 1:
000 = 10 (default)
001 = 12
010 = 14
011 = 16
100 = 18
101 = 20
110 = 22
111 = 24</td><td>If ERSET[3] = 0:
000 = 5
001 = 6
010 = 7
011 = 8
100 = 9
101 = 10
110 = 11
111 = 12</td></tr>
<tr><td>D[4:0]</td><td>CPRG[4:0]</td><td colspan="2">Programs the internal MD current reference filter. Used during calibration to match extinction ratios of the external PRBS data and the slower internal pattern enabled by DINT_EN.</td></tr>
</table>

Maximum Bias Current Register (IBIASMAX), Address: H0x0B

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IBIASMAX [7]	IBIASMAX [6]	IBIASMAX [5]	IBIASMAX [4]	IBIASMAX [3]	IBIASMAX [2]	IBIASMAX [1]	IBIASMAX [0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	1	0	0	1	0
Reset Upon Read	No	No	No	No	No	No	No	No

The IBIASMAX register sets maximum bias current limit.

BIT	NAME	DESCRIPTION
D[7:0]	IBIASMAX[7:0]	Programs the maximum settable bias current (limits the maximum value that can be written to the BIASREG[9:2] register). Note that it only relates to the eight most significant bits of the BIASREG register. 18d = 6.3mA bias current limit (default)

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Maximum Modulation Current Register (IMODMAX), Address: H0x0C

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IMODMAX [7]	IMODMAX [6]	IMODMAX [5]	IMODMAX [4]	IMODMAX [3]	IMODMAX [2]	IMODMAX [1]	IMODMAX [0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	1	1	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The IMODMAX register sets maximum modulation current limit.

BIT	NAME	DESCRIPTION
D[7:0]	IMODMAX[7:0]	Programs the maximum settable modulation current (limits the maximum value that can be written to the MODREG[8:1] register). Note that it only relates to the eight most significant bits of the MODREG register. 48d = 19.5mA modulation current limit (default)

Initial or Open-Loop Bias Value Register (SET_IBIAS), Address: H0x0D

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_ IBIAS[7]	SET_ IBIAS[6]	SET_ IBIAS[5]	SET_ IBIAS[4]	SET_ IBIAS[3]	SET_ IBIAS[2]	SET_ IBIAS[1]	SET_ IBIAS[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	1	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The SET_IBIAS register sets the initial or open-loop bias current.

BIT	NAME	DESCRIPTION
D[7:0]	SET_IBIAS[7:0]	Programs the initial or open-loop bias current. The value in this register is sent to the BIASREG[9:0] register's eight most significant bits. 4d = 2.1mA bias current (default)

Initial or Open-Loop Modulation Value Register (SET_IMOD), Address: H0x0E

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	SET_ IMOD[7]	SET_ IMOD[6]	SET_ IMOD[5]	SET_ IMOD[4]	SET_ IMOD[3]	SET_ IMOD[2]	SET_ IMOD[1]	SET_ IMOD[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	1	0	1	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The SET_IMOD register sets the initial or open-loop modulation current.

BIT	NAME	DESCRIPTION
D[7:0]	SET_IMOD[7:0]	Programs the initial or open-loop bias current. The value in this register is sent to the MODREG[8:0] register's eight most significant bits. 20d = 10mA modulation current (default)

Bias Increment Register (BIASINC), Address: H0x0F

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	X	X	X	BIASINC[4]	BIASINC[3]	BIASINC[2]	BIASINC[1]	BIASINC[0]
Read/Write	X	X	X	R/W	R/W	R/W	R/W	R/W
POR State	X	X	X	0	0	0	0	0
Reset Upon Read	X	X	X	No	No	No	No	No

The BIASINC register increments/decrements bias current as described below

BIT	**NAME**	**DESCRIPTION**
D[4:0]	BIASINC[4:0]	APC enabled: BIASINC[3:0] controls the BIAS step (coarse acquisition max step = 2 x BIASINC[3:0]). APC disabled: Laser BIAS current increment/decrement applied to BIASREG[9:0] upon write (two's complement number, the range is +15/-16).

Modulation Increment Register (MODINC), Address: H0x10

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	X	MODINC[4]	MODINC[3]	MODINC[2]	MODINC[1]	MODINC[0]
Read/Write	X	X	X	R/W	R/W	R/W	R/W	R/W
POR State	X	X	X	0	0	0	0	0
Reset Upon Read	X	X	X	No	No	No	No	No

The MODINC[4:0] register increments/decrements modulation current as described below.

BIT	NAME	DESCRIPTION
D[4:0]	MODINC[4:0]	ERC enabled: MODINC[3:0] controls the MOD step (coarse acquisition max step = 2 x MODINC[3:0]). ERC disabled: Laser modulation current increment/decrement applied to MODREG[8:0] upon write (two's complement number, the range is +15/-16).

Average Laser Power-Setting Register (SET_2XAPC), Address: H0x11

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_ 2XAPC[7]	SET_ 2XAPC[6]	SET_ 2XAPC[5]	SET_ 2XAPC[4]	SET_ 2XAPC[3]	SET_ 2XAPC[2]	SET_ 2XAPC[1]	SET_ 2XAPC[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	1	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The SET_2XAPC register sets the average laser power for the APC loop (see the *Design Procedure* section for more information).

BIT	NAME	DESCRIPTION
D[7:0]	SET_2XAPC[7:0]	Average laser power setting x 2. This register must be maintained within the 64 to 255 range for proper operation.

APC Increment Register (APCINC), Address: H0x12

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	X	X	APCINC[3]	APCINC[2]	APCINC[1]	APCINC[0]
Read/Write	X	X	X	X	R/W	R/W	R/W	R/W
POR State	X	X	X	X	0	0	0	0
Reset Upon Read	X	X	X	X	No	No	No	No

The APCINC register increments/decrements the SET_2XAPC register.

BIT	NAME	DESCRIPTION
D[3:0]	APCINC[3:0]	Increments or decrements the SET_2XAPC[7:0] value with the two's complement value from APCINC[3:0] (the range is +7/-8).

Transmitter Control Register 6 (TXCTRL6), Address: H0x13

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	THRSHLD	DPC_RUN	RESTART	SOFT_RSTR [1]	SOFT_RSTR [0]	BIAS_EN	MOD_EN	TX_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	1	0	0	0	1	1	0
Reset Upon Read	No	No	Yes	No	No	No	No	No

The TXCTRL6 register configures the Tx circuitry.

BIT	NAME	DESCRIPTION
D7	THRSHLD	Sets threshold for updating BIASREG[9:0] in APC mode and BIASREG[9:0] and MODREG[8:0] in DPC mode. 0 = 0.125LSB (default) 1 = 0.75LSB
D6	DPC_RUN	Controls the APC and ERC loops. 0 = no action 1 = APC and ERC loops start from prefreeze conditions (subject to IBUPDT_EN and IMUPDT_EN if starting from reset state); resets DPC_STOP bit (default)
D5	RESTART	Forces APC and ERC loops into acquisition mode from reset state. Once the loop is in steady state, the restart bit is reset. 0 = disabled (default) 1 = enabled
D[4:3]	SOFT_RSTR[1:0]	Soft restart for the DPC 00 = fastest acquisition (default) . . . 11 = slowest (least disruptive) acquisition
D2	BIAS_EN	Enables the bias DAC. 0 = bias DAC disabled 1 = bias DAC enabled (default)
D1	MOD_EN	Enables the modulation DAC. 0 = mod DAC disabled 1 = mod DAC enabled (default)
D0	TX_EN	Enables the Tx data path, control loops, and the bias and modulation DACs. 0 = Tx disabled (default) 1 = Tx enabled

Bias DAC Readback Register (BIASREG), Address: H0x16

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	BIASREG [9]	BIASREG [8]	BIASREG [7]	BIASREG [6]	BIASREG [5]	BIASREG [4]	BIASREG [3]	BIASREG [2]
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The BIASREG register is a read-only register for the Tx bias DAC.

BIT	NAME	DESCRIPTION
D[7:0]	BIASREG[9:2]	Bias current DAC readback. The two LSBs for this register are located at address H0x1F.

Modulation DAC Readback Register (MODREG), Address: H0x17

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MODREG [8]	MODREG [7]	MODREG [6]	MODREG [5]	MODREG [4]	MODREG [3]	MODREG [2]	MODREG [1]
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The MODREG register is a read-only register for the Tx modulation DAC.

BIT	NAME	DESCRIPTION
D[7:0]	MODREG[8:1]	Modulation current DAC readback. The LSB for this register is located at address H0x1F.

Monitor Diode Top Peak (Averaged) Register (MD1REGH), Address: H0x18

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MD1REGH [7]	MD1REGH [6]	MD1REGH [5]	MD1REGH [4]	MD1REGH [3]	MD1REGH [2]	MD1REGH [1]	MD1REGH [0]
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The MD1REGH register is a read-only register for MD top peak current.

BIT	NAME	DESCRIPTION
D[7:0]	MD1REGH[7:0]	Stored (averaged) value for monitor-diode current peak corresponding to optical P1. MD1REGH[7:0] is the upper 8 bits of the 16-bit value MD1[15:0].

Monitor Diode Top Peak (Averaged) Register (MD1REGL), Address: H0x19

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MD1REGL [7]	MD1REGL [6]	MD1REGL [5]	MD1REGL [4]	MD1REGL [3]	MD1REGL [2]	MD1REGL [1]	MD1REGL [0]
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The MD1REGL register is a read-only register for MD top peak current.

BIT	NAME	DESCRIPTION
D[7:0]	MD1REGL	Stored (averaged) value for monitor-diode current peak corresponding to optical P1. MD1REGL[7:0] is the lower 8 bits of the 16-bit value MD1[15:0].

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Monitor Diode Bottom Peak (Averaged) Register (MD0REGH), Address: H0x1A

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MD0REGH [7]	MD0REGH [6]	MD0REGH [5]	MD0REGH [4]	MD0REGH [3]	MD0REGH [2]	MD0REGH [1]	MD0REGH [0]
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The MD0REGH register is a read-only register for MD current.

BIT	NAME	DESCRIPTION
D[7:0]	MD0REGH	Stored (averaged) value for monitor-diode current peak corresponding to optical P0. MD0REGH[7:0] is the upper 8 bits of the 16-bit value MD0[15:0].

Monitor Diode Bottom Peak (Averaged) Register (MD0REGL), Address: H0x1B

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MD0REGL [7]	MD0REGL [6]	MD0REGL [5]	MD0REGL [4]	MD0REGL [3]	MD0REGL [2]	MD0REGL [1]	MD0REGL [0]
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

The MD0REGL register is a read-only register for MD current.

BIT	NAME	DESCRIPTION
D[7:0]	MD0REGL	Stored (averaged) value for monitor-diode current peak corresponding to optical P0. MD0REGL[7:0] is the lower 8 bits of the 16-bit value MD0[15:0].

LOS Status Register (RXSTAT), Address: H0x1C

Bit	D7	D6	D5	D4	D3	D2	D1	D0 (STICKY)
Bit Name	X	X	X	X	X	X	X	LOS_STAT
Read/Write	X	X	X	X	X	X	X	R
POR State	X	X	X	X	X	X	X	0
Reset Upon Read	X	X	X	X	X	X	X	Yes*

**Once flagged, these sticky registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.*

The RXSTAT register is a status register for the Rx circuitry.

BIT	NAME	DESCRIPTION
D0	LOS_STAT	Copy of the LOS status.

Dual Power Control Status Register (DPCSTAT), Address: H0x1D

Bit	D7	D6	D5 (STICKY)	D4 (STICKY)	D3 (STICKY)	D2 (STICKY)	D1 (STICKY)	D0 (STICKY)
Bit Name	X	SSMODE	IBIASOVFL	IBIASUDFL	IMODOVFL	IMODUDFL	2XAPC_OVF	2XAPC_UDF
Read/Write	X	R	R	R	R	R	R	R
POR State	X	0	0	0	0	0	0	0
Reset Upon Read	X	No	Yes*	Yes*	Yes*	Yes*	Yes*	Yes*

**Once flagged these sticky registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.*

The DPCSTAT register is a status register for the DPC circuitry.

BIT	NAME	DESCRIPTION
D6	SSMODE	DPC in steady state.
D5	IBIASOVFL	APC/DPC attempting to increase BIASREG[9:2] over IBIASMAX[7:0].
D4	IBIASUDFL	APC/DPC attempting to underflow BIASREG[9:0] register.
D3	IMODOVFL	DPC attempting to increase MODREG[8:1] over IMODMAX[7:0].
D2	IMODUDFL	DPC attempting to underflow MODREG[8:0] register.
D1	2XAPC_OVF	APCINC[3:0] setting attempting to overflow SET_2XAPC[7:0] register.
D0	2XAPC_UDF	APCINC[3:0] or SET_2XAPC[7:0] setting attempting to decrease SET_2XAPC[7:0] below minimum value. If ARX_EN = 0 or {KIMD[1:0], KRMD[2:0]} = {00, 000}, minimum value is 32. If ARX_EN = 1 and {KIMD[1:0], KRMD[2:0]} ≠ {00, 000}, minimum value is 180.

Transmitter Status Register (TXSTAT1), Address: H0x1E

Bit	D7 (STICKY)	D6 (STICKY)	D5 (STICKY)	D4 (STICKY)	D3 (STICKY)	D2 (STICKY)	D1 (STICKY)	D0 (STICKY)
Bit Name	LVFLAG	RES	RES	TXINLOS	FMD	FIOUT	FTOUT	TX_FAULT
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	Yes*	Yes*	Yes*	Yes*	Yes*	Yes*	Yes*	Yes*

**Once flagged, these sticky registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.*

The TXSTAT1 register is a status register for the Tx circuitry.

BIT	NAME	DESCRIPTION
D7	LVFLAG	V_{CCTO} undervoltage detection (fault, maskable).
D[6:5]	RES	Reserved 00 = normal (default)
D4	TXINLOS	Indicates TIN AC signal too low (fault, maskable). When the MAX3711 senses a loss of signal at TIN, the DPC loop freezes. It resumes once a signal is detected again at TIN.
D3	FMD	MDIN shorted to GND. Fault is reported, DPC is stopped, and FAULT output is set high (fault, maskable).
D2	FIOUT	IOUT open or shorted to GND. Fault is reported and FAULT output is set high (fault, maskable).
D1	FTOUT	TOUT open or shorted to GND. Fault is reported and FAULT output is set high (fault, maskable).
D0	TX_FAULT	A copy of FAULT.

Transmitter Status Register (TXSTAT2), Address: H0x1F

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	X	X	X	BIASREG[1]	BIASREG[0]	MODREG[0]
Read/Write	X	X	X	X	X	R	R	R
POR State	X	X	X	X	X	0	0	0
Reset Upon Read	X	X	X	X	X	No	No	No

The TXSTAT2 register is a status register for the Tx circuitry.

BIT	NAME	DESCRIPTION
D[2:1]	BIASREG[1:0]	LSBs of the BIASREG register.
D0	MODREG[0]	LSB of the MODREG register.

Design Procedure

Global Recommendation

It is recommended to write to the MAX3711 either through use of the block write mode or by writing to registers in sequential order to ensure the proper register updating.

Open-Loop Control of Transmitter Average Power and Modulation Amplitude

In this mode, the laser bias and modulation currents are set by means of an external controller. The APC loop can be closed externally by using the BIASINC register to update the bias current DAC value. The laser modulation current can be controlled by means of a lookup table (LUT). If MD0[15:0] and MD1[15:0] are to be used by the controller for Tx power monitoring, or to implement a power-control loop, the MDIN gains—KIMD[1:0] and KRMD[2:0] bits—must be set appropriately so that the values in the MD0REGH[7:0] and MD1REGH[7:0] registers do not hit the minimum and maximum limits of 16 and 256.

To operate with open-loop control of modulation and bias current, the registers need to be set as shown in Table 3.

Table 3. Open-Loop Setup Bits

ADDRESS	BIT(S)	NAME	DESCRIPTION	VALUE
H0x08 TXCTRL3	6	DPC_EN	Dual power control enable	0
	5	APC_EN	Automatic power control enable	0
H0x09 TXCTRL4	4	IBUPDT_EN	Bias current update	1
	3	IMUPDT_EN	Modulation current update	1
Hx013 TXCTRL6	0	TX_EN	Transmitter enable	1

Once the laser is attached and the device is powered up, the IBIASMAX[7:0] and IMODMAX[7:0] registers should be set to limits that prevent damage to the laser. Then the transmitter is enabled by setting TX_EN = 1. The default modulation and bias current is low, and it is likely that no optical power will be detected until these currents are increased.

The bias and modulation current can be adjusted by either writing to the SET_IBIAS[7:0] and SET_IMOD[7:0] registers directly or by writing to the BIASINC[4:0] and MODINC[4:0] registers.

Closed-Loop Control of Transmitter Average Power, Open-Loop Control of Modulation Amplitude

To operate in APC mode, the registers need to be set as shown in Table 4. For APC-only calibration, see Stage 1 of the *Closed-Loop Control of Transmitter Average Power and Extinction Ratio* section.

Table 4. APC Setup Bits

ADDRESS	BIT(S)	NAME	DESCRIPTION	VALUE
H0x08 TXCTRL3	6	DPC_EN	Dual power control enable	0
	5	APC_EN	Average power control enable	1
H0x09 TXCTRL4	4	IBUPDT_EN	Bias current update	1
	3	IMUPDT_EN	Modulation current update	1
H0x13 TXCTRL6	0	TX_EN	Transmitter enable	1

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Closed-Loop Control of Transmitter Average Power and Extinction Ratio

To operate in DPC mode, the registers need to be set as shown in Table 5.

Table 5. DPC Setup Bits

ADDRESS	BIT(S)	NAME	DESCRIPTION	VALUE
H0x08 TXCTRL3	6	DPC_EN	Dual power control enable	1
	5	APC_EN	Average power control enable	1
H0x09 TXCTRL4	4	IBUPDT_EN	Bias current update	1
	3	IMUPDT_EN	Modulation current update	1
H0x13 TXCTRL6	0	TX_EN	Transmitter enable	1

Laser Calibration Procedure

This novel feature enables the customer to speed up the calibration process and reduce the requirement on test equipment. The customer needs to provide the following:

a) Extinction ratio and optical average power targets

b) Optical average power measurement fed back to the testing algorithm

c) 2^{15} - 1 to 2^{31} - 1 PRBS data pattern at data rate of interest

d) Testing algorithm based on SPI read/write

The device automatically sets the laser bias and modulation current to satisfy the e_R and P_{AVG} targets. If transmitter operation at multiple power levels is required, calibration at each power level is recommended to guarantee DPC loop performance.

Calibration Scheme:

Stage 1: Average laser power calibration

1) Set bits as shown in Table 4 for APC operation, or as shown in Table 5 for DPC operation.
2) Provide 2^{15} - 1 to 2^{31} - 1 PRBS data at TIN.
3) Set TXCTRL4 DINT_EN = 1 and TX_POL = 1.
4) If DPC operation, set ERSET[3:0] to target and set CPRG[4:0] to 15.
5) Set IBIASMAX[7:0] and IMODMAX[7:0] to appropriate values according to laser's capability.
6) Set SET_IBIAS[7:0] and SET_IMOD[7:0] to 0.
7) Set MODINC[3:0] and BIASINC[3:0] to nonzero values.
8) Set SET_2XAPC[7:0] to B4h (this allows for ±1.5dB tracking error compensation range using APCINC).
9) Set TXCTRL6[7:0] to 67h.
10) MDIN gain adjustment (repeat loop until average power is equal to or above the P_{AVG} target).
    a) Stop the loop by setting TXCTRL1[7] to 1.
    b) Decrease MDIN stage gain (KIMD x KRMD) 1.5dB by increasing KRMD[2:0] one value, or by decreasing KRMD[2:0] one value and increasing KIMD[1:0] one value.
    c) Restart the loop by setting TXCTRL6[5] to 1.
11) Reduce SET_2XAPC[7:0] until average power measurement reaches the target.
12) For DPC operation, continue to Stage 2.

Stage 2: Extinction ratio calibration

1) Set DPC_STOP to 1.
2) To verify P_{AVG} and e_R, read MD0REGH[7:0] and MD1REGH[7:0] and use the equations below to calculate the apparent P_{AVG} and e_R at MDIN. Averaging is recommended for improved accuracy.

$$2XAPC = P_{AVG\_APPARENT} = \frac{MD0REGH[7:0]}{8} + MD1REGH[7:0]$$

$$IR = \frac{I_{MD1}}{I_{MD0}} = \frac{8 \times MD1REGH[7:0]}{MD0REGH[7:0]}$$

3) If 2XAPC and IR are not sufficiently close to the SET_2XAPC[7:0] and ERSET values, set DPC_RUN = 1 and go to step 2. Otherwise, continue to step 4.
4) Set DINT_EN = 0.
5) Read MD0REGH[7:0] and MD1REGH[7:0].
6) Adjust CPRG[4:0] until MD0REGH[7:0] and MD1REGH[7:0] satisfy the IR equation from step 2.

If a higher IR is desired, increase CPRG[4:0]; likewise, if a lower IR is desired, decrease CPRG[4:0].

7) Set TXCTRL6[7:0] to 67h to restart the loop and observe that MD0REGH[7:0] and MD1REGH[7:0] are at the desired values.

Power Leveling

It is recommended to use KIMD and KRMD to obtain different power level settings. Calibrate the DPC loop at each power level. When switching between power levels this procedure should be followed.

a) Stop loop by setting DPC_STOP = 1.

b) Change gain using KIMD or KRMD.

c) Run DPC by setting DPC_RUN = 1.

Tracking Error Compensation

It is recommended to use the APCINC register in auto-ranging mode for tracking error compensation. When ARX_EN is set to 1, the SET_2XAPC register value is automatically maintained within 180 to 255 by adjusting the KRMD and KIMD registers accordingly. If {KIMD, KRMD} = {00, 000}, the minimum SET_2XAPC value is reduced from 180 to 32.

Applications Information

Laser Safety and IEC 825

Using the device's laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each user must determine the level of fault tolerance required by the application, recognizing that Maxim products are neither designed nor authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application in which the failure of a Maxim product could create a situation where personal injury or death could occur.

Register Summary

ADDR	R/W	REGISTER NAME	BIT	NAME	FUNCTION/DESCRIPTION	DEFAULT STATE	NOTES
H0x00	W	MODECTRL	7:0	MODECTRL [7:0]	0h: normal mode 12h: setup mode 68h: fault clear mode	0	
H0x01	RW	RXCTRL1	1	LOS_LOWBW	Set bandwidth of the LOS circuitry 0 = for 2.5Gbps 1 = for 1.25Gbps to 125Mbps	0	
			0	RO_EN	Enables Rx output stage 0 = disable 1 = enable	1	
H0x02	RW	RXCTRL2	7	LOS_RANGE	0 = 5 to 36mV$_{P-P}$ 1 = 14 to 115mV$_{P-P}$	0	
			6	LOS_EN	0 = disable 1 = enable	1	
			5	LOS_POL	0 = inverse 1 = normal	1	
			4	RX_POL	0 = inverse 1 = normal	1	
			3	SQ_EN	0 = disable 1 = enable	0	
			2	RX_EN	0 = disable complete Rx block, including LOS 1 = enable	1	
			1	SLEW_RATE	0 = slow 1 = nominal	1	
			0	AZ_EN	0 = disable 1 = enable	1	
H0x03	RW	SET_CML	3:0	SET_CML [3:0]	Sets CML output amplitude 0d = 410mV$_{P-P}$ … 10d = 800mV$_{P-P}$ … 15d = 1000mV$_{P-P}$	1010	10d
H0x04	RW	SET_LOS	5:0	SET_LOS [5:0]	Programs the LOS threshold	00 1100	12d
H0x05	RW	TXCFG	7:6	TRF[1:0]	Output tuning 00 = slow output edge speed 11 = fast output edge speed	00	
			5:0	RES	Reserved 000110 = normal	000110	

Register Summary (continued)

ADDR	R/W	REGISTER NAME	BIT	NAME	FUNCTION/DESCRIPTION	DEFAULT STATE	NOTES
H0x06	RW	TXCTRL1	7	DPC_STOP	0 = no action 1 = APC and ERC loops freeze and DPC_RUN bit is reset	0	
			6:5	RES	Reserved 00 = normal	00	
			4	MDRNG	MD range bit 0 = fast TOSA 1 = slow TOSA	0	
			3:1	TXSTATMSK [2:0]	[2] = LVFLAG, FTOUT, FIOUT mask [1] = TXINLOS mask [0] = FMD mask	1 1 1	
			0	SOFTRES	Soft reset	0	
H0x07	RW	TXCTRL2	7	FAULT_POL	Controls FAULT pin polarity 0 = inverted 1 = normal	1	
			6	MON_SEL	0 = Bias current monitor output 1 = MD current monitor output	0	
			5	MDMON_EN	1 = enables MDMON output	0	When low, bias current monitor is automatically selected (overrides MON_SEL)
			4	AUX_RSTR	Enables restarting of APC and ERC loops by means of the DISABLE input 0 = disabled 1 = enabled	0	
			3	TXLOS_MD	TXIN LOS mode 0 = output squelches to average current during Tx LOS 1 = output unaffected during Tx LOS	0	
			2	DIS_POL	0 = inverted 1 = normal	1	
			1	RES	Reserved 1 = normal	1	
			0	TX_POL	0 = inverted 1 = normal	1	

Register Summary (continued)

ADDR	R/W	REGISTER NAME	BIT	NAME	FUNCTION/DESCRIPTION	DEFAULT STATE	NOTES
H0x08	RW	TXCTRL3	7	RES	Reserved 0 = normal	0	
			6	DPC_EN	0 = disabled 1 = enabled	0	
			5	APC_EN	0 = APC loop disabled (freeze) 1 = APC loop enabled	0	
			4:3	KIMD[1:0]	Current gain of MD input stage 00 = x1 01 = x0.5 1X = x0.25	00	
			2:0	KRMD[2:0]	Voltage gain of the MD input stage 000 = 2800Ω 001 = 1980Ω 010 = 1400Ω 011 = 990Ω 1XX = 700Ω	000	

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Register Summary (continued)

ADDR	R/W	REGISTER NAME	BIT	NAME	FUNCTION/DESCRIPTION	DEFAULT STATE	NOTES
H0x09	RW	TXCTRL4	7	DINT_EN	0 = normal TIN routing 1 = routes internal data to Tx signal path	0	Used in calibration
			6	ARX_EN	0 = auto-ranging disabled 1 = auto-ranging enabled	1	
			5	MDAVG_CNT	0 = 32 averages in steady state 1 = 256 averages in steady state	1	
			4	IBUPDT_EN	APC on: 0 = maintains last value of BIASREG[9:0] in initialization (default) 1 = FAULT/RESTART initializes BIASREG[9:2] with SET_IBIAS[7:0] APC off: 0 = BIASREG can only be changed by writing to BIASINC[4:0] (default) 1 = if IBUPDT_EN is already set to 1 a write to SET_IBIAS[7:0] is passed to BIASREG[9:2] (subject to EOB_EN)	0	
			3	IMUPDT_EN	ERC on: 0 = maintains last value of MODREG[8:0] in initialization (default) 1 = FAULT/RESTART initializes MODREG[8:1] with SET_IMOD[7:0] ERC off: 0 = MODREG[8:0] can only be changed by writing to MODINC[4:0] (default) 1 = if IMUPDT_EN is already set to 1 a write to SET_IMOD[7:0] is passed to MODREG[8:1] (subject to EOB_EN)	0	
			2:1	MDLBW[1:0]	Controls the bandwidth of the MD input stage 00 = normal mode (HF signal feedthrough from the TOSA is small) ... 11 = lowest bandwidth (external filter capacitor required on MD input to reduce excessive HF signal feedthrough)	00	
			0	ERSET[3]	0 = reduced e_R setting (5 to 12) 1 = normal e_R setting (10 to 24)	1	

Register Summary (continued)

ADDR	R/W	REGISTER NAME	BIT	NAME	FUNCTION/DESCRIPTION	DEFAULT STATE	NOTES
H0x0A	RW	TXCTRL5	7:5	ERSET[2:0]	Sets extinction ratio. If ERSET[3] = 1 (normal): 000 = 10 001 = 12 010 = 14 011 = 16 100 = 18 101 = 20 110 = 22 111 = 24 If ERSET[3] = 0 (reduced): 000 = 5 001 = 6 010 = 7 011 = 8 100 = 9 101 = 10 110 = 11 111 = 12	000	
			4:0	CPRG[4:0]	Programs the internal MD current reference filter	00000	
H0x0B	RW	IBIASMAX	7:0	IBIASMAX [7:0]	Max BIAS DAC setting allowed	0001 0010	18d
H0x0C	RW	IMODMAX	7:0	IMODMAX [7:0]	Max MOD DAC setting allowed	0011 0000	48d
H0x0D	RW	SET_IBIAS	7:0	SET_IBIAS [7:0]	Open-loop or initial value setting	0000 0100	4d
H0x0E	RW	SET_IMOD	7:0	SET_IMOD [7:0]	Open-loop or initial value setting	0001 0100	20d
H0x0F	RW	BIASINC	4:0	BIASINC [4:0]	APC enabled: Max BIAS step (coarse acquisition max step = 2 x BIASINC[3:0]) APC disabled: laser BIAS current setpoint inc/dec step size upon write	00000	
H0x10	RW	MODINC	4:0	MODINC [4:0]	ERC enabled: Max MOD step (coarse acquisition max step = 2 x MODINC[3:0]) ERC disabled: laser MOD current setpoint inc/dec step size upon write	00000	
H0x11	RW	SET_2XAPC	7:0	SET_2XAPC [7:0]	Average laser power setting x 2	0010 0000	32d
H0x12	RW	APCINC	3:0	APCINC [3:0]	Updates SET_2XAPC[7:0] with two's complement APCINC[3:0]	0000	

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Register Summary (continued)

ADDR	R/W	REGISTER NAME	BIT	NAME	FUNCTION/DESCRIPTION	DEFAULT STATE	NOTES
H0x13	RW	TXCTRL6	7	THRSHLD	Sets threshold for updating BIASREG[9:0] in APC mode and BIASREG[9:0] and MODREG[8:0] in DPC mode 0 = 0.125 LSB 1 = 0.75 LSB	0	
			6	DPC_RUN	Controls the APC and ERC loops 0 = no action 1 = APC and ERC loops restart from last saved prefreeze conditions (subject to IBUPT_EN and IMUPDT_EN) and DPC_STOP bit is reset	1	
			5	RESTART	Forces loop out of steady-state mode and enables the startup state machine 0 = disabled 1 = enabled	0	
			4:3	SOFT_RSTR[1:0]	00 = fastest DPC acquisition . . . 11 = slowest (least disruptive) DPC acquisition	00	
			2	BIAS_EN	0 = bias DAC disabled 1 = bias DAC enabled	1	
			1	MOD_EN	0 = mod DAC disabled 1 = mod DAC enabled	1	
			0	TX_EN	0 = TX path and laser control loops disabled 1 = TX path and laser control loops enabled	0	
H0x16	R	BIASREG	7:0	BIASREG [9:2]	BIAS current DAC input readback	0000 0000	
H0x17	R	MODREG	7:0	MODREG [8:1]	MOD current DAC input readback	0000 0000	
H0x18	R	MD1REGH	7:0	MD1REGH [7:0]	(Averaged) MD current top peak digitized data	0000 0000	
H0x19	R	MD1REGL	7:0	MD1REGL [7:0]	(Averaged) MD current top peak digitized data	0000 0000	
H0x1A	R	MD0REGH	7:0	MD0REGH [7:0]	(Averaged) MD current bottom peak digitized data	0000 0000	
H0x1B	R	MD0REGL	7:0	MD0REGL [7:0]	(Averaged) MD current bottom peak digitized data	0000 0000	
H0x1C	R	RXSTAT	0	LOS_STAT	Copy of the LOS status		sticky

Register Summary (continued)

ADDR	R/W	REGISTER NAME	BIT	NAME	FUNCTION/DESCRIPTION	DEFAULT STATE	NOTES
H0x1D	R	DPCSTAT	6	SSMODE	DPC in steady state		not sticky
			5	IBIASOVFL	BIASREG[9:2] input over max warning		sticky
			4	IBIASUDFL	BIASREG[9:0] input underflow		sticky
			3	IMODOVFL	MODREG[8:1] input over max warning		sticky
			2	IMODUDFL	MODREG[8:0] input underflow		sticky
			1	2XAPC_OVF	SET_2XAPC[7:0] wraparound high		sticky
			0	2XAPC_UDF	SET_2XAPC[7:0] wraparound low		sticky
H0x1E	R	TXSTAT1	7	LVFLAG	V_{CCTO} undervoltage detection		fault, sticky, maskable
			6:5	RES	Reserved		
			4	TXINLOS	Indicates TXIN ac-signal too low		fault, sticky, maskable
			3	FMD	MDIN shorted to GND. Fault is reported and FAULT output is set high.		fault, sticky, maskable; stops DPC regardless of mask
			2	FIOUT	IOUT open or shorted to GND. Fault is reported and FAULT output is set high.		fault, sticky, maskable
			1	FTOUT	TOUT open or shorted to GND. Fault is reported and FAULT output is set high.		fault, sticky, maskable
			0	TX_FAULT	A copy of FAULT		fault, sticky
H0x1F	R	TXSTAT2	2:1	BIASREG[1:0]	LSBs of BIASREG[9:0]		
			0	MODREG[0]	LSB of MODREG[8:0]		

Note: *Sticky bits remain flagged even if the cause of the flag is removed. Reading the bit resets it if the source of the flag has been removed.*

125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Layout Considerations

The high-speed data inputs and outputs are the most critical paths for the device, and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. The following are some suggestions for maximizing the device's performance:

- The data inputs should be wired directly between the connector and IC without stubs.
- The data transmission lines to the laser should be kept as short as possible, and the impedance of the transmission lines must be considered part of the laser matching network.
- Minimize capacitance on the MDIN connection.
- An uninterrupted ground plane should be positioned beneath the high-speed I/Os.
- Ground path vias should be placed close to the IC and the input/output interfaces to allow a return current path to the IC and the laser.
- Maintain 100Ω differential transmission line impedance for the RIN, ROUT, and TIN I/Os.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Refer to the schematic and board layers of the MAX3711 Evaluation Kit data sheet for more information.

Exposed-Pad Package and Thermal Considerations

The exposed pad on the MAX3711 is the only electrical connection to ground and provides a very low-thermal resistance path for heat removal from the IC. The pad is also electrical ground on the device and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Application Note 862: *HFAN-08.1: Thermal Considerations for QFN and Other Exposed-Paddle Packages* for additional information.

Chip Information

PROCESS: SiGe BiPOLAR

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3711ETG+	-40°C to +85°C	24 TQFN-EP*

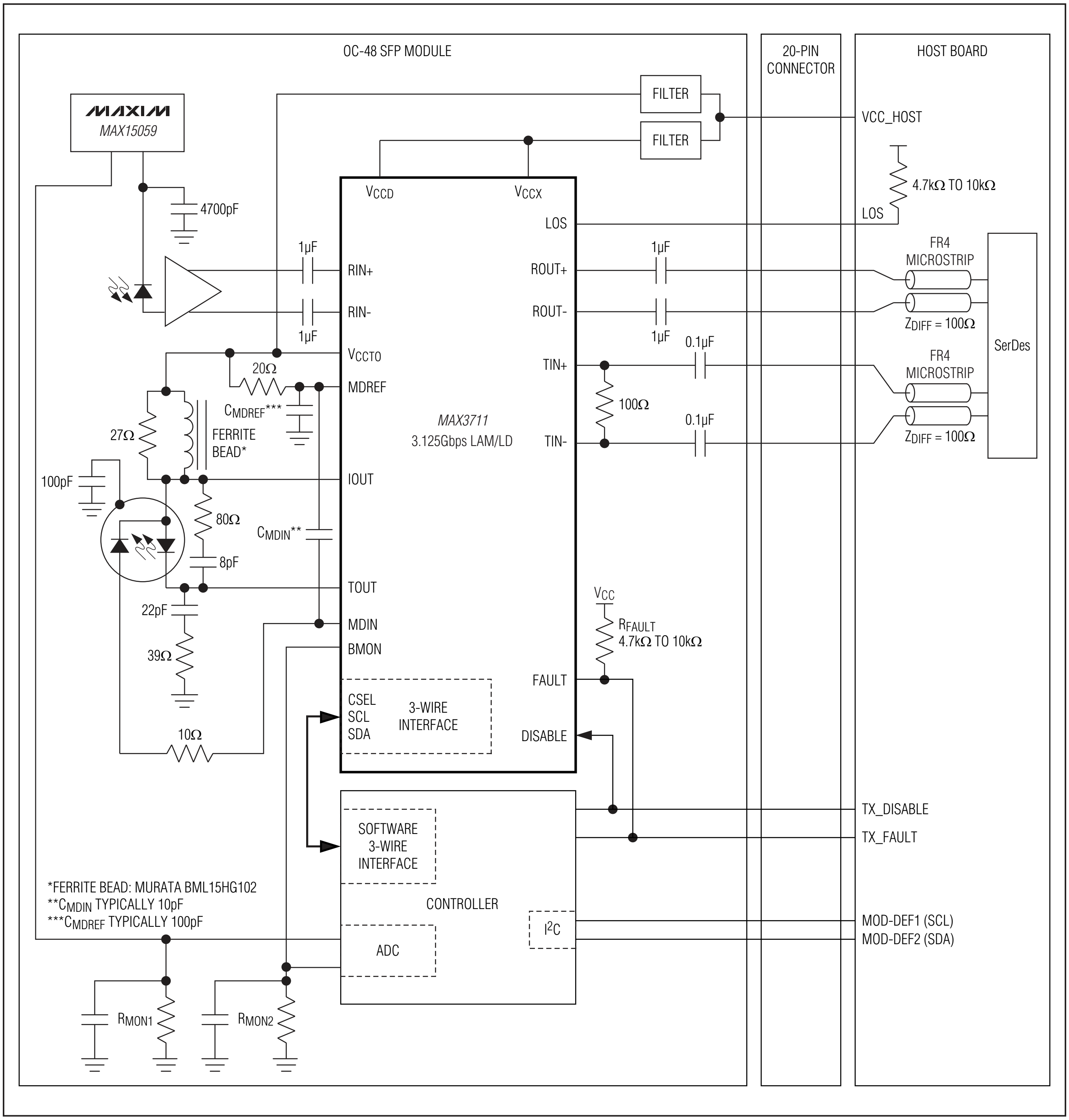
Note: *Parts are guaranteed by design and characterization to operate over the -40°C to +95°C ambient temperature range (T_A) and are tested up to +85°C.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+3	**21-0139**	**90-0021**

Typical Application Circuit—OC-48 SFP Module



125Mbps to 3.125Gbps Integrated Limiting Amplifier/ Laser Driver with Dual-Loop Power Control

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/11	Initial release	—