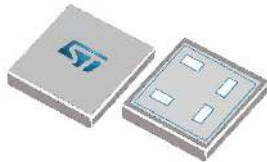


## 200 mA very low quiescent current linear regulator IC in (0.47x0.47) mm<sup>2</sup> STSTAMP™ package



STSTAMP™ (0.47x0.47) mm<sup>2</sup>

### Features

- Input voltage from 1.5 to 5.5 V
- Ultra low dropout voltage (200 mV typ. at 200 mA load)
- Very low quiescent current (20  $\mu$ A typ. at no-load, 0.03  $\mu$ A typ. in off mode)
- Output voltage tolerance:  $\pm 1.5\%$  @ 25 °C
- 200 mA guaranteed output current
- High PSRR (80 dB@1 kHz, 50 dB@100 kHz)
- Wide range of output voltages available on request: from 0.8 V up to 5.0 V in 50 mV step
- Logic-controlled electronic shutdown
- Internal soft-start
- Optional output voltage discharge feature
- Compatible with ceramic capacitor  $C_{OUT} = 0.47 \mu$ F
- Internal constant current and thermal protections
- Available in STSTAMP™ (0.47 x 0.47) mm<sup>2</sup> package
- Operating temperature range: -40 °C to 125 °C

### Applications

- Mobile phones
- Tablet
- Digital still cameras (DSC)
- Wearable devices
- Portable media players

Maturity status link

LDBL20

### Description

The LDBL20 high accuracy voltage regulator provides 200 mA of maximum current from an input voltage ranging from 1.5 V to 5.5 V, with a typical dropout voltage of 200 mV.

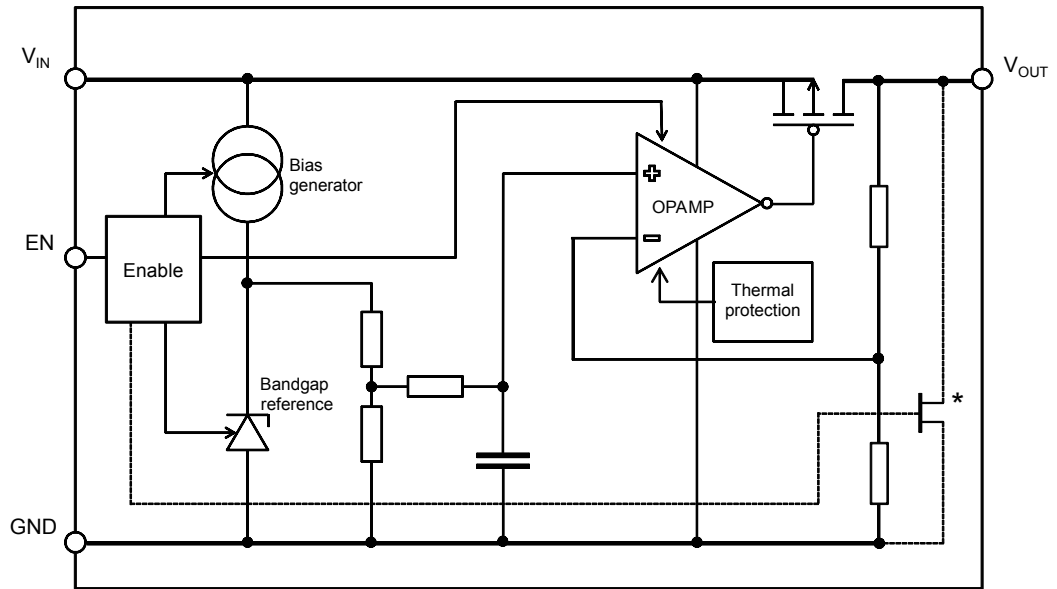
It is available in the new STSTAMP™ package, allowing the maximum space saving.

The device is stabilized with a ceramic capacitor on the output. The ultra low drop voltage, low quiescent current and low noise features, together with the internal soft-start circuit, make the LDBL20 suitable for low power battery-operated applications.

An enable logic control function puts the LDBL20 in shutdown mode with a total current consumption lower than 0.2  $\mu$ A. Constant current and thermal protection are provided.

# 1 Diagram

Figure 1. Block diagram

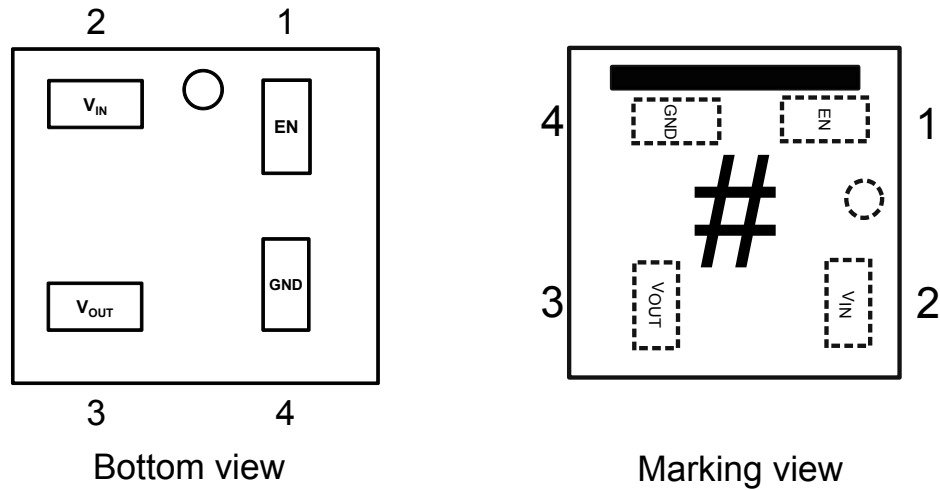


AM13852V1

Note: The output discharge MOSFET is optional.

## 2 Pin configuration

Figure 2. Pin connection



AMG110520171240MT

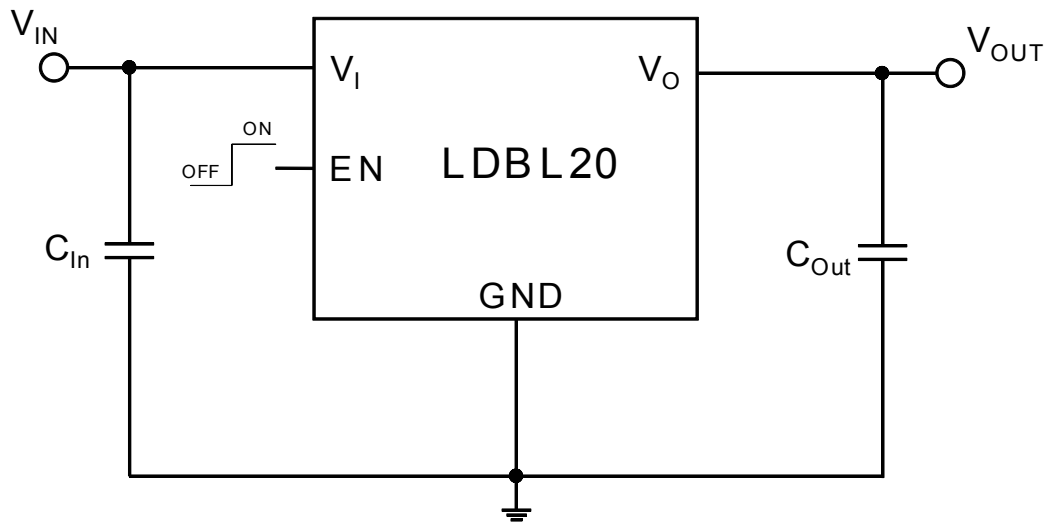
Note: "#" indicates the marking digit. Refer to Table 7. Order code. The top horizontal bar identifies pin 1 on top right corner.

Table 1. Pin description

Pin	Symbol	Function
3	OUT	Output voltage
4	GND	Common ground
1	EN	Enable pin logic input: low = shutdown, high = active
2	IN	Input voltage

### 3 Typical application

Figure 3. Typical application circuits



GIPD310820151119MT

## 4 Maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{IN}$	Input voltage	- 0.3 to 7	V
$V_{OUT}$	Output voltage	- 0.3 to $V_{IN} + 0.3$	V
$V_{EN}$	Enable input voltage	- 0.3 to 7	V
$I_{OUT}$	Output current	Internally limited	mA
$P_D$	Power dissipation	Internally limited	mW
$T_{STG}$	Storage temperature range	- 40 to 150	°C
$T_{OP}$	Operating junction temperature range	- 40 to 125	°C

*Note:* Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

**Table 3. ESD performance**

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	4	kV
		MM	400	V
		CDM	500	V

**Table 4. Thermal performance**

Symbol	Parameter	Value	Unit
$R_{thJA}$	Thermal resistance junction-ambient	230	°C/W

## 5 Electrical characteristics

$T_J = 25\text{ °C}$ ,  $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$  or  $1.5\text{ V}$ , whichever is greater,  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , unless otherwise specified.

**Table 5. LDBL20 electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating input voltage		1.5		5.5	V
$V_{OUT}$	$V_{OUT}$ accuracy	$I_{OUT} = 1\text{ mA}$ , $T_J = 25\text{ °C}$	-1.5		+1.5	%
		$I_{OUT} = 1\text{ mA}$ , $-40\text{ °C} < T_J < 125\text{ °C}$	-3		+3	%
$\Delta V_{OUT}$	Static line regulation <sup>(1)</sup>	$V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 10\text{ mA}$		0.02		%V
		$-40\text{ °C} < T_J < 125\text{ °C}$			0.2	
$\Delta V_{OUT}$	Static load regulation	$I_{OUT} = 0\text{ mA}$ to $200\text{ mA}$		10		mV
		$-40\text{ °C} < T_J < 125\text{ °C}$			0.01	%/mA
$V_{DROP}$	Dropout voltage	$I_{OUT} = 30\text{ mA}$ , $V_{OUT} = 2.8\text{ V}$		35		mV
		$I_{OUT} = 200\text{ mA}$ , $V_{OUT} = 2.8\text{ V}$ $-40\text{ °C} < T_J < 125\text{ °C}$		200	350	
$\epsilon_N$	Output noise voltage	10 Hz to 100 kHz, $I_{OUT} = 10\text{ mA}$		45		$\mu\text{V}_{RMS}/V_{OUT}$
SVR	Supply voltage rejection	$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2\text{ V}$ Frequency = 1 kHz $I_{OUT} = 30\text{ mA}$		80		dB
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2\text{ V}$ Frequency = 100 kHz $I_{OUT} = 30\text{ mA}$		55		
$I_Q$	Quiescent current	$I_{OUT} = 0\text{ mA}$		20	40	$\mu\text{A}$
		$I_{OUT} = 200\text{ mA}$		100		
$I_{Standby}$	Standby current	$V_{IN}$ input current in OFF mode: $V_{EN} = \text{GND}$		0.03	0.2	$\mu\text{A}$
$I_{SC}$	Short-circuit current	$R_L = 0$	250	350		mA
$R_{ON}$	Output voltage discharge MOSFET			100		$\Omega$
$V_{EN}$	Enable input logic low	$V_{IN} = 1.5\text{ V}$ to $5.5\text{ V}$ $-40\text{ °C} < T_J < 125\text{ °C}$			0.4	V
	Enable input logic high	$V_{IN} = 1.5\text{ V}$ to $5.5\text{ V}$ $-40\text{ °C} < T_J < 125\text{ °C}$	1			
$I_{EN}$	Enable pin input current	$V_{EN} = V_{IN}$			100	nA
$T_{ON}$ <sup>(2)</sup>	Turn-on time			100		$\mu\text{s}$
$T_{SHDN}$	Thermal shutdown			160		$\text{°C}$
	Hysteresis			20		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>OUT</sub>	Output capacitor	Capacitance	0.47		22	μF

1. *Not applicable for V<sub>out(nom)</sub> > 4.5 V*
2. *Turn-on time is time measured between the enable input just exceeding V<sub>EN</sub> high value and the output voltage just reaching 95 % of its nominal value*

## 6 Application information

### 6.1 Soft-start function

The LDBL20 has an internal soft-start circuit. By increasing the startup time up to 100  $\mu\text{s}$ , without the need of any external soft-start capacitor, this feature keeps the regulator inrush current at startup under control.

### 6.2 Output discharge function

The LDBL20 integrates a MOSFET connected between  $V_{\text{OUT}}$  and GND. This transistor is activated when the EN pin goes to low logic level and has the function to quickly discharge the output capacitor when the device is disabled by the user.

The device is available with or without the auto-discharge feature. See [Table 7. Order code](#).

### 6.3 Input and output capacitors

The LDBL20 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used but, the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR overtemperature.

Locating the input/output capacitors as closer as possible to the relative pins is recommended.

The LDBL20 requires an input capacitor with a minimum value of 1  $\mu\text{F}$ .

This capacitor must be located as closer as possible to the input pin of the device and returned to a clean analog ground.

The control loop of the LDBL20 is designed to work with an output ceramic capacitor.

This capacitor must meet the requirements of minimum capacitance and equivalent series resistance (ESR), as shown in [Figure 17. Stability area vs \( \$C\_{\text{OUT}}\$ , ESR\)](#). To assure stability, the output capacitor must maintain its ESR and capacitance in the stable region, over the full operating temperature range.

The LDBL20 shows stability with a minimum effective output capacitance of 220 nF.

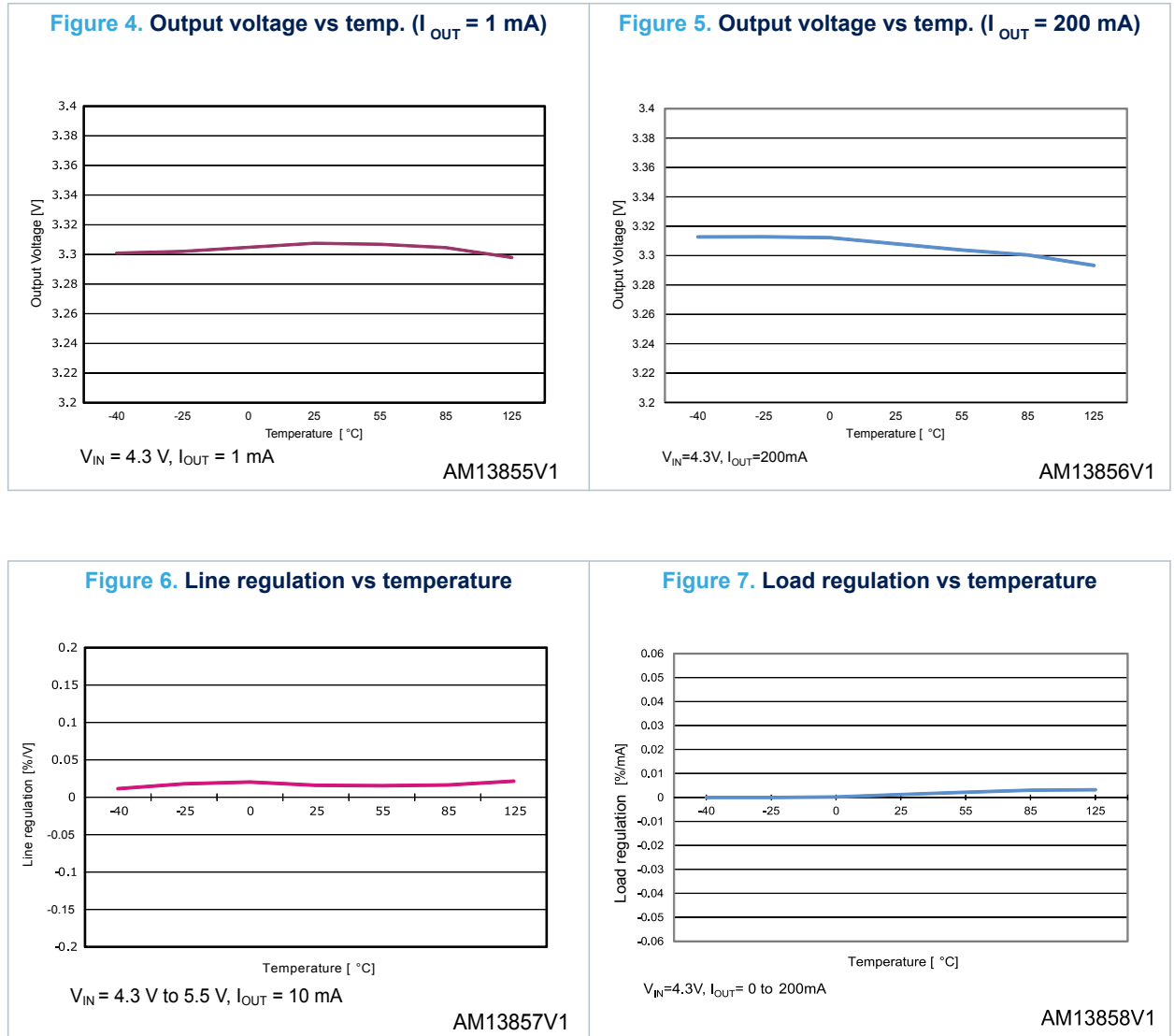
However, to keep stability in all operating conditions (temperature, input voltage and load variations), a minimum output capacitor of 0.47  $\mu\text{F}$  is recommended.

The suggested combination of 1  $\mu\text{F}$  input and output capacitors offers a good compromise among the stability of the regulator, optimum transient response and total PCB area occupation.

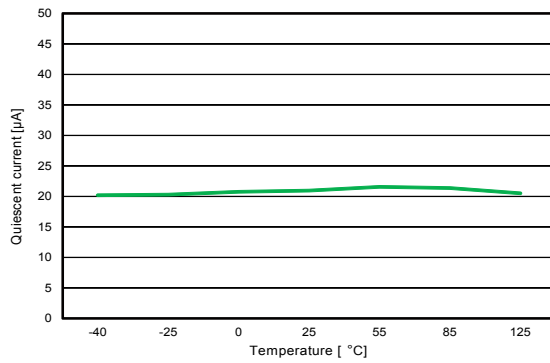


## 7 Typical characteristics

( $C_{IN} = C_{OUT} = 1 \mu F$ ,  $V_{EN}$  to  $V_{IN}$ ,  $T_J = 25 \text{ }^\circ\text{C}$  unless otherwise specified)



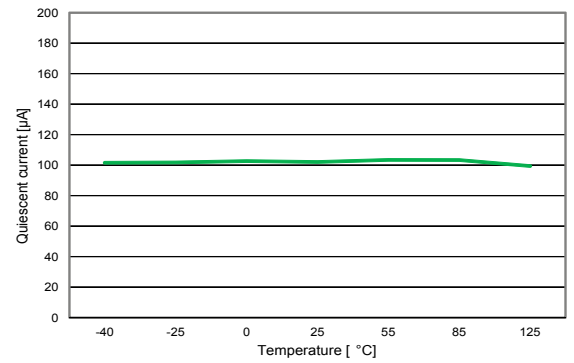
**Figure 8. Quiescent current vs temp. ( $I_{OUT} = 0 \text{ mA}$ )**



$V_{IN} = 4.3 \text{ V}, I_{OUT} = 0 \text{ mA}$

AM13859V1

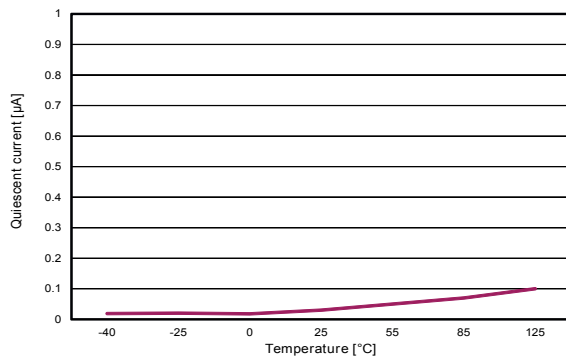
**Figure 9. Quiescent current vs temp. ( $I_{OUT} = 200 \text{ mA}$ )**



$V_{IN}=4.3\text{V}, I_{OUT}= 200\text{mA}$

AM13860V1

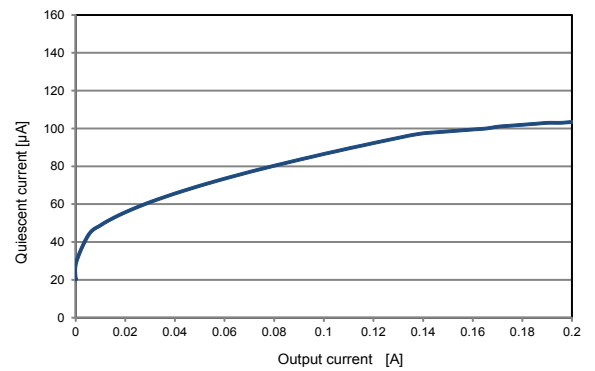
**Figure 10. Shutdown current vs temperature**



$V_{IN} = V, V_{EN} = \text{GND}$

AM13861V1

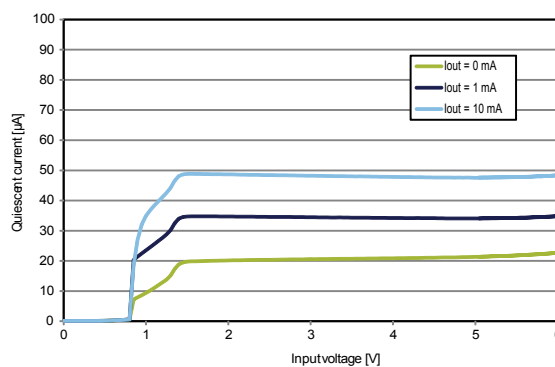
**Figure 11. Quiescent current vs load current**



$V_{IN}=2\text{V}, V_{OUT}=1\text{V}$

AM13862V1

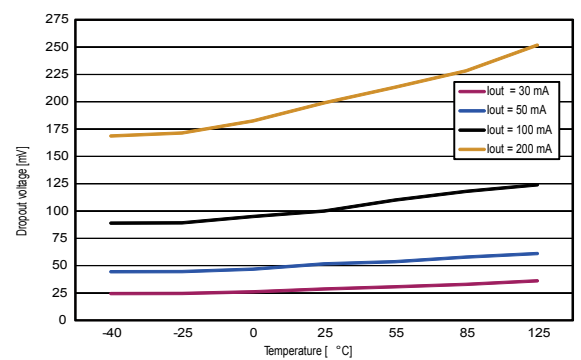
**Figure 12. Quiescent current vs input voltage**



$V_{IN} = 2 \text{ V}, V_{OUT} = 1 \text{ V}$

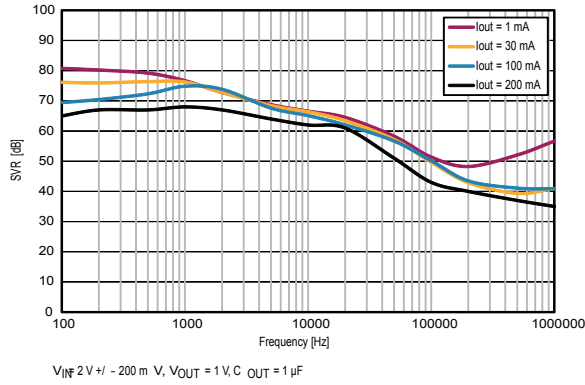
AM13863V1

**Figure 13. Dropout voltage vs temperature**



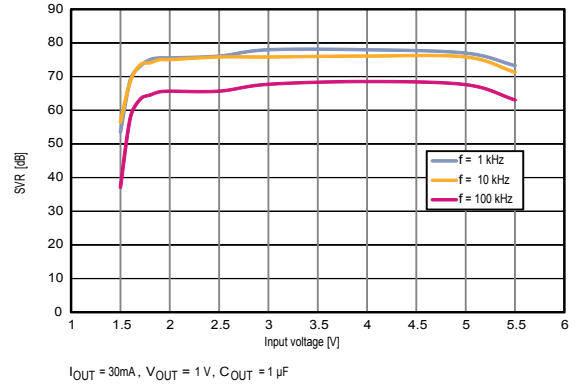
AM13864V1

**Figure 14. Supply voltage rejection vs frequency**



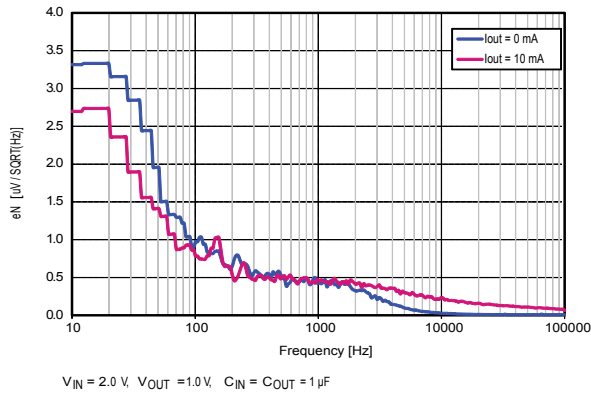
AM13865V1

**Figure 15. Supply voltage rejection vs input voltage**



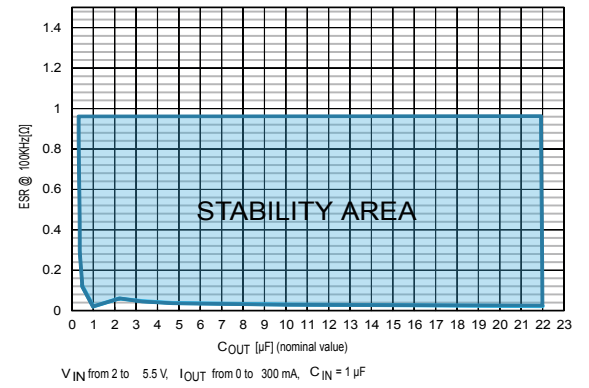
AM13866V1

**Figure 16. Output noise spectral density**



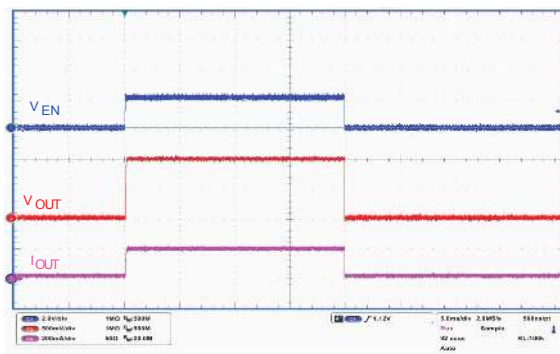
AM13867V1

**Figure 17. Stability area vs (C<sub>OUT</sub>, ESR)**



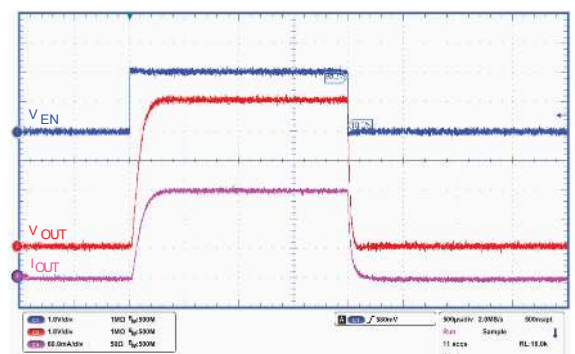
AM13868V1

**Figure 18. Enable startup ( $V_{OUT} = 1V$ )**



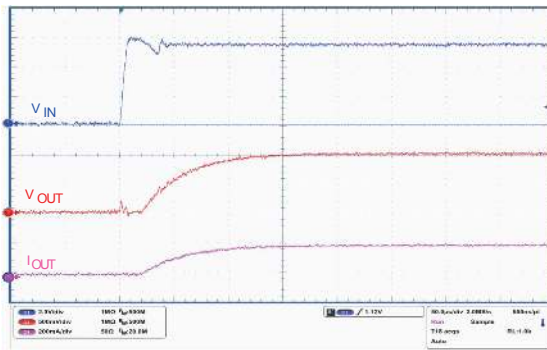
AM13869V1

**Figure 19. Enable startup ( $V_{OUT} = 5V$ )**



AM13870V1

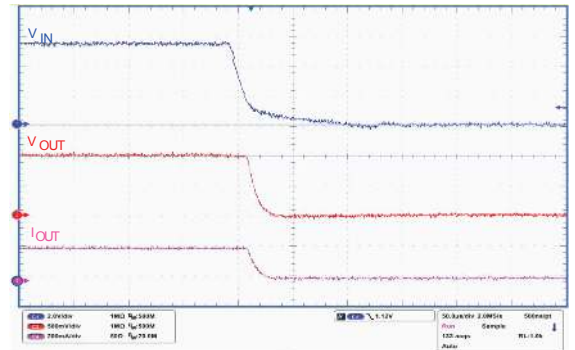
**Figure 20. Turn-on time ( $V_{OUT} = 1\text{ V}$ )**



$V_{IN} = V_{EN}$  = from 0 V to 5.5 V,  $I_{OUT} = 0.2\text{ A}$ ,  $V_{OUT} = 1\text{ V}$ ,  $T_r = 5\ \mu\text{s}$

AM13871V1

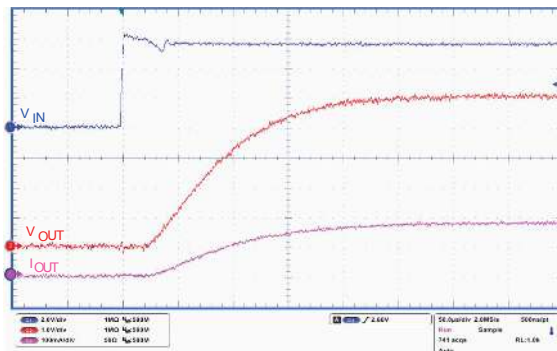
**Figure 21. Turn-off time ( $V_{OUT} = 1\text{ V}$ )**



$V_{IN} = V_{EN}$  = from 5.5 V to 0 V,  $I_{OUT} = 0.2\text{ A}$ ,  $V_{OUT} = 1\text{ V}$ ,  $T_f = 5\ \mu\text{s}$

AM13872V1

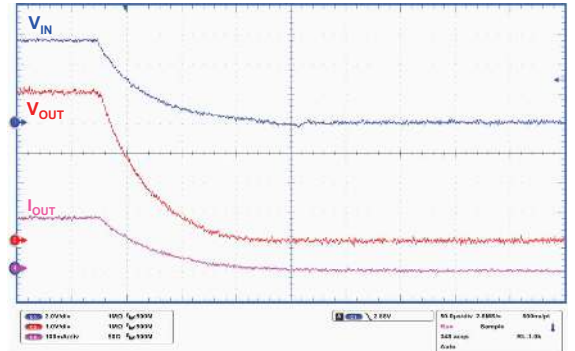
**Figure 22. Turn-on time ( $V_{OUT} = 5\text{ V}$ )**



$V_{IN} = V_{EN}$  = from 0 V to 5.5 V,  $I_{OUT} = 0.2\text{ A}$ ,  $V_{OUT} = 5\text{ V}$ ,  $T_r = 5\ \mu\text{s}$

AM13873V1

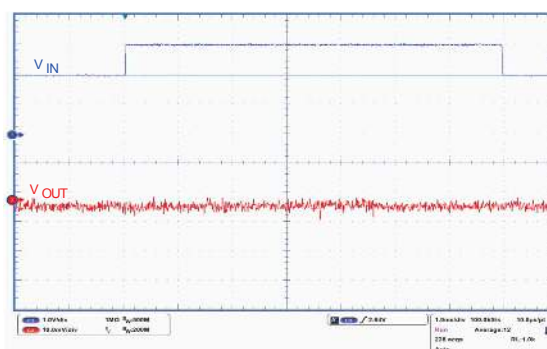
**Figure 23. Turn-off time ( $V_{OUT} = 5\text{ V}$ )**



$V_{IN} = V_{EN}$  = from 5.5 V to 0 V,  $I_{OUT} = 0.2\text{ A}$ ,  $V_{OUT} = 5\text{ V}$ ,  $T_f = 5\ \mu\text{s}$

AM13874V1

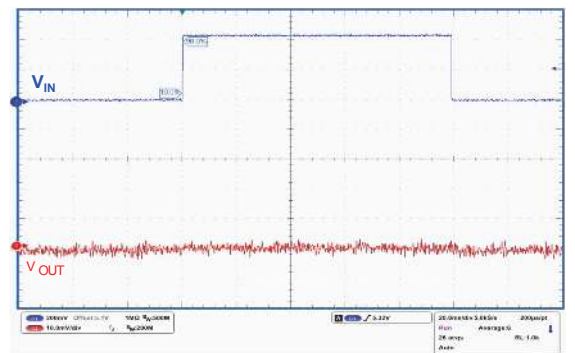
**Figure 24. Line transient ( $V_{OUT} = 1\text{ V}$ )**



$V_{IN} = V_{EN}$  = from 2 V to 3 V,  $I_{OUT} = 10\text{ mA}$ ,  $V_{OUT} = 1\text{ V}$ ,  $T_r = T_f = 5\ \mu\text{s}$

AM13875V1

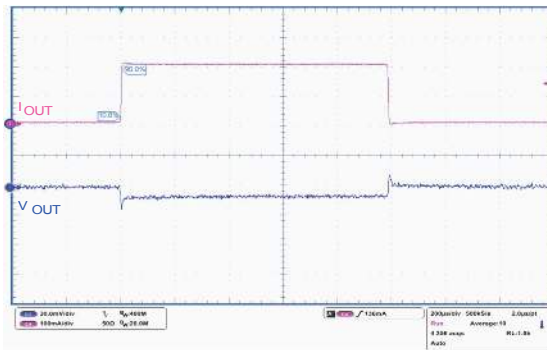
**Figure 25. Line transient ( $V_{OUT} = 5\text{ V}$ )**



$V_{IN} = V_{EN}$  = from 5.1 V to 5.5 V,  $I_{OUT} = 10\text{ mA}$ ,  $V_{OUT} = 5\text{ V}$ ,  $T_r = T_f = 5\ \mu\text{s}$

AM13876V1

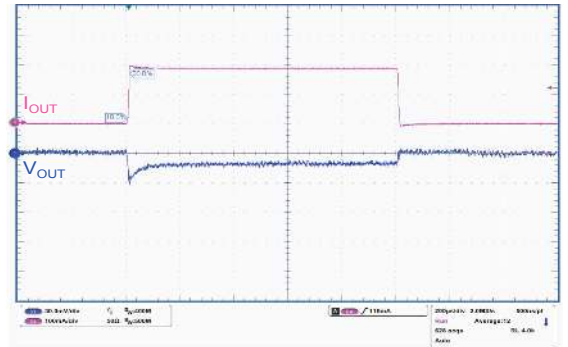
**Figure 26. Load transient ( $V_{OUT} = 1\text{ V}$ )**



$V_{IN} = V_{EN} = 2\text{ V}$ ,  $I_{OUT}$  = from 0 to 0.2 A ,  $V_{OUT} = 1\text{ V}$ ,  $t_r = t_f = 5\ \mu\text{s}$

AM13877V1

**Figure 27. Load transient ( $V_{OUT} = 5\text{ V}$ )**



$V_{IN} = V_{EN} = 5.5\text{ V}$ ,  $I_{OUT}$  = from 0 to 0.2 A ,  $V_{OUT} = 5\text{ V}$ ,  $t_r = t_f = 5\ \mu\text{s}$

AM13878V1

## 8 Recommendation on PCB assembly

### 8.1 PCB design recommendations

- PCB PAD design: non solder mask defined
- PCB pad size: see drawing in [Figure 30](#). STSTAMP™ (0.47x0.47) mm<sup>2</sup> recommended footprint
- Solder mask opening: 50 µm between the edge of the pad and the edge of the solder mask
- To keep under control the solder paste amount, closed vias are recommended instead of open vias
- The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to reduce the effect of tilt phenomena caused by asymmetrical solder paste amount due to the solder flowing away

### 8.2 Stencil

- Stencil aperture: see drawing in [Figure 31](#). STSTAMP™ (0.47x0.47) mm<sup>2</sup> recommended solder stencil
- Stencil thickness: 75 µm

### 8.3 Solder paste

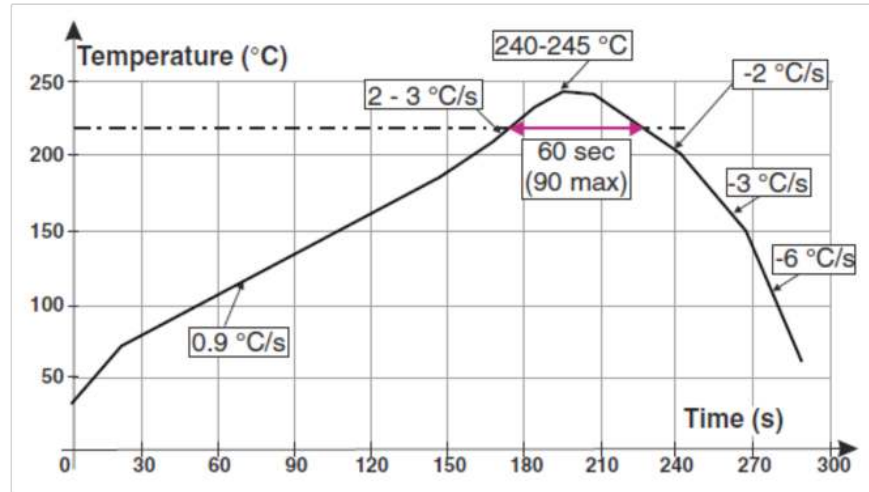
- 95.8% Sn, 3.5% Ag, 0.7% Cu solder paste
- Halide-free flux qualification ROL0 according to ANSI/J-STD-004
- “No clean” solder paste is recommended.
- Offers a high tack force to resist component movement during high speed
- Solder paste with fine particles: powder particle size is 20-45 µm. • type 4

### 8.4 Placement

- Manual positioning is not recommended
- It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
- Standard tolerance of ± 0.05 mm is recommended
- 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages
- To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool
- For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools

## 8.5 Reflow profile

Figure 28. ST ECOPACK® recommended soldering reflow profile for PCB mounting



AMG110520171340MT

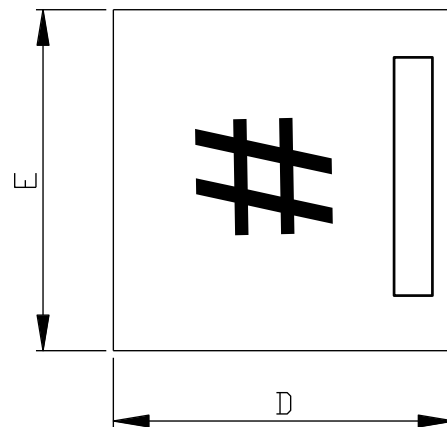
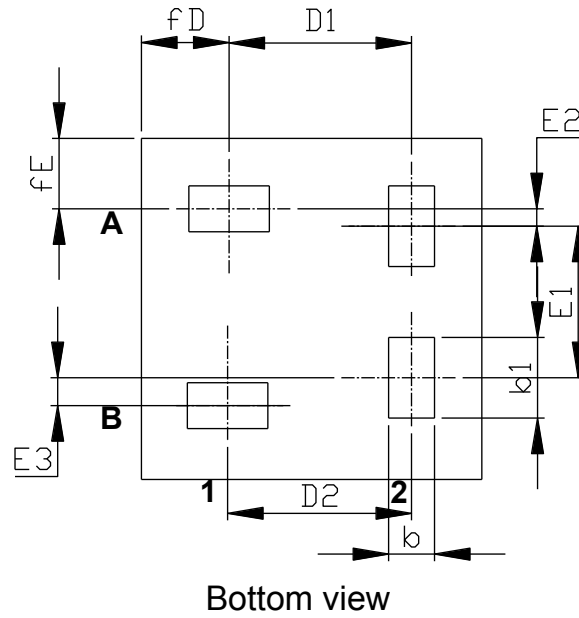
Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

## 9 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

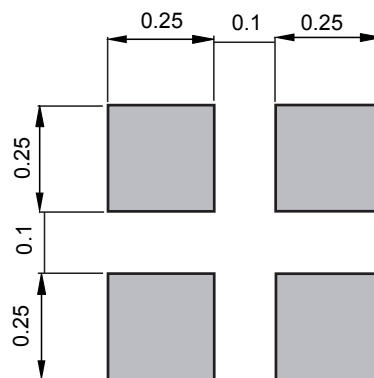
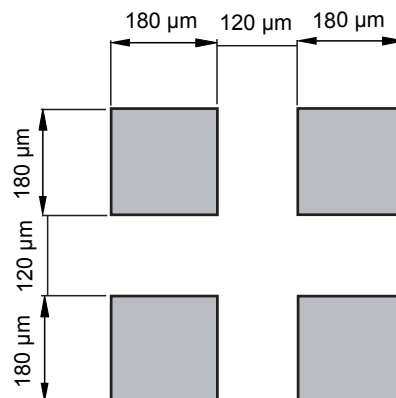


**9.1 STSTAMP™ (0.47x0.47) mm<sup>2</sup> package information**
**Figure 29. STSTAMP™ (0.47x0.47) mm<sup>2</sup> package outline**

**Marking view**

8351431\_D

**Table 6. STSTAMP™ (0.47x0.47) mm<sup>2</sup> mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.18	0.200	0.220
b	0.060	0.065	0.070
b1	0.109	0.114	0.119
E	0.450	0.480	0.510
E1	0.208	0.213	0.218
E2	0.019	0.024	0.029
E3	0.034	0.039	0.044
D	0.450	0.480	0.510
D1	0.252	0.257	0.262
D2	0.255	0.260	0.265
fE	0.095	0.101	0.106
fD	0.106	0.111	0.116

**Figure 30. STSTAMP™ (0.47x0.47) mm<sup>2</sup> recommended footprint**

**Figure 31. STSTAMP™ (0.47x0.47) mm<sup>2</sup> recommended solder stencil**


## 10 Order code

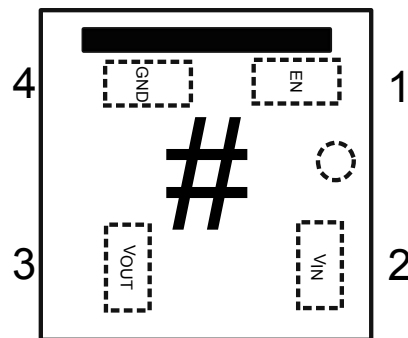
**Table 7. Order code**

Order code	Output voltage (V)	Auto-discharge	Marking	Packing
LDBL20D-11 <sup>(1)</sup>	1.1	Yes		Tape and reel
LDBL20D-12	1.2		D	
LDBL20D-18R	1.8		A	
LDBL20D-25R	2.5		B	
LDBL20D-33R	3.3		C	

1. Available on request.

### 10.1 Marking information

**Figure 32. Marking composition (marking view)**



AMG110520171241MT

*Note:* The symbol "#" indicates the marking digit, as per Table 7. Order code.

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
10-Nov-2015	1	Initial release
02-Aug-2017	2	Updated Section 2: "Pin configuration", Table 5: "LDBL20 electrical characteristics". Added Section 8: "Recommendation on PCB assembly". Updated Section 10: "Ordering information". Minor text changes.
27-Jan-2021	3	Added new order codes in <a href="#">Table 7</a> .

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