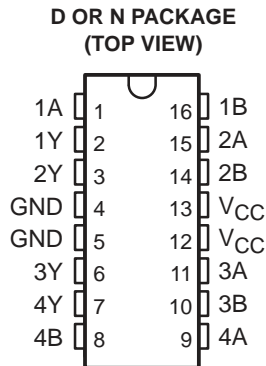


# 74AC11086 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS081A – NOVEMBER 1989 – REVISED APRIL 1996

- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (N)



## description

This device contains four independent 2-input exclusive-OR gates. It performs the Boolean function  $Y = A \oplus B = \bar{A}B + A\bar{B}$  in positive logic.

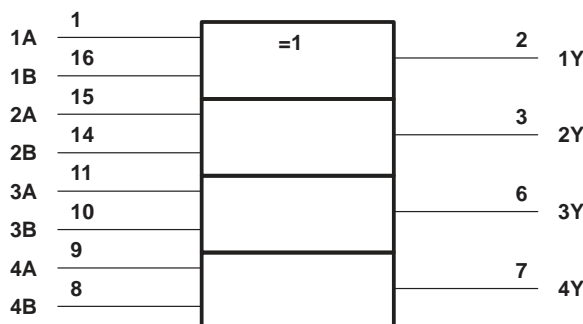
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The 74AC11086 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE  
(each gate)**

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

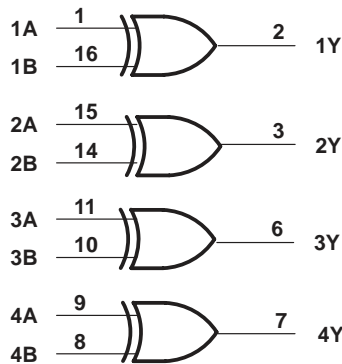
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

# 74AC11086 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS081A – NOVEMBER 1989 – REVISED APRIL 1996

## logic diagram (positive logic)



## exclusive-OR logic

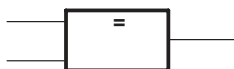
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

### EXCLUSIVE OR



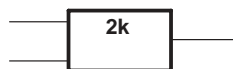
These are five equivalent exclusive-OR symbols valid for a 74AC11086 gate in positive logic; negation may be shown at any two ports.

### LOGIC-IDENTITY ELEMENT



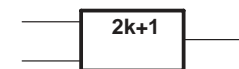
The output is active (high) if all inputs stand at the same logic level (i.e.,  $A=B$ ).

### EVEN-PARITY ELEMENT



The output is active (high) if an even number of inputs (i.e., 0 or 2) are active (high).

### ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active (high).

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package .....	1.3 W
..... N package .....	1.1 W
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

# 74AC11086 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS081A – NOVEMBER 1989 – REVISED APRIL 1996

## recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 5.5 V	3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V	0.9		V
		V <sub>CC</sub> = 4.5 V	1.35		
		V <sub>CC</sub> = 5.5 V	1.65		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V	-4		mA
		V <sub>CC</sub> = 4.5 V	-24		
		V <sub>CC</sub> = 5.5 V	-24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V	12		mA
		V <sub>CC</sub> = 4.5 V	24		
		V <sub>CC</sub> = 5.5 V	24		
Δt/Δv	Input transition rise or fall rate	0	10		ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9		2.9		V	
		4.5 V	4.4		4.4			
		5.5 V	5.4		5.4			
	I <sub>OH</sub> = -4 mA	3 V	2.58		2.48			
		4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V			3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V			0.1		V	
		4.5 V			0.1			
		5.5 V			0.1			
	I <sub>OL</sub> = 12 mA	3 V	0.36		0.44			
		4.5 V	0.36		0.44			
		5.5 V	0.36		0.44			
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V			1.65				
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±0.1		±1		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	4		40		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	3.5				pF	

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

# 74AC11086 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS081A – NOVEMBER 1989 – REVISED APRIL 1996

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	1.5	5.6	9.4	1.5	10.6	ns
$t_{PHL}$			1.5	5.1	7.4	1.5	8.2	

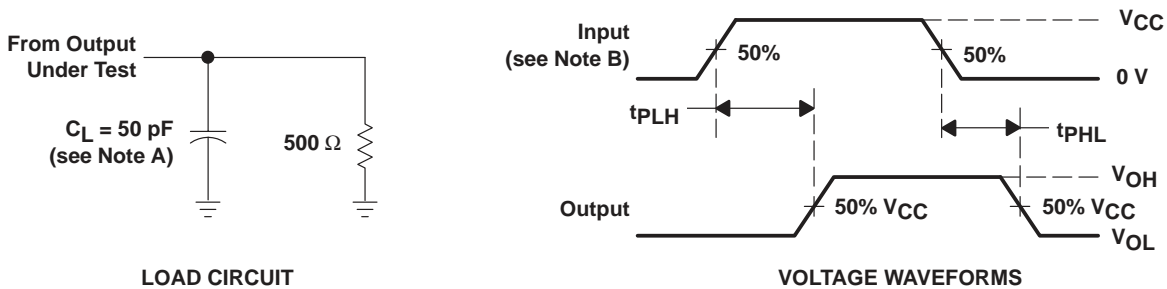
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	1.5	3.8	6.8	1.5	7.6	ns
$t_{PHL}$			1.5	3.8	6.2	1.5	6.8	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per gate	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	27	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.