Apacer

RoHS Recast Compliant

Industrial SDHC/XC 5.0

CV110-SD Product Specifications

(Kioxia TLC BiCS3 64 Layers)

April 19, 2022

Version 1.5

Specifications Overview:

- **Fully Compatible with SD Card Association Specifications**
  - Physical Layer Specification Ver6.1
  - Security Specification Ver4.0

- **Capacity**
  - 32, 64, 128, 256 GB

- **Performance[1]**
  - Sequential read: Up to 85 MB/sec
  - Sequential write: Up to 32 MB/sec
  - Random read (4K): Up to 1,500 IOPS
  - Random write (4K): Up to 600 IOPS

- **Flash Management**
  - Built-in advanced ECC algorithm
  - Global Wear Leveling
  - Flash bad-block management
  - Power Failure Management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - SMART Read Refresh™

- **NAND Flash Type:** Kioxia TLC BiCS3 64 Layers

- **SD-Protocol Compatible**

- **Supports SD SPI Mode**

- **Backward Compatible with 3.0 and 2.0**

- **Endurance (in Terabytes Written: TBW)**
  - 32 GB: 48 TBW
  - 64 GB: 94 TBW
  - 128 GB: 163 TBW
  - 256 GB: 342 TBW

- **Temperature Range**
  - Operating:
    - Standard: -25°C to 85°C
    - Wide: -40°C to 85°C
  - Storage: -40°C to 85°C

- **Operating Voltage: 2.7V ~ 3.6V**

- **Power Consumption[1]**
  - Operating: 95 mA
  - Standby: 160 μA

- **Bus Speed Mode:** Supports Class 10 with U1 and UHS-I[2]
  - SDR12: SDR up to 25MHz 1.8V signaling
  - SDR25: SDR up to 50MHz 1.8V signaling
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
  - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

- **Physical Dimensions**
  - 32mm (L) x 24mm (W) x 2.1mm (H)

- **Supports Video Speed Class**
  - V10: 32 GB
  - V30: 64-256 GB

- **RoHS Recast Compliant**

Notes:
1. Varies from capacities. Performance values presented here are typical and measured based on USB 3.0 card reader. The results may vary depending on settings and platforms.
2. Timing in 1.8V signaling is different from that of 3.3V signaling. Operation mode selection command is complaint with SD 3.0, referring to SDA's Part 1, Physical Layer Specification, Ver 3.01 (Section 3.9).

Table of Contents

1. General Description

Apacer SD CV110-SD is compatible with the SD card version 5.0. The command list supports [Physical Layer Specification Ver6.10 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver4.00 Final] Specifications.

The SD 5.0 card comes with 9-pin interface designed to operate at a maximum operating frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. It supports capacity up to 256GB with exFAT SDXC.

Apacer SD CV110-SD Secure Digital 5.0 card with high performance, good reliability and wide compatibility is nowadays one of the most popular cards well adapted for hand-held applications with customized firmware techniques in semi-industrial/medical markets already.

1.1 Functional Block

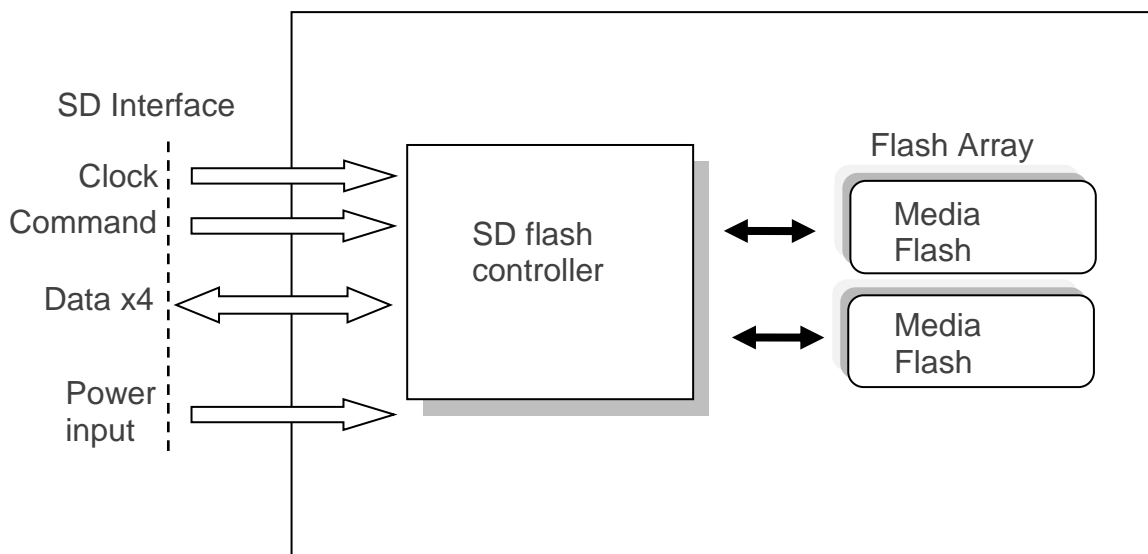The SD contains a flash controller and flash media with SD standard interface.

Figure 1-1 Functional Block Diagram

1.2 Flash Management

1.2.1 Bad Block Management

The SD controller contains logical/physical flash block mapping and bad block management system. It will manage all flash block include user data space and spare block.

The SD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD replaces this bad bit with a spare bit within the sector header. If necessary, the SD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.2.2 Powerful ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the SD card applies the advanced ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.2.3 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer's SD and MicroSD cards. Note that this tool can only support Apacer's industrial SD and MicroSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

1.2.4 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

1.2.5 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

1.2.6 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

1.2.7 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

2. Product Specifications

2.1 Card Architecture

Write Enabled   Write Protected
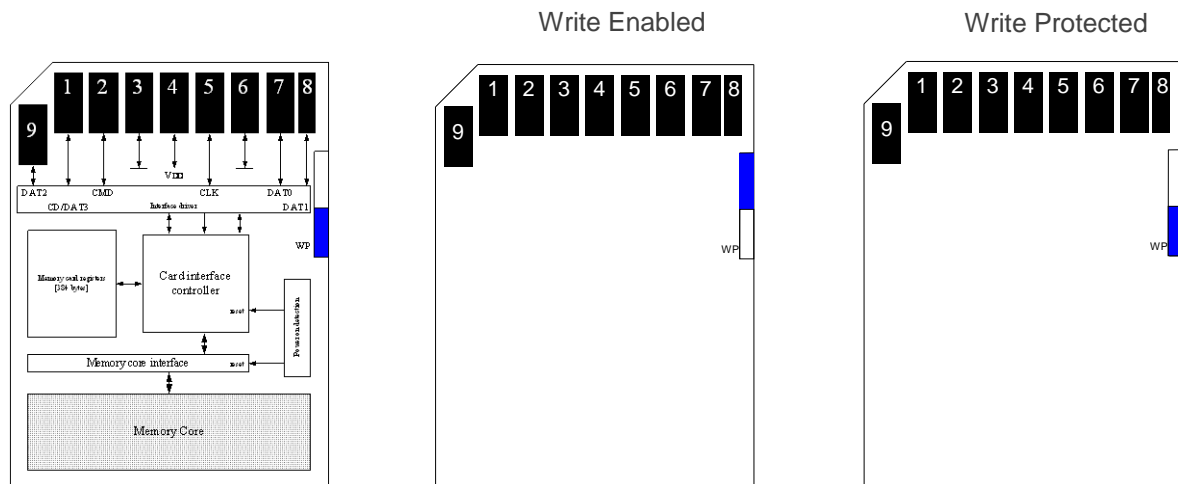
Figure 2-1 Card Architecture

2.2 Pin Assignments

Table 2-1 Pin Assignments

Pin	SD Mode		SPI Mode	
	Name	**Description**	**Name**	**Description**
1	CD/DAT3	Card detect/Data line[Bit 3]	CS	Chip select
2	CMD	Command/Response	DI	Data in
3	VSS1	Supply voltage ground	VSS	Supply voltage ground
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS2	Supply voltage ground	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]	DO	Data out
8	DAT1	Data line[Bit 1]	Reserved	
9	DAT2	Data line[Bit 2]	Reserved	

2.3 Capacity

The following table shows the specific capacity for the SD 5.0 card.

Table 2-2 Capacity Specifications

Capacity	Total bytes
32 GB	31,033,655,296
64 GB	62,243,471,360
128 GB	124,755,378,176
256 GB	249,443,647,488

Note: Total bytes are viewed under Windows operating system and were measured by SD format too.

2.4 Performance

Performances of the SD 5.0 card are shown in the table below.

Table 2-3 Performance Specifications

Capacity Performance	32 GB	64 GB	128 GB	256 GB
Sequential Read* (MB/s)	85	85	80	85
Sequential Write* (MB/s)	20	27	32	32
Random Read IOPS** (4K)	1,400	1,500	1,500	1,500
Random Write IOPS** (4K)	500	600	600	600

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 32.
- Performance results are measured based on USB 3.0 card reader.

2.5 Electrical

Table 2-4 Operating Voltages

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power Supply Voltage	2.7	3.6	V

Table 2-5 Power Consumption

Capacity Mode	32 GB	64 GB	128 GB	256 GB
Operating (mA)	70	75	90	95
Standby (µA)	85	95	120	160

Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.
- Power is measured based on USB 3.0 card reader.

2.6 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 2-6 Endurance Specifications

| Capacity	TeraBytes Written
32 GB	48
64 GB	94
128 GB	163
256 GB	342

Notes:
- This estimation complies with Apacer internal workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB

3. Physical Characteristics

3.1 Physical Dimensions

Dimensions: 32 ㎜ (L) x 24 ㎜ (W) x 2.1 ㎜ (H)

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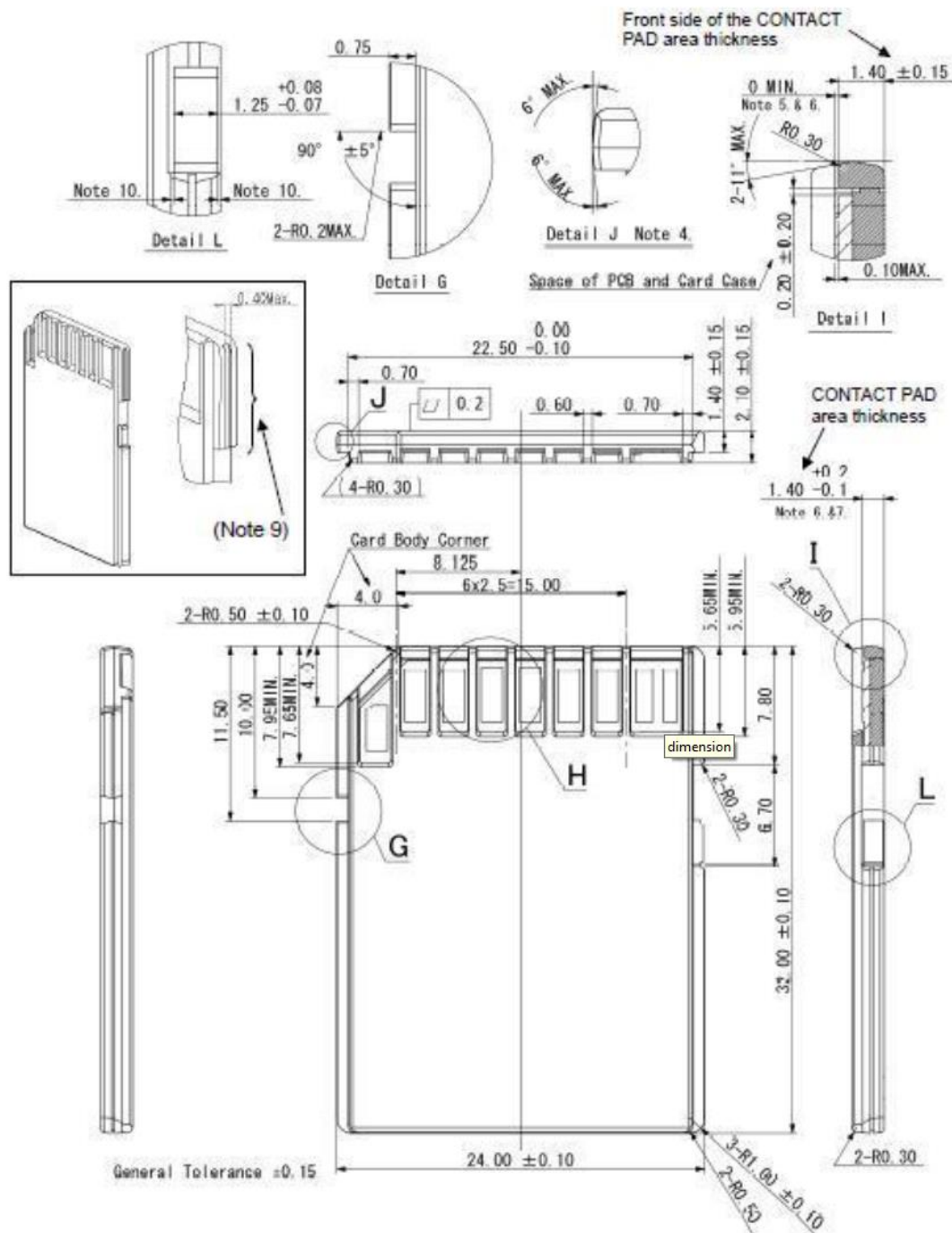
3.2 Durability Specifications

Table 3-1 Durability Specifications

Item	Specifications
Temperature	-25°C to 85°C (Standard) -40°C to 85°C (Wide)
	-40°C to 85°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	1.5m free fall, 6 surfaces of each
Bending	≧ 10N, hold 1min/5times
Torque	0.15N-m or 2.5deg, hold 30 seconds/ 5 times
Salt spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance, Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card ;storage for 30 mins)
Switch cycle	0.4~0.5N, 1000 times
Durability	10,000 times mating cycle
ESD	Contact: +/-4KV each item 25 times Air: +/-8KV 10 times

4. DC Characteristics

4.1 SD Interface Timing (Default)
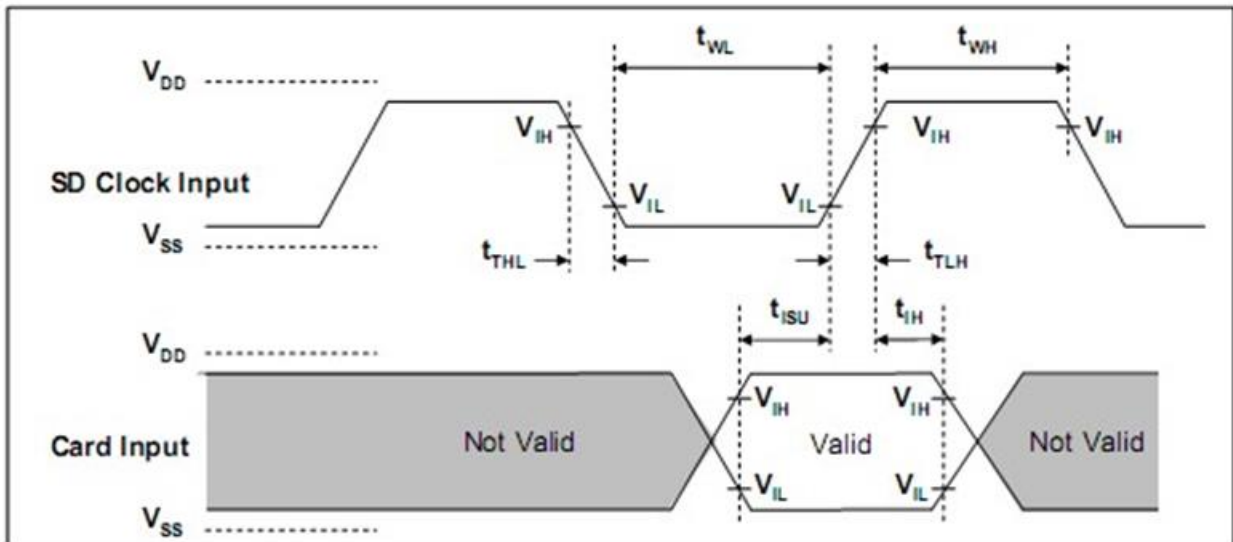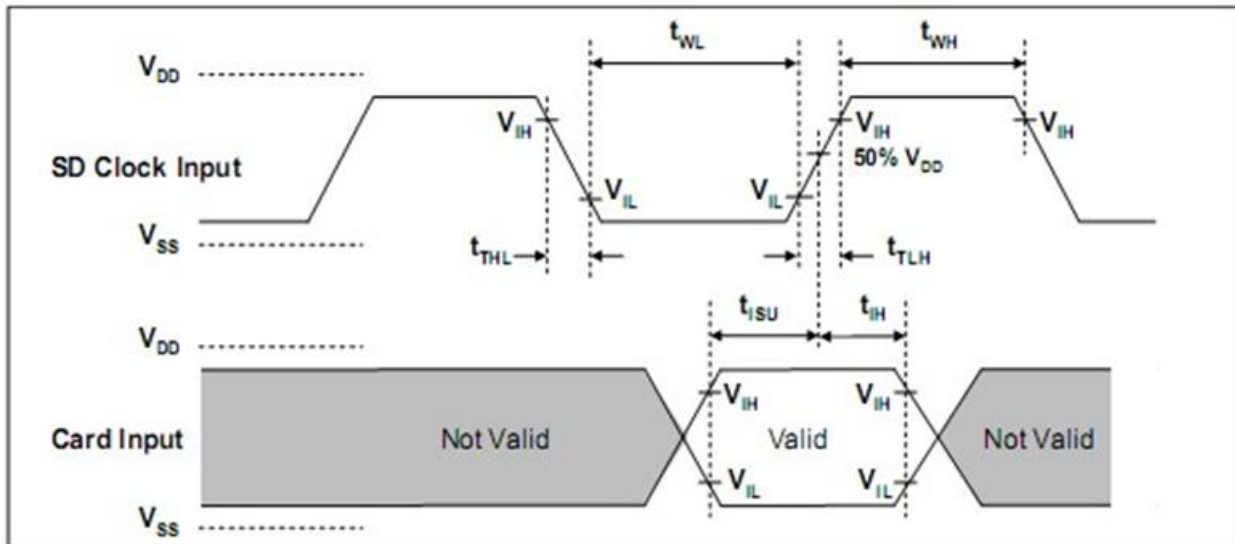

Card input Timing (Default Speed Card)
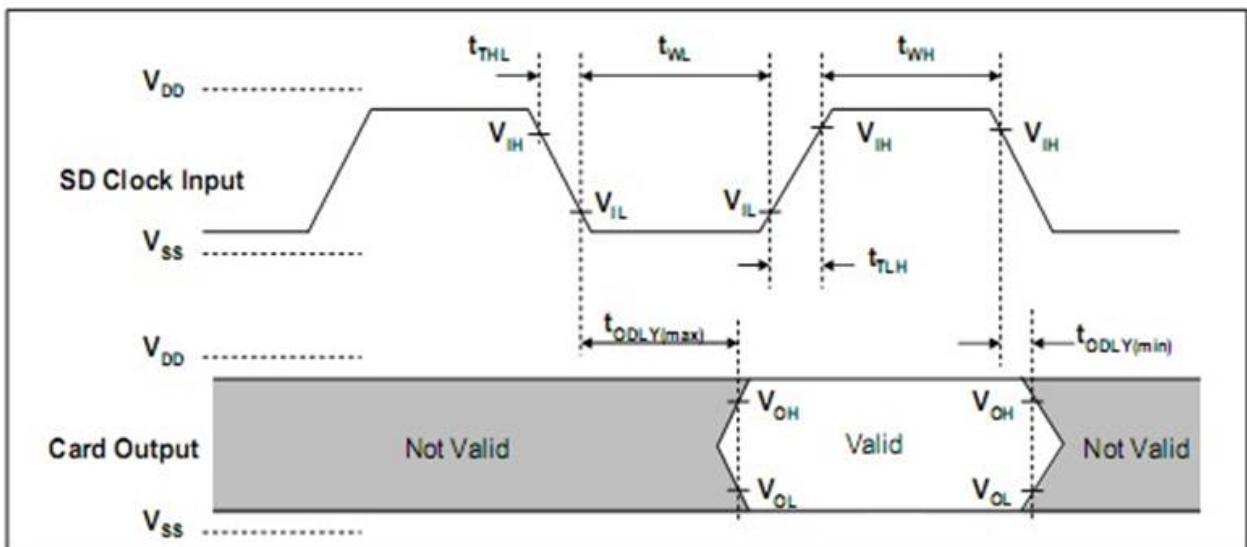
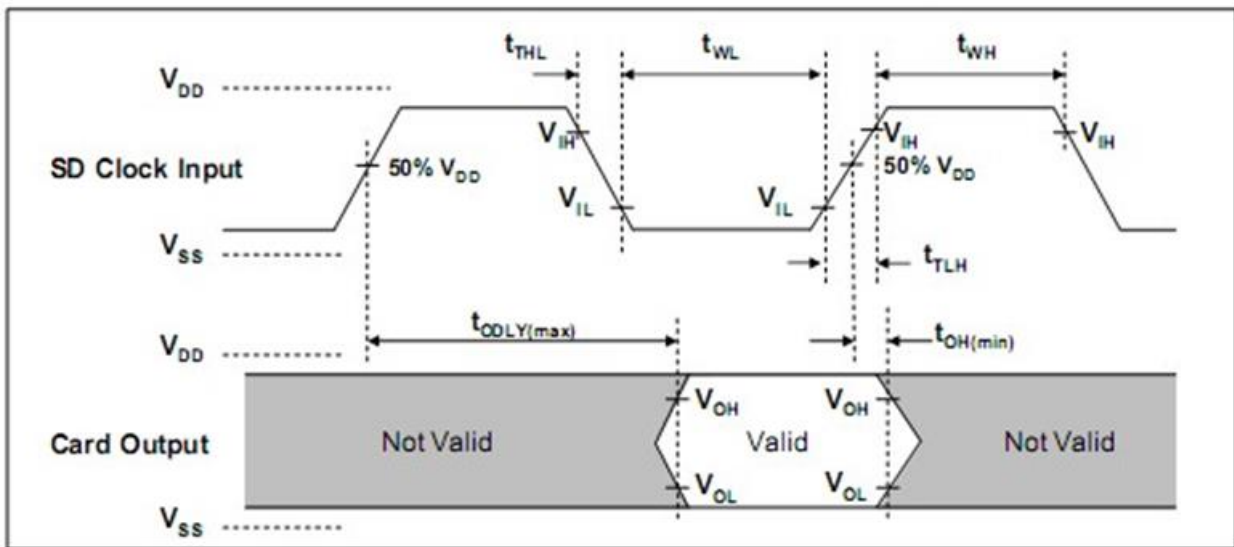Card Output Timing (Default Speed Mode)

Symbol	Parameter	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V$_{IH}$) and max(V$_{IL}$))					
f$_{PP}$	Clock frequency Data Transfer Mode	0	25	MHz	C$_{card}$ ≤ 10 pF (1 card)
f$_{OD}$	Clock frequency Identification Mode	0*/100	400	kHz	C$_{card}$ ≤ 10 pF (1 card)
t$_{WL}$	Clock low time	10		ns	C$_{card}$ ≤ 10 pF (1 card)
t$_{WH}$	Clock high time	10		ns	C$_{card}$ ≤ 10 pF (1 card)
t$_{TLH}$	Clock rise time		10	ns	C$_{card}$ ≤ 10 pF (1 card)
t$_{THL}$	Clock fall time		10	ns	C$_{card}$ ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
t$_{ISU}$	Input setup time	5		ns	C$_{card}$ ≤ 10 pF (1 card)
t$_{IH}$	Input hold time	5		ns	C$_{card}$ ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
t$_{ODLY}$	Output Delay time during Data Transfer Mode	0	14	ns	C$_L$ ≤ 40 pF (1 card)
t$_{ODLY}$	Output Delay time during Identification Mode	0	50	ns	C$_L$ ≤ 40 pF (1 card)

*0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 SD Interface Timing (High-Speed Mode)

**Card Input Timing (High Speed Card)**

Card Output Timing (High Speed Mode)

Symbol	Parameter	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	50	MHz	Ccard ≤ 10 pF (1 card)
t_{WL}	Clock low time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{WH}	Clock high time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	3	ns	Ccard ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	3	ns	Ccard ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	6	-	ns	Ccard ≤ 10 pF (1 card)
t_{TH}	Input hold time	2	-	ns	Ccard ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer made	-	14	ns	CL ≤ 40 pF (1 card)
t_{OH}	Output hold time	2.5	-	ns	CL ≥ 15 pF (1 card)
C_L	Total system capacitance for each line*	-	40	pF	1 card

*In order to satisfy severe timing, host shall run on only one card

4.3 SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

4.3.1 Input
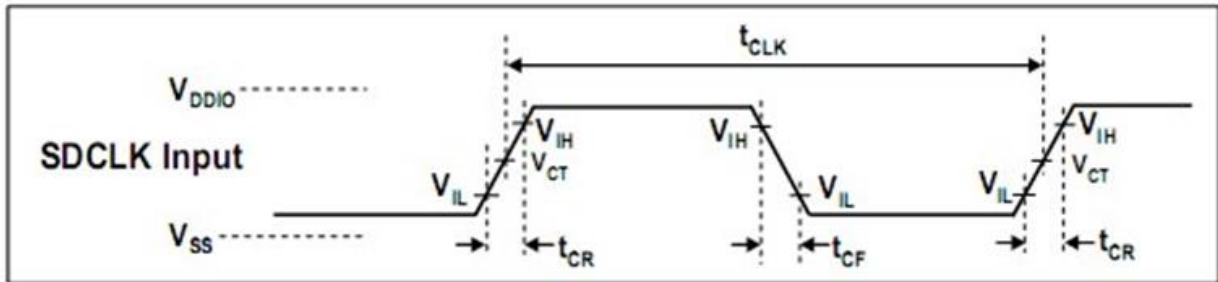
Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 2.00ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

SDR12, SDR25, SDR50 and SDR104 Input Timing
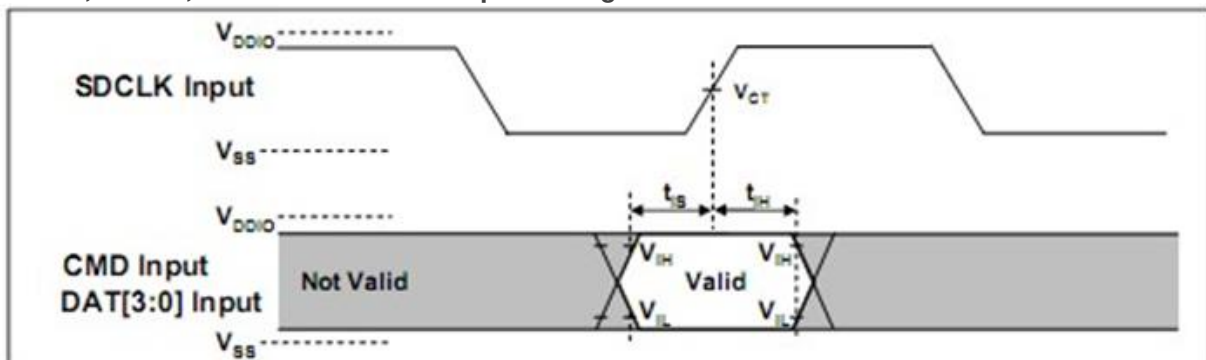
Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	Min	Max	Unit	SDR12, SDR25 and SDR50 Modes
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

4.3.2 Output
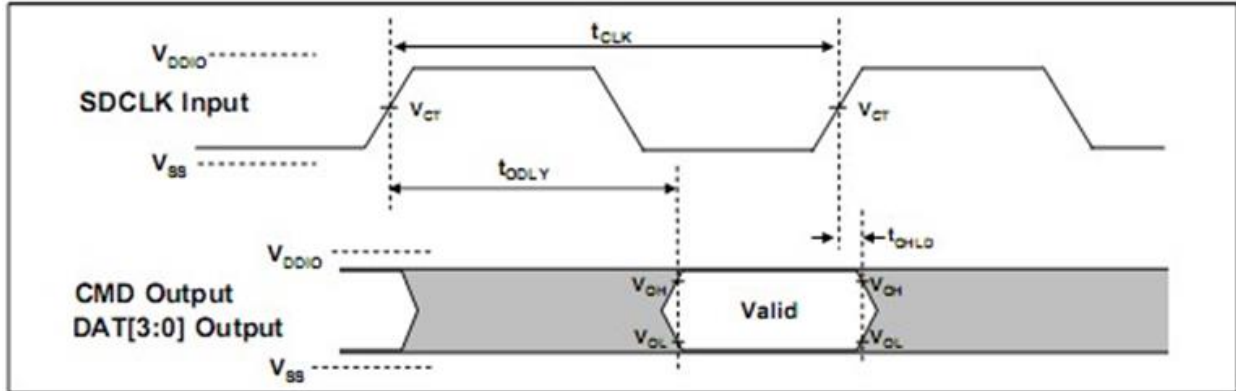
Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, C_L=30pF, using driver Type B, for SDR50.
t_{ODLY}	-	14	ns	t_{CLK} ≥20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). C_L=15pF

Output (SDR104 mode)
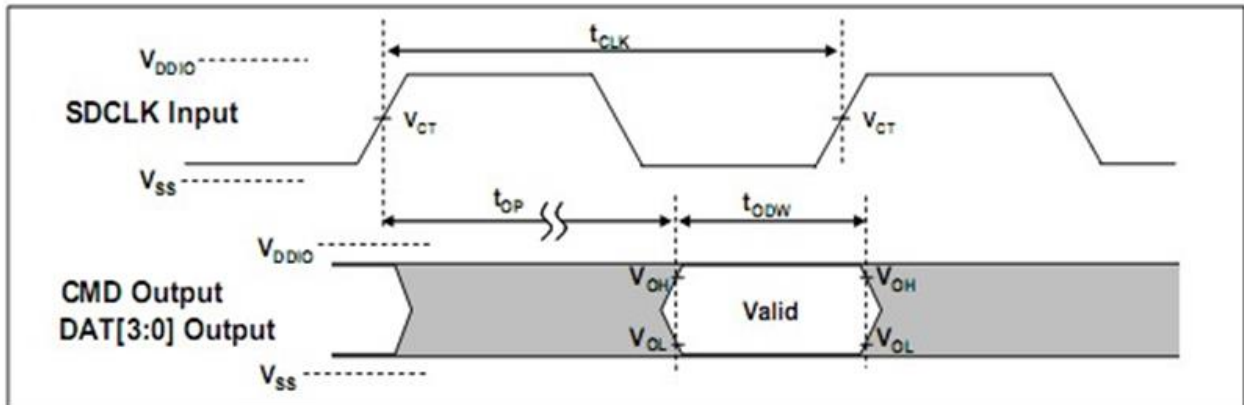
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.4 SD Interface Timing (DDR50 Mode)
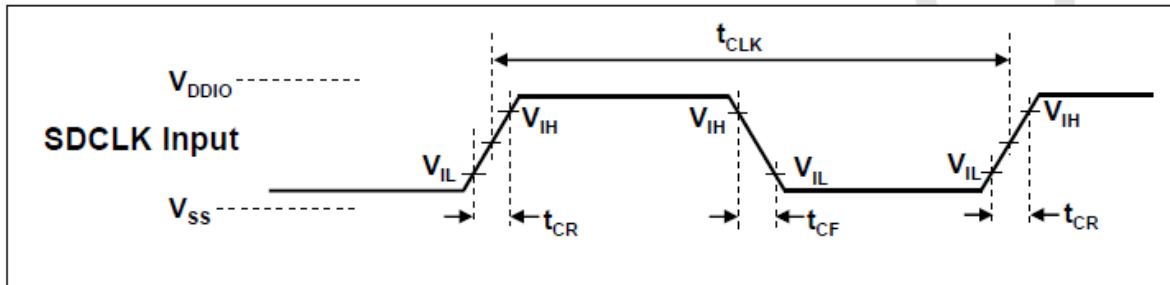
Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2 t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line)

Available timing window for card output transition

Available timing window for host to sample data from card
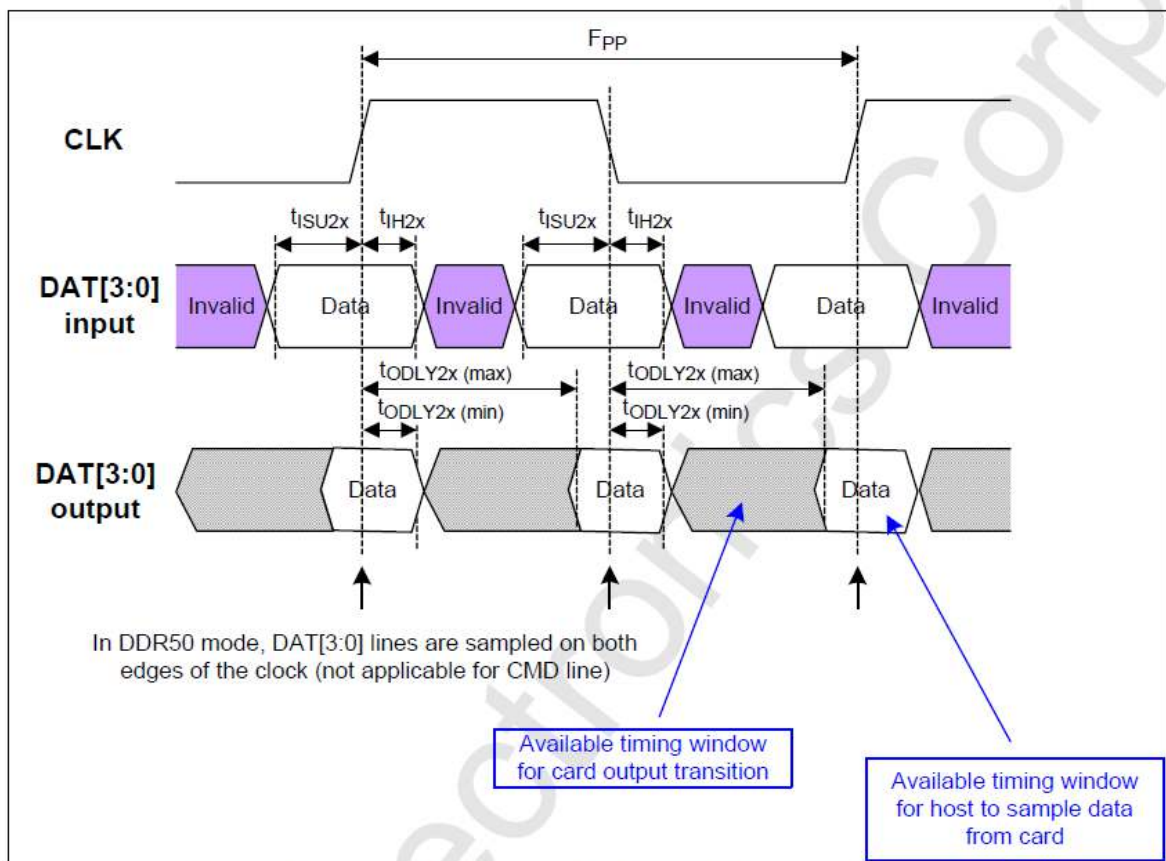
Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameter	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input setup time	6	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	$C_L \leq 30$ pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input setup time	3	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	$C_L \leq 25$ pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)

5. S.M.A.R.T.

5.1 Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:

[31:24]	[23:16]	[15:18]	[7:1]	[0]
Argument #3	Argument #2	Argument #1	Index	"1/0"
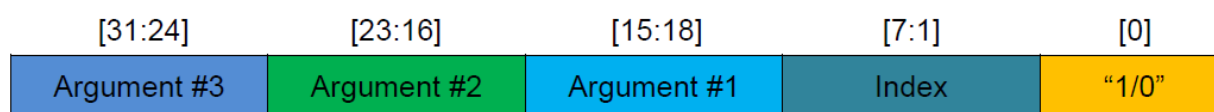
- Bit [0]: Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.

- Bit [7:1]: Indicates the index of the function to be executed:

    - Read Mode: Index = 0x10 Get SMART Command Information

    - Write Mode: Index = 0x08 Pre-Load SMART Command Information

- Bit [15:8]: Function argument #1 (1-byte)

- Bit [23:16]: Function argument #2 (1-byte)

- Bit [31:24]: Function argument #3 (1-byte)

5.2 Process for Retrieving SMART Data

Retrieving SMART data requires the following two commands executed in sequence and in accordance with the SD Association standard flowchart for CMD56 (see below).

Step 1: Write Mode – [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] "0" (Write Mode) [1:7] "0001 000" (Index = 0x08) [8:511] All '0' (Reserved)	No expected data

Step 2: Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56	[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:31] All '0' (Reserved)	1 sector (512 bytes) of response data byte[0-8] Flash ID byte[9-10] IC Version byte[11-12] FW Version byte[13] Reserved byte[14] CE Number byte[15] Reserved byte[16-17] Bad Block Replace Maximum byte[18] Reserved byte[32-63] Bad Block count per Die byte[64-65] Good Block Rate(%) byte[66-79] Reserved byte[80-83] Total Erase Count byte[84-95] Reserved byte[96-97] Endurance (Remain Life) (%) byte[98-99] Average Erase Count – L* byte[100-101] Minimum Erase Count – L* byte[102-103] Maximum Erase Count – L* byte[104-105] Average Erase Count – H* byte[106-107] Minimum Erase Count – H* byte[108-109] Maximum Erase Count – H* byte[110-111] Reserved byte[112-115] Power Up Count byte[116-127] Reserved byte[128-129] Abnormal Power Off Count byte[130-159] Reserved byte[160-161] Total Refresh Count byte[176-183] Product "Marker" byte[184-215] Bad Block count per Die byte[216-511] Reserved

*Please refer to technical note for High/Low byte definition.

Figure 5-1: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

6. Product Ordering Information

6.1 Product Code Designations

Apacer's CV110-SD is available in different configurations and densities. See the chart below for a comprehensive list of options for the CV110-SD series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	J	6	.	1	1	2	X	X	A	.	X	X	X	1	0

Code 1-3 (Product Line & Form Factor)	CV110-SD
Code 5-6 (Model/Solution)	CV110
Code 7-8 (Product Capacity)	2F: 32GB 2G: 64GB 2H: 128GB 2J: 256GB
Code 9 (Flash Type & Product Temp)	G: 3D TLC Standard Temperature H: 3D TLC Wide Temperature
Code 10 (Product Spec)	SD Card
Code 12-14 (Version Number)	Random number generated by system
Code 15-16 (Firmware Version)	Firmware page mode

6.2 Valid Combinations

The following table lists the available models of the CV110-SD series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Standard Temperature	Wide Temperature
32GB	AJ6.112FGA.00110	AJ6.112FHA.00110
64GB	AJ6.112GGA.00110	AJ6.112GHA.00110
128GB	AJ6.112HGA.00110	AJ6.112HHA.00110
256GB	AJ6.112JGA.00110	AJ6.112JHA.00110

Revision History

Revision	Description	Date
0.1	Preliminary release	9/9/2019
1.0	- Completed endurance rating for 64GB - Added Power Failure Management to Flash Management on Specifications Overview - Added 1.2.5 Power Failure Management	10/3/2019
1.1	Updated supported bus mode to Class 10 with U3 and UHS-I at Bus Speed Mode on Specifications Overview	3/31/2020
1.2	Changed support for U3 to U1 at Bus Speed Mode on Specifications Overview page	4/8/2021
1.3	- Updated Performance and Power Consumption on Specifications Overview page - Updated Tables 2-3 and 2-5 - Updated 6. Product Ordering Information due to FW change	6/1/2021
1.4	- Removed DataRAID support - Updated NAND flash type on the cover page and Specifications Overview page from Toshiba to Kioxia	6/9/2021
1.5	Modified SD card version from 6.1 to 5.0	4/19/2022

Global Presence

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