5V TTL to Differential ECL Translator

Description

The MC10ELT/100ELT24 is a TTL to differential ECL translator. Because ECL levels are used a +5 V, -5.2 V (or -4.5 V) and ground are required. The small outline 8-lead package and the single gate of the ELT24 makes it ideal for those applications where space, performance and low power are at a premium.

The 100 Series contains temperature compensation.

Features

- 0.8 ns t_{PHL}, 0.95 ns t_{PLH} Typical Propagation Delay
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts
- Operating Range: $V_{CC} = 4.5 \text{ V}$ to 5.5 V; $V_{EE} = -4.2 \text{ V}$ to -5.5 V with GND = 0 V
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant



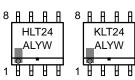
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MARKING DIAGRAMS*



SOIC-8 D SUFFIX CASE 751





TSSOP-8 DT SUFFIX CASE 948R









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H = MC10 A = Assembly Location
K = MC100 L = Wafer Lot
5E = MC10 Y = Year
2T = MC100 W = Work Week
M = Date Code ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

^{*}For additional marking information, refer to Application Note AND8002/D.

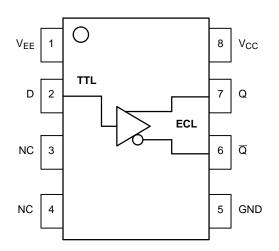


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
Q, Q	ECL Differential Outputs*
D	TTL Input
V _{CC}	Positive Supply
V _{EE}	Negative Supply
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

^{*}Output state undetermined when inputs are open.

Table 2. ATTRIBUTES

Charac	cteristics	Value			
Internal Input Pulldown Resist	Internal Input Pulldown Resistor				
Internal Input Pullup Resistor		N/A			
ESD Protection	Human Body Model Machine Model	> 4 kV > 200 V			
Moisture Sensitivity, Indefinite	Time Out of Drypack (Note 1)	Pb-Free Pkg			
	SOIC-8 TSSOP-8 DFN8	Level 1 Level 3 Level 1			
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in			
Transistor Count		51 Devices			
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test					

^{1.} For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V	V _{EE} = -5.0 V	7	V
V _{EE}	Negative Power Supply	GND = 0 V	V _{CC} = +5.0 V	-8	V
V _{IN}	Input Voltage	GND = 0 V	$V_{I} \leq V_{CC}$	0 to V _{CC}	V
l _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SO-8 SO-8	190 130	°C/W
θЈС	Thermal Resistance (Junction-to-Case)	Standard Board	SO-8	41 to 44	°C/W
$\theta_{\sf JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ±5%	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W
T _{sol}	Wave Solder Pb-Free	<2 to 3 sec @ 260°C		265	°C
θЈС	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. 10ELT SERIES NECL OUTPUT DC CHARACTERISTICS $V_{CC} = 5.0 \text{ V}$; $V_{EE} = -5.0 \text{ V}$; $V_{EE} = -5.0$

		-40°C		25°C		85°C					
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Icc	V _{CC} Power Supply Current			7.0		4.5	7.0			7.0	mA
I _{EE}	Power Supply Current			18		12.5	18			18	mA
V _{OH}	Output HIGH Voltage (Note 4)	-1080	-990	-890	-980	-895	-810	-910	-815	-720	mV
V _{OL}	Output LOW Voltage (Note 4)	-1950	-1800	-1650	-1950	-1790	-1630	-1950	-1773	-1595	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 3. Output parameters vary 1:1 with GND. V_{CC} can vary 4.5 V / 5.5 V. V_{EE} can vary -4.2 V / -5.5 V.
- 4. Outputs are terminated through a 50 Ω resistor to GND 2 V.

Table 5. 100ELT SERIES NECL OUTPUT DC CHARACTERISTICS $V_{CC} = 5.0 \text{ V}$; $V_{EE} = -5.0 \text{ V}$; $V_{EE} = -5.0 \text{ V}$; $V_{CC} = 5.0 \text{ V}$; $V_{CC} =$

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Icc	V _{CC} Power Supply Current			7.0		4.5	7.0			7.0	mA
I _{EE}	Power Supply Current			18		12.5	18			18	mA
V _{OH}	Output HIGH Voltage (Note 6)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage (Note 6)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 5. Output parameters vary 1:1 with GND. V_{CC} can vary 4.5 V / 5.5 V. V_{EE} can vary -4.2 V / -5.5 V.
- 6. Outputs are terminated through a 50 Ω resistor to GND 2 V.

^{2.} JEDEC standard multilayer board - 2S2P (2 signal, 2 power)

Table 6. TTL INPUT DC CHARACTERISTICS V_{CC} = 4.5 V to 5.5 V; V_{EE} = -4.2 V to -5.5 V; GND = 0.0 V; T_A = -40°C to +85°C

Symbol	Characteristic	Condition	Min	Тур	Max	Unit
I _{IH}	Input HIGH Current	V _{IN} = 2.7 V			20	μΑ
I _{IHH}	Input HIGH Current	V _{IN} = 7.0 V			100	μΑ
I _{IL}	Input LOW Current	V _{IN} = 0.5 V			-0.6	mA
V _{IK}	Input Clamp Diode Voltage	$I_{IN} = -18 \text{ mA}$			-1.2	V
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 7. AC CHARACTERISTICS $V_{CC} = 4.5 \text{ V}$ to 5.5 V; $V_{EE} = -4.2 \text{ V}$ to -5.5 V; GND = 0.0 V

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Toggle Frequency					400					MHz
t _{PLH}	Propagation Delay (Note 7) 1.5 V to 50%	0.5		2.0	0.5	0.95	2.0	0.5		2.0	ns
t _{PHL}	Propagation Delay (Note 7) 1.5 V to 50%	0.5		2.0	0.5	0.8	2.0	0.5		2.0	ns
t _{JITTER}	Random Clock Jitter (RMS)					2.5					ps
t _r /t _f	Output Rise/Fall Time (20–80%)	0.25		1.25	0.25		1.25	0.25		1.25	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

7. Specifications for standard TTL input signal.

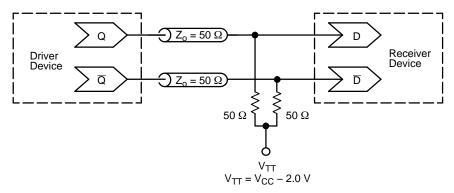


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10ELT24DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC10ELT24DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT24DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10ELT24DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT24MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel
MC100ELT24DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100ELT24DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT24DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100ELT24DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT24MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AN1672/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

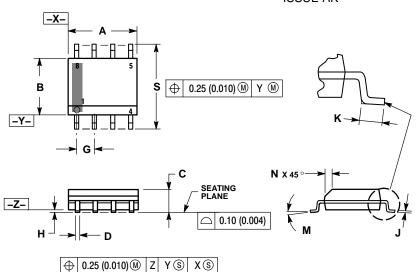
AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SOIC-8 NB CASE 751-07 **ISSUE AK**



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

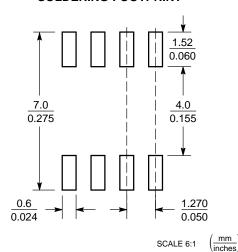
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

 6. 751–01 THRU 751–06 ARE OBSOLETE. NEW STANDARD IS 751–07.
- STANDARD IS 751-07.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27	7 BSC	0.050 BSC		
H	0.10	0.25	0.004	0.010	
7	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
M	0 °	8 °	0 °	8 °	
Z	0.25	0.50	0.010	0.020	
s	5.80	6.20	0.228	0.244	

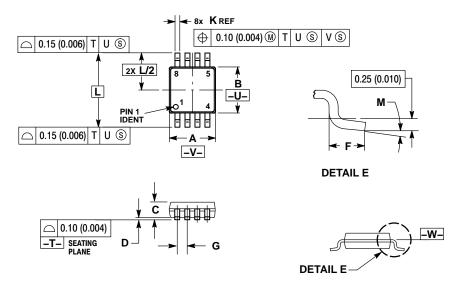
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-8 **DT SUFFIX** CASE 948R-02 **ISSUE A**



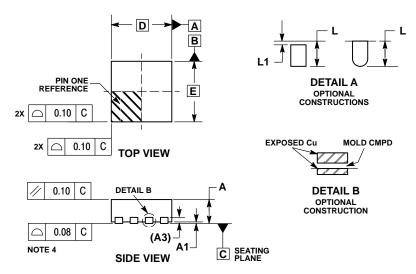
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH.
 PROTRUSIONS OR GATE BURRS. MOLD FLASH
 OR GATE BURRS SHALL NOT EXCEED 0.15
- On ONTE SUPING STALL NOT EXCEED 0.19
 O.006) PER SIDE.

 DIMENSION B DOES NOT INCLUDE INTERLEAD
 FLASH OR PROTRUSION, INTERLEAD FLASH OR
 PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	2.90	3.10	0.114	0.122	
В	2.90	3.10	0.114	0.122	
С	0.80	1.10	0.031	0.043	
D	0.05	0.15	0.002	0.006	
F	0.40	0.70	0.016	0.028	
G	0.65	BSC	0.026	BSC	
K	0.25	0.40	0.010	0.016	
Ĺ	4.90	BSC	0.193 BSC		
8.6	00	C 0	00	C 0	

PACKAGE DIMENSIONS

DFN8 2x2, 0.5P CASE 506AA ISSUE E

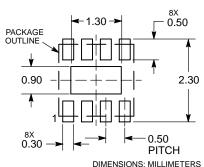


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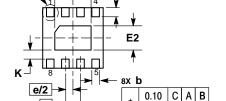
- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994 . CONTROLLING DIMENSION: MILLIMETERS. DIMENSION 6 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
 COPLANARITY APPLIES TO THE EXPOSED
- PAD AS WELL AS THE TERMINALS

	MILLIMETERS				
DIM	MIN	MAX			
Α	0.80	1.00			
A1	0.00	0.05			
A3	0.20	REF			
b	0.20	0.30			
D	2.00	BSC			
D2	1.10	1.30			
E	2.00	BSC			
E2	0.70	0.90			
е	0.50	BSC			
K	0.30	REF			
L	0.25	0.35			
L1		0.10			

RECOMMENDED **SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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0.05 C NOTE 3

BOTTOM VIEW

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DETAIL A

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