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Chapter 1. Introduction



1.1 General Description

AP3928 is an off-line universal AC Voltage input step-down regulator which provides accurate constant voltage (CV) output, outstanding low standby power, high efficiency at light loading and excellent dynamic response based on non-isolated buck topology.

The AP3928 EV1 Evaluation Board provides a good design example for a cost-effective 9.9W single output 18V/550mA power application used in home appliances.

1.2 AP3928 Key Features

- Universal 85V to 265V V_{AC} Input
- Internal MOSFET 700V (6.5Ω max)
- Maximum 600mA rated Output current
- Low Standby Power Consumption (<30mW at no load)
- High Light-Loading and Average efficiency can meet DOE and CoC requirement
- Frequency Modulation to suppress EMI to meet EN55022 class B
- Rich Protection including: OTP, OLP, OLD, SCP
- Extremely low system component count
- Totally Lead-free & Fully RoHS Compliant (SO-8)
- Halogen and Antimony Free. "Green" Device

1.3 Applications

- Non-Isolated Home Appliances: AC Fans, Rice Cookers, Air conditioners, Coffee Machines, Soy Milk Machines, etc.
- Auxiliary Power for IoT Devices.

1.4 Board Pictures



Figure 1: Top View

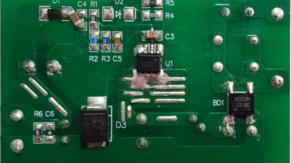


Figure 2: Bottom View



Chapter 2. Power Supply Specification

2.1 System Performance

The system performance contains input/output characters, specifications, EMC, protections, and etc.

			Min.	Тур.	Max.	Comments
				Input Characters		
Inpu	Input AC voltage rating		100V/60Hz	115/230	240V/50Hz	
Inpu	nput AC voltage range		85V/60Hz	-	265V/50Hz	Two wires, no PE
Input AC frequency range		cy range	47Hz	50/60	63Hz	
				Dutput Characters		
Output voltage Output tolerance		17.1V 18V 18.9V		18.9V	Tested at board terminal	
		ance	-		±5%	rested at board terminal
	Loading current			550		mA
			Meas	urement Performanc	e	
	Input AC voltage range Input AC frequency range Output voltage Output tolerance Loading current Standby power I15Vac 10% loac Avg. eff. 230Vac 10% loac	ower	-	16.5mW		@230V/50Hz
	1151/00	10% load		87.88%	-	
Efficiency standard	115Vac	Avg. eff.		86.81%	-	DoE VI: 71.97%
	2201/22	10% load		85.39%		CoC V5 tier 2: 72.03%/62.03%
	230Vac	Avg. eff.		85.82%		
Load regulation		-	- ±2.19% -		Tested at board terminal	
	Line regulat	ion	-	±0.28%	-	Tested at board terminal
·		ise	-	57.6mV	-	@full load and full voltage range
	Startup tim	ne	-	18.6ms	-	85V/60Hz
				EMC Test		
Standby power - 16.5mW @230Va 115Vac 10% load 87.88% - 00E VI: 7 230Vac 10% load 86.81% - 00E VI: 7 230Vac 10% load 85.39% CoC V5 tier 2: 75 230Vac 10% load 85.82% CoC V5 tier 2: 75 Load regulation - ±2.19% - Tested at boa Line regulation - ±0.28% - 0full load and ful Startup time - 18.6ms - 85V/6 EMC Test EMC Test EMC Test Contact 8kV - - EFT test 2kV - - ±5kHz/1 Conduction EMI 110V 6dB margin - - ENS5						
	lest	Contact	8kV	-	-	@100Ω concrete resistor
	EFT test		2kV	-	-	±5kHz/100kHz
	Surge Tes	st	1kV	-	-	Differential mode, 20hm, 1.2/50us
EFT te Surge T		110V	6dB margin	-	-	FCC Part 15 Class B
Conduction EMI		230V	6dB margin	-	-	EN55022
			Pr	otection Functions		
	SCP test		-	-		ОК
		-	-	-	ОК	
	OLP test		-	8.2V	-	OK
	OTP test		135°C	150°C	165°C	OK(IC internal Temp)

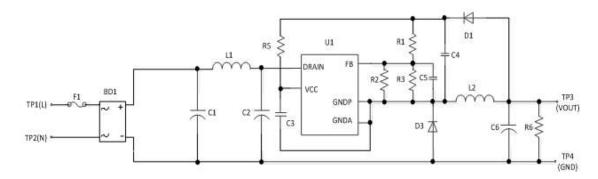
2.2 Environment

Operation temperature:	-20°C~85°C
Operation Humidity:	20%~90% R.H.
Storage temperature:	0~40°C
Storage Humidity:	0%~95% R.H.



Chapter 3. Schematic and Bill of Material

3.1 Schematic



3.2 Bill of Material

Figure 3: Evaluation Board Schematic

ltown	Designation	Paperintian		0	Manufaatuuru
Items	Designator	Description	Footprint	Qty.	Manufacturer
1	F1	3.15A/300V; Fuse	8*4*8mm	1	OAHE
2	BD1	ABS10A	SOPA-4	1	Diodes
3	C1, C2	10uF/400V, Electrolytic capacitor	Ф10*13mm	2	Rubycon
4	C3	2.2µF/25V, X7R	SMD 0805	1	Murata
5	C4	1μF/50V, X7R	SMD 1206	1	Murata
6	C5	1.5nF/50V, X7R	SMD 0805	1	Murata
7	C6	220µF/35V, Electrolytic capacitor	Ф8*12mm	1	Rubycon
8	D1	RS1MSWF; Fast type diode	SOD123F	1	Diodes
9	D3	STTH2R06S; Fast diode, 2A/600V	SMC	1	ST
10	L1	220μH; Inductor, 0.96Ω, 0.5A	DIP, Φ5*8mm	1	Wurth
11	L2	470μH; Inductor, 0.47Ω, 1.15A	DIP, Ф10*15mm	1	Wurth
12	R1	100kΩ	SMD 0805, 1%	1	Yageo
13	R2	16.2kΩ	SMD 0805, 1%	1	Yageo
14	R3	300.1kΩ	SMD 0805, 1%	1	Yageo
15	R5	5.1kΩ	SMD 0805, 5%	1	Yageo
16	R6	68kΩ	SMD 0805, 5%	1	Yageo
17	U1	AP3928	SO-8	1	Diodes
	Total		18pcs		

Table 1: Bill of Material



Chapter 4. The Evaluation Board Connections

4.1 PCB Layout

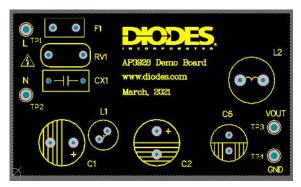


Figure 4: PCB Board Layout Top View

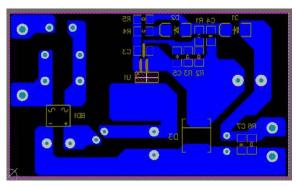


Figure 5: PCB Board Layout Bottom View

4.2 Circuit Description

4.2.1 Input EMI Filtering

The input stage is composed of fusible resistor F1, rectifier bridge DB1, filtering inductor L1, Capacitors C1 and C2. Resistor F1 is a flame proof, fusible, wire-wound resistor. It limits inrush current to safe levels for input rectifier diodes, provides differential mode noise reduction and acts as an input fuse in the event of short circuit.

4.2.2 Control IC

AP3928 co-packages a 700V power MOSFET and control circuitry into a cost-effective SO-8 package. The device is self-starting from the Drain pin with local supply decoupling provided by a small capacitor C3 (at least 100nF) connected to the BP pin when AC source is applied.

4.2.3 Output Rectification

During the ON time of U1, current ramps in L2 and is simultaneously delivered to the load. During the OFF time the inductor current ramps down via the free-wheeling diode D3, feedback diode D1, and the load. Diode D3 should be an ultra-fast diodes (Trr<50ns or lower). Capacitor C3 should be selected to have an adequate ripple margin (low ESR type).

4.2.4 Output Feedback

The voltage across L2 is rectified by C4 and D1 during the off-time of U1. For forward voltage drop of D1 and D3 is approximately equal, the voltage across C4 tracks the output voltage. To provide a feedback signal, the voltage across C4 is divided by R1 and R2//R3. This voltage is specified for U1 at FB pin (2.5V). This allows the simple feedback to meet the required overall output tolerance of ±5% at rated output current.

4.3 Quick Start Guide

- 1. The evaluation board is preset at 18V/550mA from output.
- 2. Ensure that the AC source is switched OFF or disconnected before doing connection.
- 3. Connect the AC line wires of power supply to "L" & "N" connectors on the left side of the board.
- 4. Turn on the AC main switch.
- 5. Measure "+V" & "GND" connectors to ensure correct output voltage, 18V.

CAUTION: This EV board is non-isolated. Do not touch anywhere there are electrical connections because they are all coupled to high voltage potential.



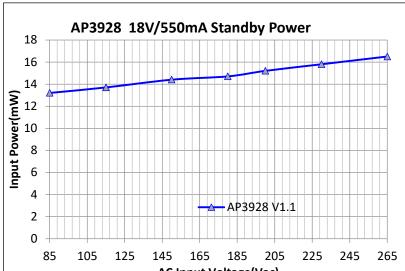
Chapter 5. System Test

5.1 Input & Output Characteristics

5.1.1 Input Standby Power

Standby power and output voltage is measured after 10-minute aging. The voltage data is tested at the PCB terminal. All data is tested at ambient temperature.

Table 2: Standby Power and Output Voltage @ no load								
AC input Voltage	Pin (mW)	Vo (V)						
85V/60Hz	13.2	19.025						
115V/60Hz	13.7	19.015						
230V/50Hz	15.8	19.006						
265V/50Hz	16.5	18.999						



AC Input Voltage(Vac)

Figure 6: Standby Power versus Vin Curve

5.1.2 Efficiency

The efficiency data is measured after 10-minute aging, and it is tested at the PCB terminal. All the data is tested at ambient temperature.



			Table 3: Conv	version Efficiency	/		
AC input voltage	Items	10%	25%	50%	75%	100%	Avg. Eff.
	Vo (V)	18.603	18.537	18.514	18.513	18.502	
	lo (mA)	55	137.5	275	412.5	550	00.049/
115V/60Hz	Pin (W)	1.0231	2.5488	5.0913	7.6366	10.1761	86.81%
	Efficiency (%)	87.88%	87.24%	87.39%	86.54%	86.07%	
	Vo (V)	18.565	18.513	18.491	18.492	18.488	
0001//5011	lo (mA)	55	137.5	275	412.5	550	05.00%
230V/50Hz	Pin (W)	1.0211	2.5455	5.0851	7.6279	10.1684	85.82%
	Efficiency (%)	85.39%	85.04%	85.47%	86.56%	86.24%	

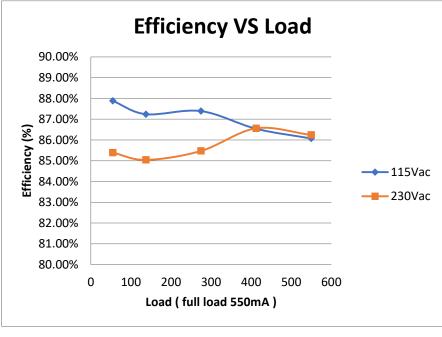


Figure 7: Efficiency versus Loading Curve

1.4.1

5.1.3 Line and Load Regulation

The line and load regulation data is measured after 10-minute aging. The voltage data is tested at the PCB terminal. All the data is tested at ambient temperature.



Table 4: Line and Load Regulation Data

AC input voltage	Loading(mA)								
AC input voltage	0	50	100	150	200	250	300		
85Vac/60Hz	19.215	18.654	18.572	18.532	18.524	18.516	18.512		
115Vac/60Hz	19.206	18.603	18.569	18.537	18.526	18.518	18.514		
230Vac/50Hz	19.312	18.565	18.538	18.513	18.504	18.496	18.495		
265Vac/50Hz	19.315	18.556	18.530	18.512	18.505	18.501	18.498		
Line Regulation	±0.28%	±0.26%	±0.11%	±0.08%	±0.06%	±0.06%	±0.05%		
			Load	CV					
AC input voltage	350	400	450	500	550	Regulation	Regulation		
85Vac/60Hz	18.503	18.494	18.489	18.485	18.483	±1.94%			
115Vac/60Hz	18.513	18.511	18.509	18.506	18.502	±1.87%			
230Vac/50Hz	18.493	18.492	18.491	18.489	18.488	±2.18%	±4.05%		
265Vac/50Hz	18.495	18.493	18.491	18.488	18.487	±2.19%			
Line Regulation	±0.05%	±0.05%	±0.06%	±0.06%	±0.05%	-			

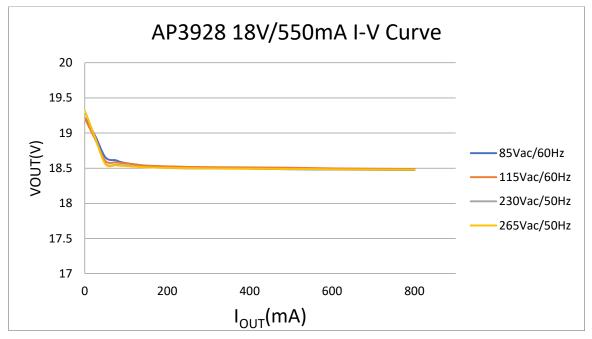


Figure 8: Output Voltage versus Loading Curve



5.2 Key Performance Test

5.2.1 Start-up Performance

The start-up time is measured with a differential probe across AC inputs, "L" and "N" connectors and a common low-voltage probe across output terminals, "+V" and "GND" connectors. Before starting up, buck capacitors should be discharged.

AC input voltage	Loading	Figures	
AC input voltage	No load	Full load	Figures
85Vac/60Hz	10.5ms	18.6ms	Fig. 9, Fig. 10
115Vac/60Hz	10.4ms	17.9ms	-
230Vac/50Hz	10.2ms	16.5ms	-
265Vac/50Hz	10.1ms	16.1ms	Fig. 11, Fig. 12

Table 5: Start-up Performance

CH2:Vin; CH4:Vo

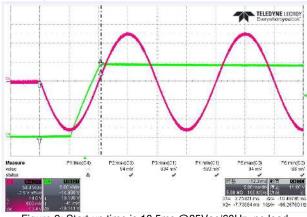


Figure 9: Start up time is 10.5ms @85Vac/60Hz, no load

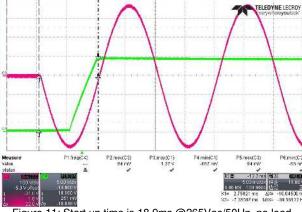


Figure 11: Start up time is 18.9ms @265Vac/50Hz, no load

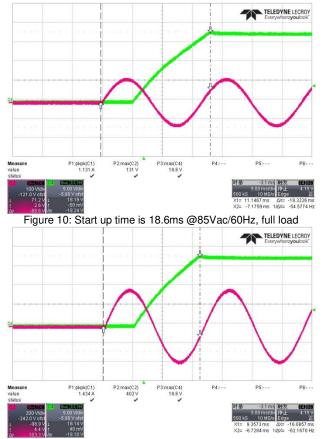


Figure 12: Start up time is 29.4ms @265Vac/50Hz, full load

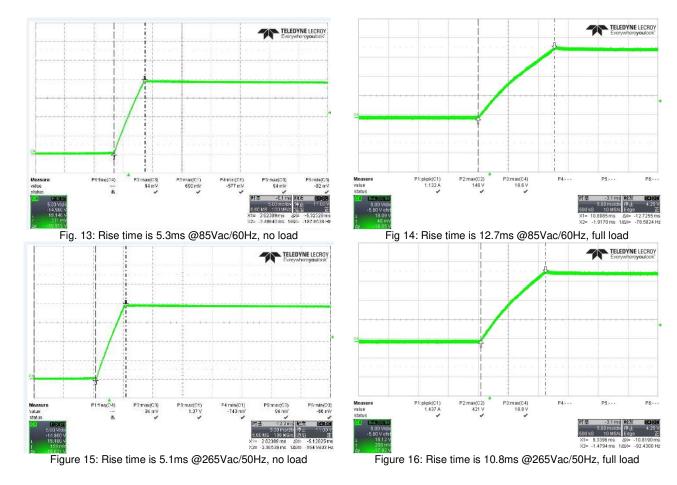


5.2.2 Rise Time

The rise time is measured with a common low-voltage probe across output terminals, "+V" and "GND" connectors. Before starting up, output capacitors should be discharged.

Table 6: Rise Time

	Loading c	Figureo	
AC input voltage	No load	Full load	Figures
85Vac/60Hz	5.3ms	12.7ms	Fig. 13, Fig.14
115Vac/50Hz	5.3ms	12.4ms	-
230Vac/50Hz	5.1ms	11.2ms	-
265Vac/50Hz	5.1ms	10.8ms	Fig. 15, Fig.16





5.2.3 Voltage Stress

The voltage is measured between the "Drain" and "S" pins of AP3928. The test needs differential probes.

Table 7:	Internal MOSFET	Drain-Source	Voltage Stress
rubic 7.		Drain Obuloc	Voltage Offess

ſ		Loading	Figureo	
	AC input voltage	No load	Full load	Figures
	85Vac/60Hz	139V	155V	Fig. 17, Fig 18
	115Vac/60Hz	184V	197V	-
	230Vac/50Hz	358V	364V	-
	265Vac/50Hz	396V	438V	Fig. 19, Fig. 20

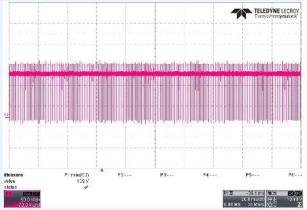
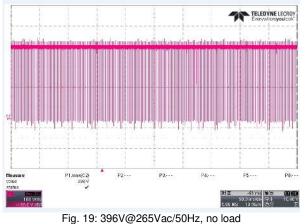


Figure 17: 139V@85Vac/60Hz, no load



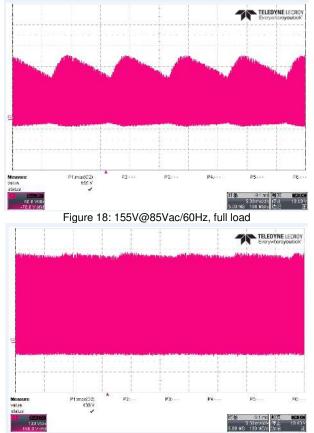


Fig. 20: 438V@265Vac/50Hz, full load



5.2.4 Output Ripple & Noise

The ripple and noise is tested at PCB terminal, using 10:1 probe without probe cap and ground clip. The bandwidth is limited to 20MHz. A 10µF electrolytic capacitor and a 100nF ceramic capacitor should be paralleled to the output terminal.

					L	oading co	onditions				F :	_	
AC	input volta	ge	No load				Full load			Figures			
8	35Vac/60Hz			15.	4mV			57.6mV		F	ig. 21, Fi	g.22	
115Vac/60Hz				25.	5mV			56.9mV			-	9	
230Vac/50Hz			27.	8mV			55.2mV			-			
2	65Vac/50Hz	<u>.</u>		29.	7mV			55.7mV		Fi	ig. 23, Fig	g. 24	
			Ť		TELE Every	DYNE LECROY whereyoulook					4	TELEDY Everywit	YNE LECR
					1955 - 30 4957 - 9	1. 19.3 (9.3)	19. al ales a						
Maletterholy	nitale estimation de state de	diseasily, doi -) aildon		a kan taki a kati a		iniu dhatati hulu	-						
								AAAAA	-	AAAA	-	-	
						((13) (a) (c)							
			Ť.							i.			
sure e	P1:pkpk(C4) 15.4 mV	P2	P3:	P4:	P5:	P6:	Measure value	P1:pkpk(C4) 57.6 mV	P2:max(C4) 23.0 mV	P3:min(C4) -34.6 mV	P4:	P5:	E
EwE ACTM 20.0 mV/dw 0 00 mV ofst Figu	ure 21: Outp	ut R&N, 15	5.4mV@)Hz, no lo	維友 CELED 停止 82.0 mV Edge 正 Dad, DYNE LECROY	20.0 mV/div 0.00 mV ofst Fig	jure 22: Out	tput R&N,	57.6mV@8	500 x	160 µs 2.00 ms/div 5 25 MS/s Hz, full I TELEDY Everywf	
		1 (2 X 2) ((2 X 2)											
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1 K 453 K	400 0 100 0 X 10			ACD 13 14 COC 54	******	6 7. J. 100			1072-01 (R. 194-19)			12.2.2	
sure e	P1:pkpk(C4) 23.7 mV	P2:	P3:	P4:	P5:	P6:	Measure value status	P1:pkpk(C4) 55.7 mV	P2:max(C4) 20.5 mV	P3:min(C4) -35.2 mV	P4:	P5:	F
IS	1				†恭 0.00 s	触发 区回	CA BACACIM	•			时基	80 us At	5 余

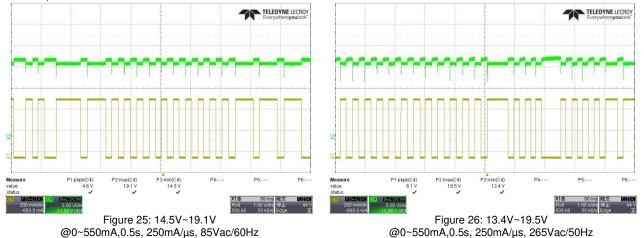


5.2.5 Dynamic Response

The dynamic response of output voltage is tested at the PCB terminal and the bandwidth is limited to 20MHz. Loading is set 0A as low load and 550mA as high load. Besides, the period is 2 seconds and the ramp is set at 250mA/µs.

Table 9: Dynamic Response				
	Output	voltage		
AC input voltage	Max Vo(V)	Min Vo(V)	Figures	
85Vac/60Hz	19.1	14.5	Fig. 25	
115Vac/60Hz	19.2	14.6	-	
230Vac/50Hz	19.4	13.9	-	
265Vac/50Hz	19.5	13.4	Fig. 26	

CH1: lo; CH4: Vo





5.3 Protection Test

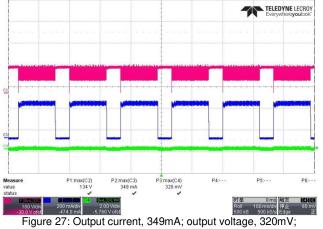
5.3.1 Short Circuit Protection (SCP) Test

The SCP test is measured under the condition that output cable terminals are shorted. The cable end short resistance value used is 50mΩ.

AC input voltage	Max Vo (mV)	Max lo(mA)	Vds(V)	Average input power (W)	Figures
85Vac/60Hz	320	349	134	0.480	Fig. 27
115Vac/60Hz	320	364	179	0.698	-
230Vac/50Hz	448	694	352	0.442	-
265Vac/50Hz	448	777	404	0.234	Fig. 28

	.	.		
Table 10	: Short	Circuit	Protection	Test

CH2: Vds; CH3 :lo; CH4: Vo



Vds is 134V@output is shorted@85Vac/60Hz

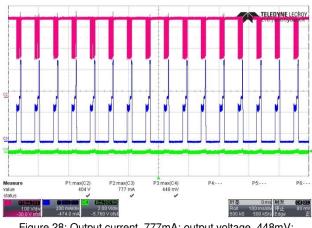


Figure 28: Output current, 777mA; output voltage, 448mV; Vds is 404V@output is shorted@265Vac/50Hz

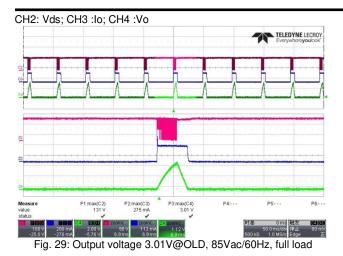
5.3.2 Open Loop Detection (OLD) Protection Test

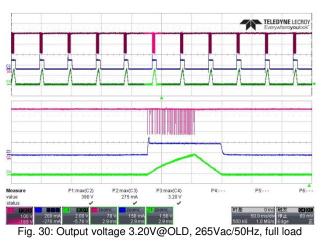
The open loop detection protection is measured when FB pin is connected to Source pin.

Table 11: Open Loop Detection	on Test
-------------------------------	---------

AC input voltage	The peak of output voltage(V)	Figures
85Vac/60Hz	3.01	Fig. 29
115Vac/60Hz	3.07	-
230Vac/50Hz	3.20	-
265Vac/50Hz	3.20	Fig. 30







5.3.3 Overload Protection (OLP) Test

The overload protection point is tested as below: increase the loading by 10mA/step until the system cannot maintain a stable output, and then mark the loading level as over load protection point.

Table 12: Overload Protection Point test

AC input voltage	Overload protection point(mA)
85Vac/60Hz	750
115Vac/60Hz	750
230Vac/50Hz	750
265Vac/50Hz	750

5.4 Thermal Test

The thermal test is under ambient temperature after 1-hour aging. The board has no case in open frame. Thermal imager is used to observe the surface temperature of AP3928.

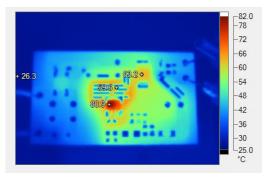


Figure 31: AP3928, 80.9°C, D2 63.2°C @85Vac/60Hz, full load, ambient temperature, 25°C.

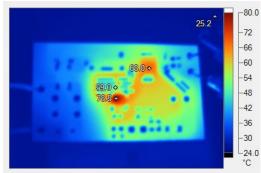


Figure 32: AP3928, 78.5°C, D2 68°C @ 265Vac/50Hz, full load, ambient temperature, 25°C.

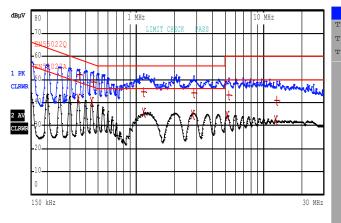


5.5 System EMI Scan

The power supply meets EN55022 Class B (for 110Vac input and 230Vac input) EMI requirements with more than 6dB margin.

5.5.1 Conducted EMI Test of 230V@full load

The test result can pass EN55022 Class B limit with more than 6dB margin.



		EDIT	PEAK	LIST (F	rinal		Results)
Crao	cel:		EN550	22Q			
Ira	ce2:		EN550	22A			
frad	ce3:						
	TRAC	CE	F	REQUENCY	Y	LEVEL dBµV	DELTA
2	Avera	je	346.0	08411600	6 kHz	42.00	-7.0
1	Quasi	Peak	352.9	63180679	9 kHz	52.13	-6.7
2	Avera	je	443.7	32257589	9 kHz	40.40	-6.5
1	Quasi	Peak	457.1	7778872	6 kHz	48.98	-7.7
2	Avera	je	1.130	65507633	l MHz	35.60	-10.3
1	Quasi	Peak	1.141	96162708	8 MHz	44.82	-11.1
2	Avera	je	2.768	55896362	2 MHz	34.99	-11.0
1	Quasi	Peak	2.824	20699879	9 MHz	44.41	-11.5
2	Avera	je	5.182	0348060	7 MHz	34.53	-15.4
1	Quasi	Peak	5.339	05564273	3 MHz	43.29	-16.7
2	Avera	je	12.43	8878293	6 MHz	32.46	-17.5
1	Quasi	Peak	12.68	88997473	3 MHz	41.04	-18.9

Fig. 33, L line conducted waveform@230Vac/50Hz, full load.

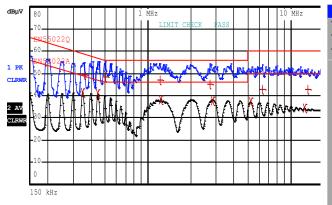


Figure 35: N line conducted waveform@230Vac/50Hz, full load.

Fig. 34, L line conducted data@230Vac/50Hz, full load.

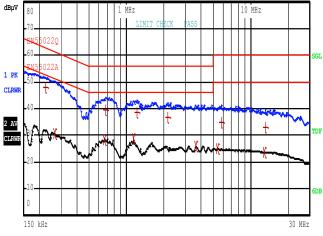
EDIT	PEAK LIST (Final	Measurement	Results)
cel:	EN55022Q			
ce2:	EN55022A			
ce3:				
TRACE	FREQUENC	Y	LEVEL dBµV	DELT
Average	346.00841160	6 kH2	41.41	-7.4
Quasi Peak	356.49281248	6 kHz	49.42	-9.3
Average	443.73225758	9 kHz	40.96	-6.0
Quasi Peak	500.00861452	8 kHz	48.48	-7.5
Quasi Peak	1.2122152783	6 MHz	46.81	-9.1
Average	1.2243374311	4 MHz	38.36	-7.4
Quasi Peak	2.7140074145	9 MHz	45.33	-10.4
Average	2.8242069987	9 MHz	37.87	-8.1
Average	5.2338551541	3 MHz	37.17	-12.8
Quasi Peak	6.3230672570	3 MHz	42.74	-17.2
Average	12.438878293	6 MHz	34.19	-15.8
Quasi Peak	13.073386098	5 MHz	42.97	-17.0
	cel: ce2: ce3: TRACE Average Quasi Peak Average Quasi Peak Average Quasi Peak Average Average Quasi Peak Average	Cel: EN55022Q ce2: EN55022A ce3: TRACE FREQUENC Average 346.00841160 Quasi Peak 356.49281248 Average 443.73225758 Quasi Peak 500.00861452 Quasi Peak 1.2122152783 Average 1.2243374311 Quasi Peak 2.7140074145 Average 2.8242069987 Average 5.2338551541 Quasi Peak 6.3230672570 Average 12.438878293	cel: EN55022Q ce2: EN55022A ce3: TRACE FREQUENCY Average 346.008411606 kH: Quasi Peak 356.492812486 kH: Average 443.732257589 kH: Quasi Peak 500.008614528 kH: Quasi Peak 1.21221527836 MH: Average 1.22433743114 MH: Quasi Peak 2.71400741459 MH: Average 5.23385515413 MH: Quasi Peak 6.32306725703 MH: Average 12.4388782936 MH:	EN55022A Ce3: EN5502A TRACE FREQUENCY LEVEL dBµV Average 346.008411606 kHr 41.41 Quasi Peak 356.492812486 kHr 49.42 Average 443.732257589 kHr 40.96 Quasi Peak 500.008614528 kHr 48.48 Quasi Peak 1.21221527836 MHr 46.81 Average 1.22433743114 MHr 38.36 Quasi Peak 2.71400741459 MHr 45.33 Average 2.82420699879 MHr 37.87 Average 5.23385515413 MHr 37.17 Quasi Peak 6.32306725703 MHr 42.74 Average 12.4388782936 MHr 34.19

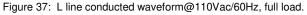
Figure 36: N line conducted data@230Vac/50Hz, full load.

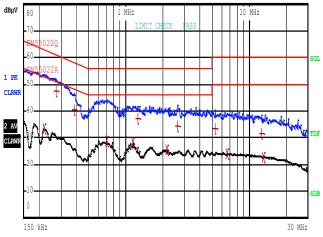


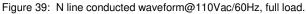
5.5.2 Conducted EMI Test of 110V@full load

The test result can pass EN55022 Class B limit with more than 6dB margin.









Tra	cel:	EN55022Q			
Tra	ice2:	EN55022A			
Tra	ice3:				
	TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB	
1	Quasi Peak	221.118376275 kHz	47.97	-14.80	
2	Average	264.49018761 kHz	30.76	-20.52	
2	Average	660.656865747 kHz	28.35	-17.64	
1	Quasi Peak	673.936068749 kHz	39.44	-16.56	
2	Average	1.13065507631 MHz	28.56	-17.43	
1	Quasi Peak	1.21221527836 MHz	38.78	-17.21	
1	Quasi Peak	2.1374603093 MHz	36.76	-19.23	
2	Average	3.6218534158 MHz	25.73	-20.26	
2	Average	5.39244619915 MHz	24.87	-25.12	
1	Quasi Peak	5.83924652649 MHz	34.64	-25.35	
2	Average	12.8157887448 MHz	23.83	-26.16	
1	Quasi Peak	13.0733860985 MHz	33.12	-26.87	

Figure 38: L line conducted data@110Vac/60Hz, full load.

	EDI	T PEAK LIST (Final	Measurement Resul	ts)	
Tra	cel:	EN55022Q			
Tra	ice2:	EN55022A			
Tra	ice3:				
	TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB	
2	Average	216.761470714 kHz	33.49	-19.44	
1	Quasi Peak	272.504504785 kHz	47.46	-13.57	
1	Quasi Peak	382.208547038 kHz	40.61	-17.61	
2	Average	694.357005568 kHz	28.86	-17.13	
2	Average	1.13065507631 MHz	28.30	-17.69	
1	Quasi Peak	1.2489466135 MHz	37.25	-18.74	
2	Average	2.1374603093 MHz	25.31	-20.68	
1	Quasi Peak	2.634188858 MHz	34.41	-21.58	
1	Quasi Peak	5.28619370567 MHz	33.38	-26.62	
2	Average	6.57980914316 MHz	24.15	-25.84	
1	Quasi Peak	12.5632670765 MHz	31.55	-28.44	
2	Average	12.9439466322 MHz	22.89	-27.11	
Figure 40: Niling conducted date@110\(co/60Hz, full load					

Figure 40: N line conducted data@110Vac/60Hz, full load.



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