

MC74LCX244

Octal Buffer, Non-Inverting, Low Voltage, 3-State

The MC74LCX244 is a high performance, non-inverting octal buffer operating from a 2.3 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX244 inputs to be safely driven from 5 V devices. The MC74LCX244 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs. The Output Enable (OE) input, when HIGH, disables the output by placing them in a HIGH Z condition.

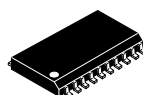
Features

- Designed for 2.3 to 5.5 V V_{CC} Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
 - ◆ Human Body Model >2000 V
 - ◆ Machine Model >200 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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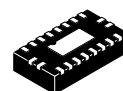
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SOIC-20 WB
DW SUFFIX
CASE 751D

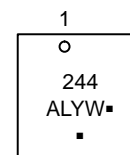
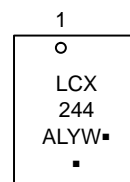
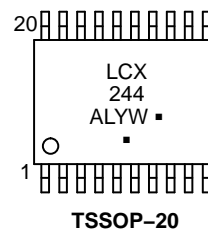
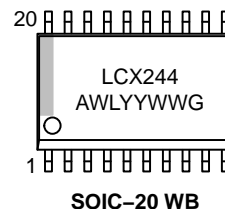


TSSOP-20
DT SUFFIX
CASE 948E



QFN20
MN SUFFIX
CASES 485AA
& 485CB

MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74LCX244

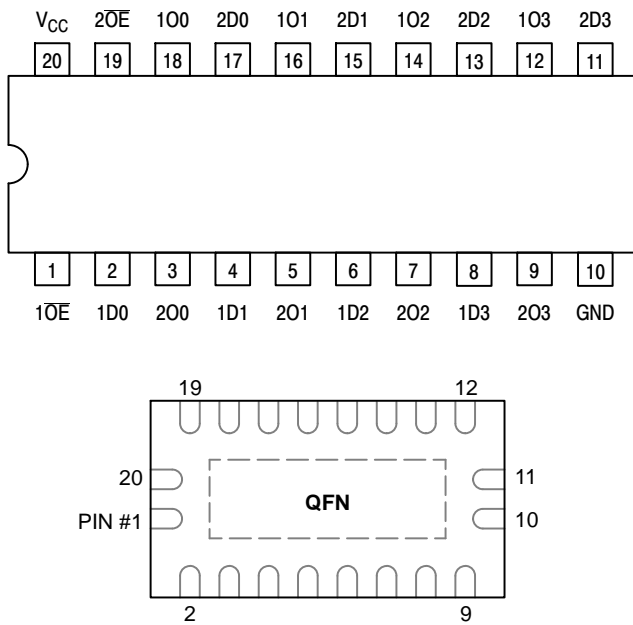


Figure 1. Pinouts: 20-Lead (Top View)

PIN NAMES

| PINS | FUNCTION |
|------------------|----------------------|
| $n\overline{OE}$ | Output Enable Inputs |
| 1Dn, 2Dn | Data Inputs |
| 1On, 2On | 3-State Outputs |

TRUTH TABLE

| INPUTS | | OUTPUTS |
|--------------------------------------|------------|----------|
| $1\overline{OE}$ $2\overline{OE}$ | 1Dn 2Dn | 1On, 2On |
| L | L | L |
| L | H | H |
| H | X | Z |

H = High Voltage Level
 L = Low Voltage Level
 Z = High Impedance State
 X = High or Low Voltage Level and Transitions are Acceptable
 For I_{CC} reasons, DO NOT FLOAT Inputs

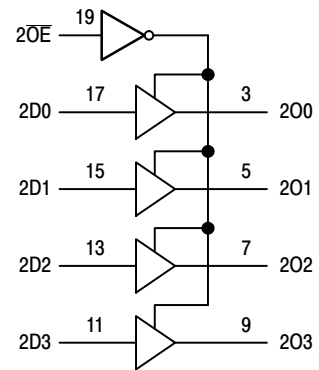
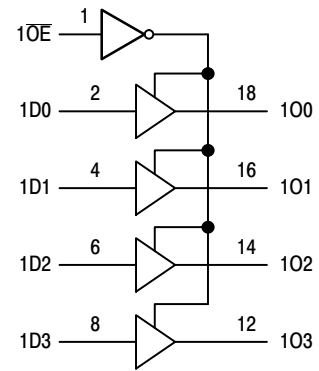


Figure 2. Logic Diagram

MC74LCX244

MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Units |
|---------------|---|-----------------------------------|--------------------------------------|-------|
| V_{CC} | DC Supply Voltage | -0.5 to +7.0 | | V |
| V_I | DC Input Voltage | $-0.5 \leq V_I \leq +7.0$ | | V |
| V_O | DC Output Voltage | $-0.5 \leq V_O \leq +7.0$ | Output in 3-State | V |
| | | $-0.5 \leq V_O \leq V_{CC} + 0.5$ | Output in HIGH or LOW State (Note 1) | V |
| I_{IK} | DC Input Diode Current | -50 | $V_I < GND$ | mA |
| I_{OK} | DC Output Diode Current | -50 | $V_O < GND$ | mA |
| | | +50 | $V_O > V_{CC}$ | mA |
| I_O | DC Output Source/Sink Current | ± 50 | | mA |
| I_{CC} | DC Supply Current Per Supply Pin | ± 100 | | mA |
| I_{GND} | DC Ground Current Per Ground Pin | ± 100 | | mA |
| T_{STG} | Storage Temperature Range | -65 to +150 | | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | $T_L = 260$ | | °C |
| T_J | Junction Temperature Under Bias | $T_J = 150$ | | °C |
| θ_{JA} | Thermal Resistance (Note 2) | $\theta_{JA} = 140$ | | °C/W |
| MSL | Moisture Sensitivity | | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|---------------------|---|-----|----------|----------|-------|
| V_{CC} | Supply Voltage Operating Data Retention Only | 2.0 | 2.5, 3.3 | 5.5 | V |
| | | 1.5 | 2.5, 3.3 | 5.5 | |
| V_I | Input Voltage | 0 | | 5.5 | V |
| V_O | Output Voltage HIGH or LOW State 3-State | 0 | | V_{CC} | V |
| | | 0 | | 5.5 | |
| I_{OH} | HIGH Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ | | | -24 | mA |
| | | | | -12 | |
| I_{OL} | LOW Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ | | | 24 | mA |
| | | | | 12 | |
| T_A | Operating Free-Air Temperature | -55 | | +125 | °C |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, $V_{CC} = 3.0\text{ V}$ | 0 | | 10 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74LCX244

DC ELECTRICAL CHARACTERISTICS

| Symbol | Characteristic | Condition | T _A = -55°C to +125°C | | Units |
|------------------|---------------------------------------|--|----------------------------------|------|-------|
| | | | Min | Max | |
| V _{IH} | HIGH Level Input Voltage (Note 3) | 2.3 V ≤ V _{CC} ≤ 2.7 V | 1.7 | | V |
| | | 2.7 V ≤ V _{CC} ≤ 3.6 V | 2.0 | | |
| V _{IL} | LOW Level Input Voltage (Note 3) | 2.3 V ≤ V _{CC} ≤ 2.7 V | | 0.7 | V |
| | | 2.7 V ≤ V _{CC} ≤ 3.6 V | | 0.8 | |
| V _{OH} | HIGH Level Output Voltage | 2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA | V _{CC} - 0.2 | | V |
| | | V _{CC} = 2.3 V; I _{OH} = -8 mA | 1.8 | | |
| | | V _{CC} = 2.7 V; I _{OH} = -12 mA | 2.2 | | |
| | | V _{CC} = 3.0 V; I _{OH} = -18 mA | 2.4 | | |
| | | V _{CC} = 3.0 V; I _{OH} = -24 mA | 2.2 | | |
| V _{OL} | LOW Level Output Voltage | 2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA | | 0.2 | V |
| | | V _{CC} = 2.3 V; I _{OL} = 8 mA | | 0.6 | |
| | | V _{CC} = 2.7 V; I _{OL} = 12 mA | | 0.4 | |
| | | V _{CC} = 3.0 V; I _{OL} = 16 mA | | 0.4 | |
| | | V _{CC} = 3.0 V; I _{OL} = 24 mA | | 0.55 | |
| I _{OZ} | 3-State Output Current | V _{CC} = 3.6 V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 0 to 5.5 V | | ±5 | μA |
| I _{OFF} | Power Off Leakage Current | V _{CC} = 0, V _{IN} = 5.5 V or V _{OUT} = 5.5 V | | 10 | μA |
| I _{IN} | Input Leakage Current | V _{CC} = 3.6 V, V _{IN} = 5.5 V or GND | | ±5 | μA |
| I _{CC} | Quiescent Supply Current | V _{CC} = 3.6 V, V _{IN} = 5.5 V or GND | | 10 | μA |
| ΔI _{CC} | Increase in I _{CC} per Input | 2.3 ≤ V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V | | 500 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS (t_R = t_F = 2.5 ns; R_L = 500 Ω)

| Symbol | Parameter | Waveform | Limits | | | | | | Units |
|--|--|----------|----------------------------------|-----|-------------------------|-----|-------------------------------|-----|-------|
| | | | T _A = -55°C to +125°C | | | | | | |
| | | | V _{CC} = 3.0 V to 3.6 V | | V _{CC} = 2.7 V | | V _{CC} = 2.5 V ± 0.2 | | |
| | | | C _L = 50 pF | | C _L = 50 pF | | C _L = 30 pF | | |
| | | | Min | Max | Min | Max | Min | Max | |
| t _{PLH} t _{PHL} | Propagation Delay Input to Output | 1 | 1.5 | 6.5 | 1.5 | 7.5 | 1.5 | 7.8 | ns |
| | | | 1.5 | 6.5 | 1.5 | 7.5 | 1.5 | 7.8 | |
| t _{PZH} t _{PZL} | Output Enable Time to High and Low Level | 2 | 1.5 | 8.0 | 1.5 | 9.0 | 1.5 | 10 | ns |
| | | | 1.5 | 8.0 | 1.5 | 9.0 | 1.5 | 10 | |
| t _{PHZ} t _{PLZ} | Output Disable Time From High and Low Level | 2 | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | ns |
| | | | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | |
| t _{OSHL} t _{OSLH} | Output-to-Output Skew (Note 4) | | | 1.0 | | | | | ns |
| | | | | 1.0 | | | | | |

4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

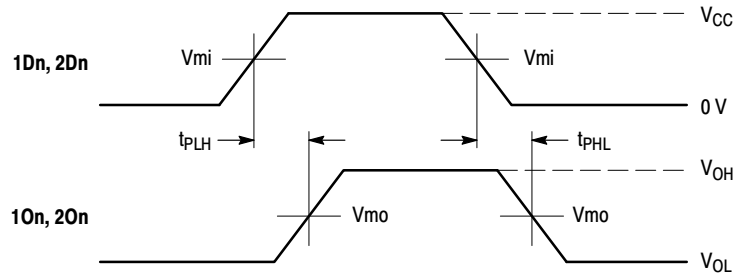
| Symbol | Characteristic | Condition | T _A = +25°C | | | Units |
|------------------|-------------------------------------|--|------------------------|--------------|-----|-------|
| | | | Min | Typ | Max | |
| V _{OLP} | Dynamic LOW Peak Voltage (Note 5) | V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V | | 0.8 0.6 | | V |
| V _{OLV} | Dynamic LOW Valley Voltage (Note 5) | V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V | | -0.8 -0.6 | | V |

5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

MC74LCX244

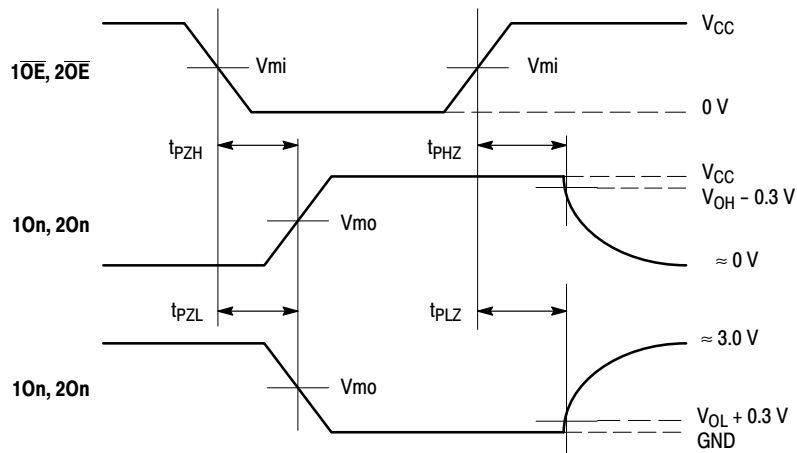
CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Units |
|-----------|-------------------------------|--|---------|-------|
| C_{IN} | Input Capacitance | $V_{CC} = 3.3\text{ V}$, $V_I = 0\text{ V}$ or V_{CC} | 7 | pF |
| C_{OUT} | Output Capacitance | $V_{CC} = 3.3\text{ V}$, $V_I = 0\text{ V}$ or V_{CC} | 8 | pF |
| C_{PD} | Power Dissipation Capacitance | 10 MHz, $V_{CC} = 3.3\text{ V}$, $V_I = 0\text{ V}$ or V_{CC} | 25 | pF |



WAVEFORM 1 – PROPAGATION DELAYS

$t_R = t_F = 2.5\text{ ns}$, 10% to 90%; $f = 1\text{ MHz}$; $t_W = 500\text{ ns}$



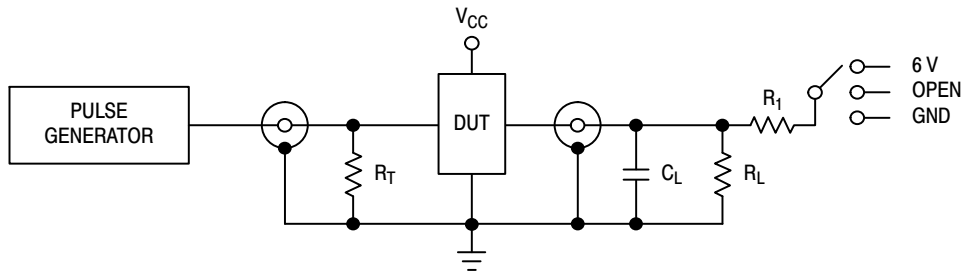
WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.5\text{ ns}$, 10% to 90%; $f = 1\text{ MHz}$; $t_W = 500\text{ ns}$

Figure 3. AC Waveforms

| Symbol | V_{CC} | | |
|----------|-------------------------|-------------------------|--------------------------|
| | 3.3 V \pm 0.3 V | 2.7 V | 2.5 V \pm 0.2 V |
| V_{mi} | 1.5 V | 1.5 V | $V_{CC}/2$ |
| V_{mo} | 1.5 V | 1.5 V | $V_{CC}/2$ |
| V_{HZ} | $V_{OL} + 0.3\text{ V}$ | $V_{OL} + 0.3\text{ V}$ | $V_{OL} + 0.15\text{ V}$ |
| V_{LZ} | $V_{OH} - 0.3\text{ V}$ | $V_{OH} - 0.3\text{ V}$ | $V_{OH} - 0.15\text{ V}$ |

MC74LCX244



| TEST | SWITCH |
|--|--|
| t_{PLH} , t_{PHL} | Open |
| t_{PZL} , t_{PLZ} | 6 V at $V_{CC} = 3.3 \pm 0.3$ V 6 V at $V_{CC} = 2.5 \pm 0.2$ V |
| Open Collector/Drain t_{PLH} and t_{PHL} | 6 V |
| t_{PZH} , t_{PHZ} | GND |

$C_L = 50$ pF at $V_{CC} = 3.3 \pm 0.3$ V or equivalent (includes jig and probe capacitance)
 $C_L = 30$ pF at $V_{CC} = 2.5 \pm 0.2$ V or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 500 \Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 4. Test Circuit

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-------------------|-----------------------------|-----------------------|
| MC74LCX244DWG | SOIC-20 WB (Pb-Free) | 38 Units / Rail |
| MC74LCX244DWR2G | SOIC-20 WB (Pb-Free) | 1000 / Tape & Reel |
| MC74LCX244DTG | TSSOP-20 (Pb-Free) | 75 Units / Rail |
| MC74LCX244DTR2G | TSSOP-20 (Pb-Free) | 2500 / Tape & Reel |
| NLV74LCX244DTR2G* | TSSOP-20 (Pb-Free) | 2500 / Tape & Reel |
| MC74LCX244MNTWG | QFN20, 2.5x4.5 (Pb-Free) | 3000 / Tape & Reel |
| MC74LCX244MN2TWG | QFN20, 2.5x3.5 (Pb-Free) | 3000 / Tape & Reel |

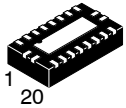
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

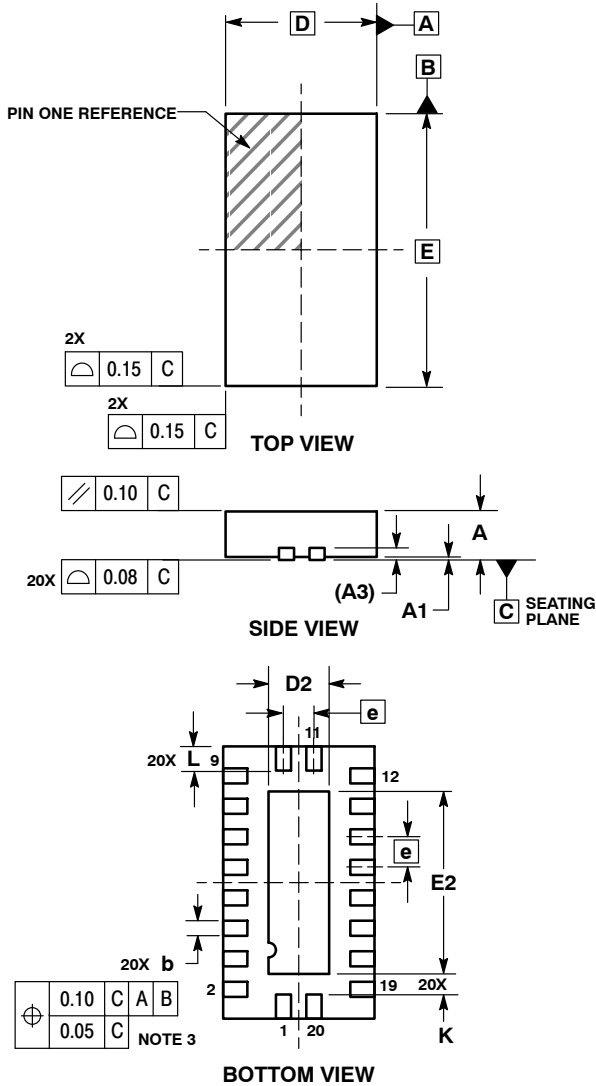
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SCALE 2:1

QFN20, 2.5x4.5 MM
CASE 485AA-01
ISSUE B

DATE 30 APR 2010

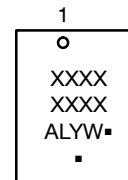


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.50 BSC | |
| D2 | 0.85 | 1.15 |
| E | 4.50 BSC | |
| E2 | 2.85 | 3.15 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

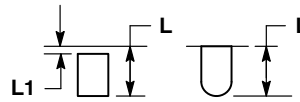
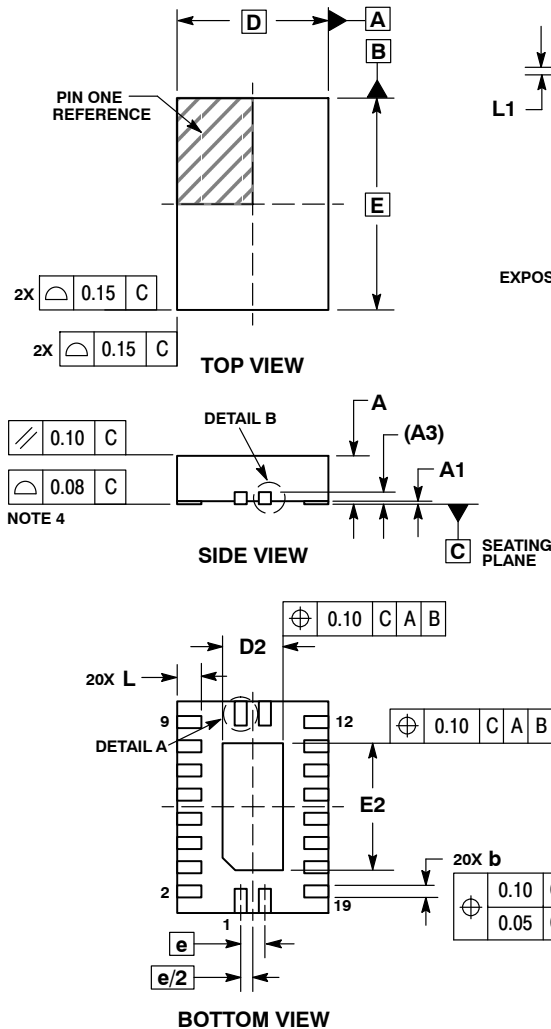
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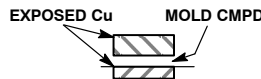
SCALE 2:1

QFN20, 2.5x3.5, 0.4P CASE 485CB ISSUE O

DATE 25 OCT 2011



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



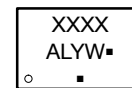
DETAIL B
ALTERNATE
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.15 | 0.25 |
| D | 2.50 BSC | |
| D2 | 0.90 | 1.10 |
| E | 3.50 BSC | |
| E2 | 2.00 | 2.20 |
| e | 0.40 BSC | |
| L | 0.35 | 0.45 |
| L1 | --- | 0.15 |

GENERIC MARKING DIAGRAM*

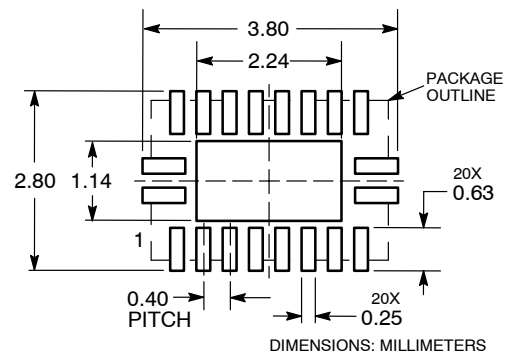


- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*

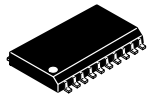


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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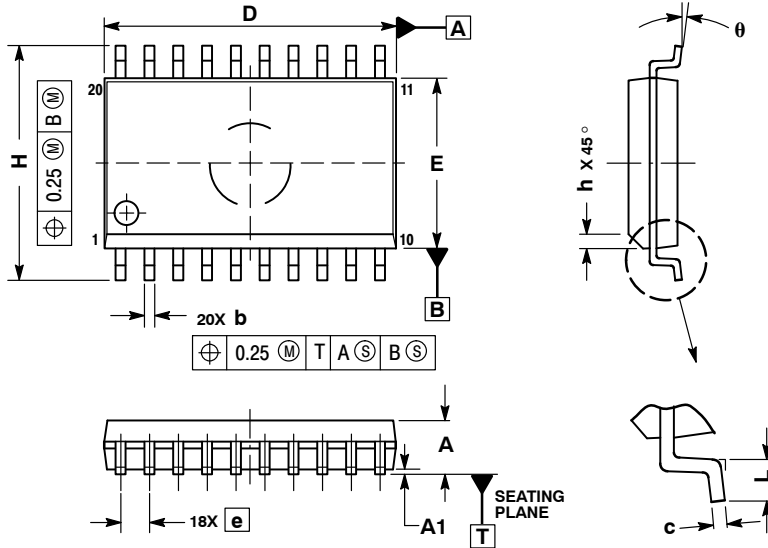
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

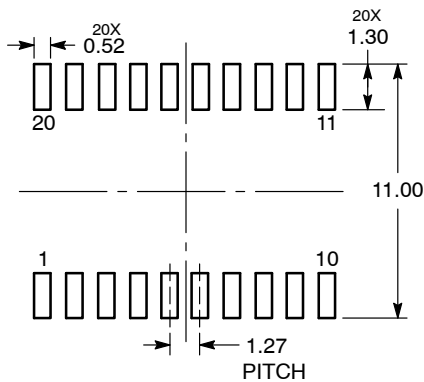


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

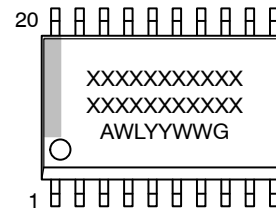
| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

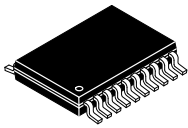
| | | |
|------------------|-------------|--|
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| DESCRIPTION: | SOIC-20 WB | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

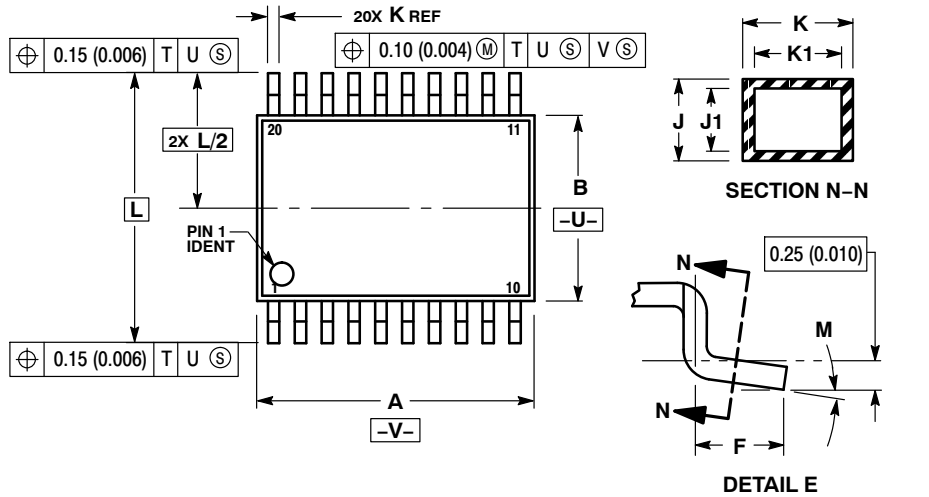
ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

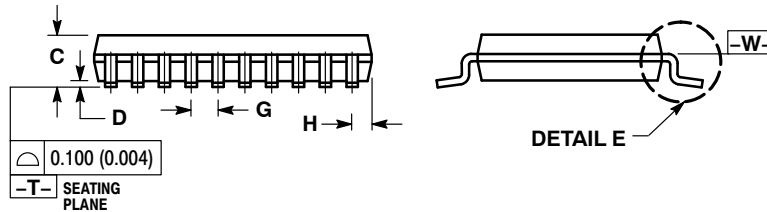
SCALE 2:1



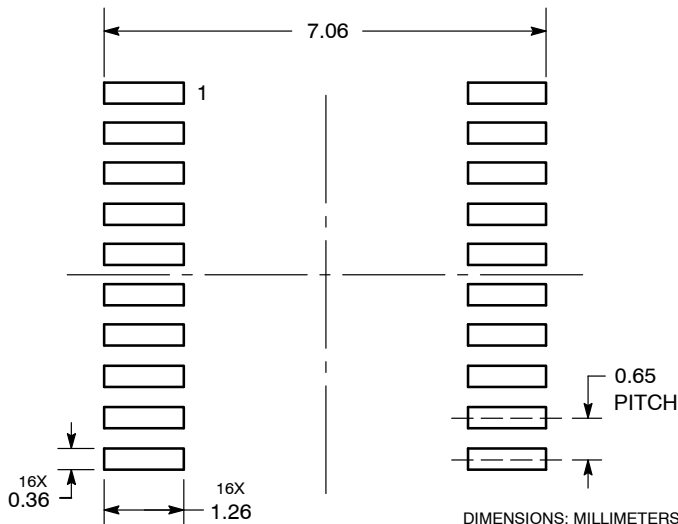
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

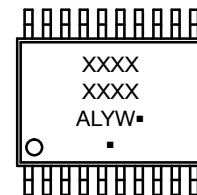
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|-------------|--|
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