

Fast-Charge Development System

Control of On-Board P-FET Switch-Mode Regulator

Features

- bq2004/E/H fast charge control evaluation and development
- ➤ Charge current sourced from an on-board switch-mode regulator (up to 3.0 A)
- ➤ Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast charge termination by delta temperature/delta time (ΔΤ/Δt), negative delta voltage (-ΔV) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- > -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- ➤ Programmable charge status display
- ➤ Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- ➤ Inhibit fast charge by logic-level input

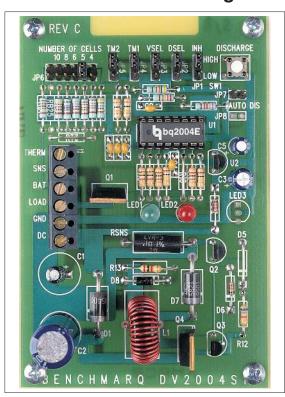
General Description

The DV2004S1/ES1/HS1 Development System provides a development environment for the bq2004/E/H Fast Charge IC. The DV2004S1/ES1/HS1 incorporates a bq2004/E/H and a buck-type switch-mode regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

The user provides a power supply and batteries. The user configures the DV2004S1/ES1/HS1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch S1.

Please review the bq2004/E/H data sheet before using the DV2004S1/ES1/HS1 board.



Connection Descriptions

J1

THERM	Thermistor connection
SNS tor	Negative battery terminal and thermis-
	connection
BAT+	Positive battery terminal and high side of discharge load
LOAD	Low side of discharge load
GND	Ground from charger supply
DC	DC input from charger supply

SLUU016A - 3/99 revised 8/2002 Rev. C Board

JP1 INH Inhibit input

JP2 DSEL Display select

JP3 VSEL Voltage termination select

JP4 TM1 TM1 setting
JP5 TM2 TM2 setting

JP6 NOC Select number of cells

JP7 Auto discharge-before-charge select

JP8 Auto cycle select

Fixed Configuration

The DV2004S1/ES1/HS1 board has the following fixed characteristics:

 $V_{\rm CC}~(4.75\text{--}5.25V)$ is regulated on-board from the supply at connector J1 DC.

LED1 and LED2 indicate charge status.

LED3 can replace LED1 and LED2 and provide an optional tri-color LED feature.

Charge initiates on the later application of the battery or DC, which provides $V_{\rm CC}$ to the bq2004/E/H.

Pin \overline{DCMD} may be tied to ground through JP7 for automatic discharge-before-charge. With JP7 open, a toggle of switch S1 momentarily pulls \overline{DCMD} low and initiates a discharge-before-charge. The bq2004E output activates FET Q1, allowing current to flow through an external current-limiting load between BAT+ and LOAD on connector J1.

As shipped from Benchmarq, the DV2004S1/ES1/HS1 buck-type switch-mode regulator is configured to a charging current of 2.25A. This current level is controlled by the value of sense resistor $R_{\rm SNS}$ by the relationship:

$$I_{\rm CHG} \ = \ \frac{0.225 V}{R_{\it SNS}}$$

The value of R_{SNS} at shipment is $0.100\Omega.$ This resistor can be changed depending on the application.

The suggested maximum $I_{\rm CHG}$ for the DV2004S1/ES1/HS1 board is 3A. The maximum cell voltage (MCV) setting is 1.8V.

Zener diode D5 is used to limit Q4 $V_{\rm GS}$ per a given DC voltage. The board is shipped with D5 shorted. The user can modify this Zener diode for the application. Refer to Table 1 for suggested D5 values for DC voltages.

Table 1. Lookup Table for D5 Selection

+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18-21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27-30	1N966A	16
30-32	1N967A	18
32–35	1N968A	20

Note:

Capacitors C2 and C3 must be changed from those shipped with the board for input voltage in excess of 24V.

With the provided NTC thermistor connected between THERM and SNS, values are: LTF = 0°C, HTF = 40°C, and TCO = 60°C. The $\Delta T/\Delta t$ settings at 30°C ($T_{\Delta T}$) are: minimum = 0.82°C/minute, typical = 1.10°C/minute.

The thermistor is identified by the serial number suffix as follows:

Identifier Thermistor			
K1	Keystone RL0703-5744-103-S1		
(blank)	Philips 2322-640-63103		
F1	Fenwal Type 16, 197-103LA6-A01		
01	Ozhumi 150-108-00(4)		
S1	Semetic 103AT-2		

Jumper-Selectable Configuration

The DV2004S1/ES1/HS1 must be configured as described below.

Jumper Setting	Pin State		
[12]3	Disabled (high)		
1[23]	Enabled (low)		

INH (**JP1**): Enables/disables charge inhibit (see bq2004/E/H data sheet).

Jumper Setting	Pin State		
[12]3	High		
1[23]	Low		
1 2 3	Float		

TM1 and TM2 (JP4 and JP5): Select fast charge safety time/hold-off/top-off (see bq2004/E/H data sheet).

Number of Cells (JP6): A resistor-divider network is

Closed Jumper	Number of Cells		
RB25	User-selectable		
RB24	10		
RB23	8		
RB22	6		
RB21	5		
RB20	4		

provided to select 4 to 10 cells (the resulting resistor value equals $\frac{N}{2}-1$ cells). RB1 is a 150K Ω resistor, and RB2 (RB20–RB25) is jumper-selected.

Temperature Disable: Connecting a $10 \text{K}\Omega$ resistor between THERM and SNS disables temperature control.

DSEL (JP2): Selects LED1 and LED2 (LED3 optional) display state (see bq2004E data sheet, Table 2, page 5).

VSEL (JP3): Selects $-\Delta V$ or peak-voltage detection, or disables voltage-based termination (see bq2004E data ssheet, page 7).

AUTO DIS SELECT (JP7): Jumping JP7 enables automatic discharge-before-charge.

AUTO CYCLE SELECT (JP8): Jumping JP8 automatically initiates a continuous discharge-before-charge/fast-charge cycling for data collection purposes.

Setup Procedure

- 1. Configure VSEL, TM1, TM2, DSEL, $\overline{INH},$ and number-of-cells (NOC) jumpers.
- 2. Connect the provided thermistor or a $10 \mathrm{K}\Omega$ resistor between THERM and SNS.
- 3. If using the discharge-before-charge or auto-cycle options, connect a current-limiting discharge load between BAT+ and LOAD.
- Attach the battery pack to BAT+ and SNS. For temperature control, the thermistor must contact the cells.
- 5. Attach DC current source to DC (+) and GND (-) connections in J1.

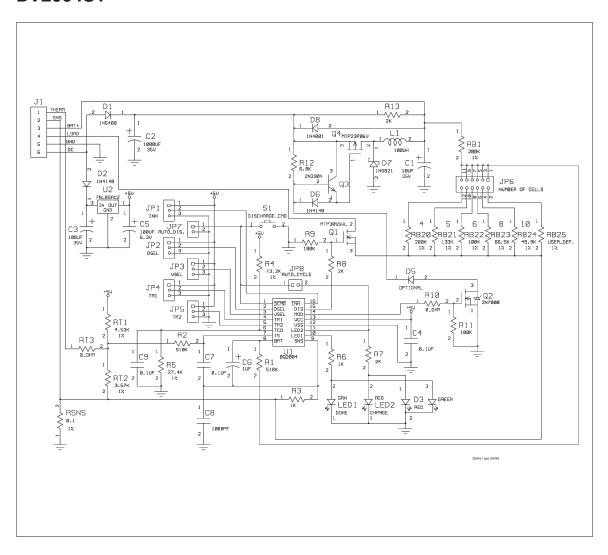
Recommended DC Operating Conditions

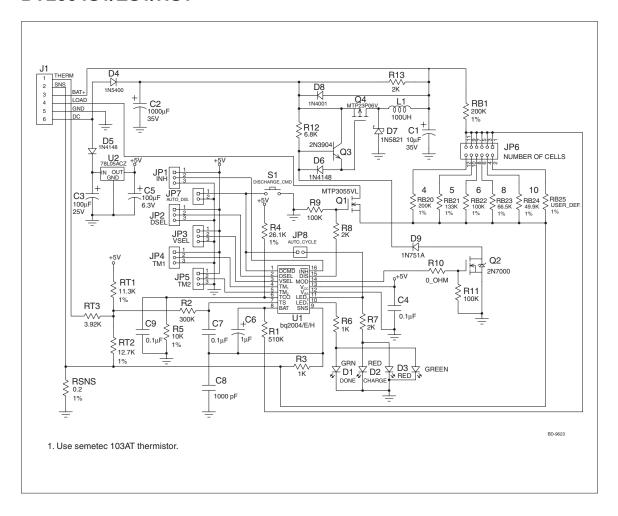
Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
I_{DC}	Maximum input current	-	-	2.4	A	
$V_{ m DC}$	Maximum input voltage	$\begin{array}{c} 2.0 + \mathrm{V_{BAT}} \\ \text{or } 15 \end{array}$	-	18 + V _{BAT} or 35	V	Note 1
V_{BAT}	BAT input voltage	-	-	24	V	
V_{THERM}	THERM input voltage	0	-	5	V	
I _{DSCHG}	Discharge load current	-	-	2	A	

Note:

1. The V_{DC+} limits consider the appropriate Zener diode at D5. The voltage at D5 is application-specific and limits the V_{GS} of Q4 to a safe enhancement value during Q4 conduction. See Table 1 for recommended D5 selections per V_{DC+} .

DV2004S1





IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated