

CSD18511KCS 40-V N-Channel NexFET™ Power MOSFET

1 Features

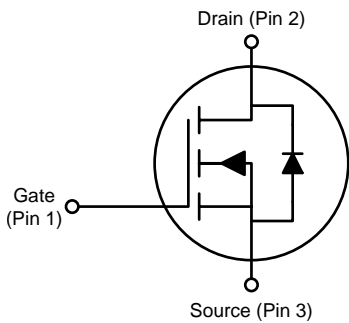
- Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 40-V, 2.1-m Ω , TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	40		V
Q_g	Gate Charge Total (10 V)	63.9		nC
Q_{gd}	Gate Charge Gate-to-Drain	9.7		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	3.2	m Ω
		$V_{GS} = 10\text{ V}$	2.1	
$V_{GS(th)}$	Threshold Voltage	1.8		V

Device Information⁽¹⁾

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD18511KCS	Tube	50	TO-220 Plastic Package	Tube

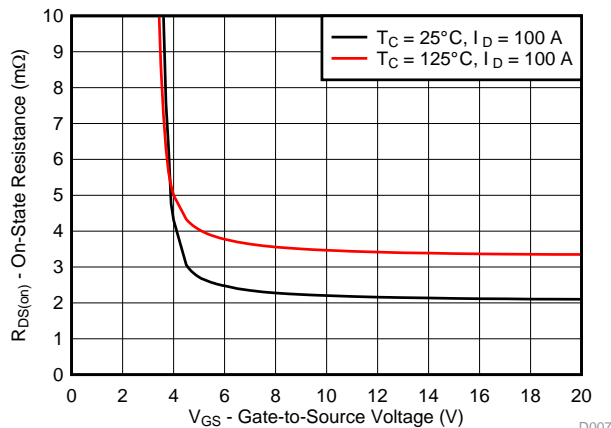
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package Limited)	110	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	194	
	Continuous Drain Current (Silicon Limited), $T_C = 100^\circ\text{C}$	137	
I_{DM}	Pulsed Drain Current ⁽¹⁾	400	A
P_D	Power Dissipation	188	W
T_J, T_{stg}	Operating Junction, Storage Temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche Energy, Single Pulse $I_D = 56\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	156	mJ

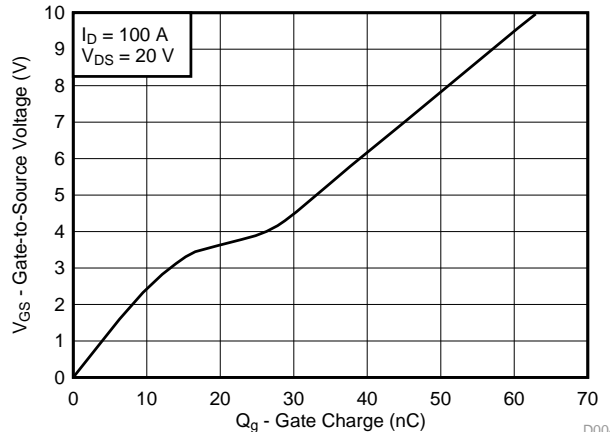
(1) Max $R_{\theta JC} = 0.8^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$.

$R_{DS(on)}$ vs V_{GS}



D007

Gate Charge



D004



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4 Revision History

DATE	REVISION	NOTES
July 2017	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 32\text{ V}$			1	μA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.5	1.8	2.4	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 100\text{ A}$		3.2	4.2	m Ω
		$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		2.1	2.6	
g_{fs}	Transconductance	$V_{DS} = 4\text{ V}, I_D = 100\text{ A}$		249		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$		4570	5940	pF
C_{oss}	Output capacitance			454	591	pF
C_{rss}	Reverse transfer capacitance			235	306	pF
R_G	Series gate resistance			0.9	1.8	Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 20\text{ V}, I_D = 100\text{ A}$		31		nC
Q_g	Gate charge total (10 V)			64		nC
Q_{gd}	Gate charge gate-to-drain			9.7		nC
Q_{gs}	Gate charge gate-to-source			17.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			7.4		nC
Q_{oss}	Output charge		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		20.7	
$t_{d(on)}$	Turnon delay time	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 100\text{ A}, R_G = 0\ \Omega$		8		ns
t_r	Rise time			6		ns
$t_{d(off)}$	Turnoff delay time			17		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 100\text{ A}, V_{GS} = 0\text{ V}$		0.9	1.0	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 20\text{ V}, I_F = 100\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		62		nC
t_{rr}	Reverse recovery time			31		ns

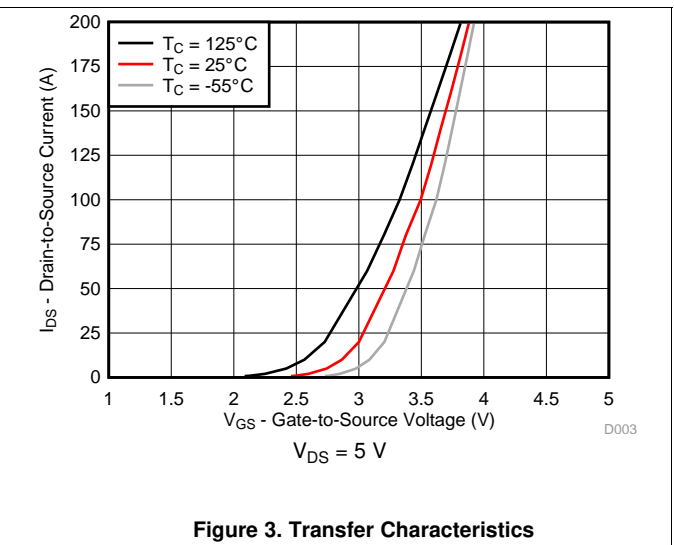
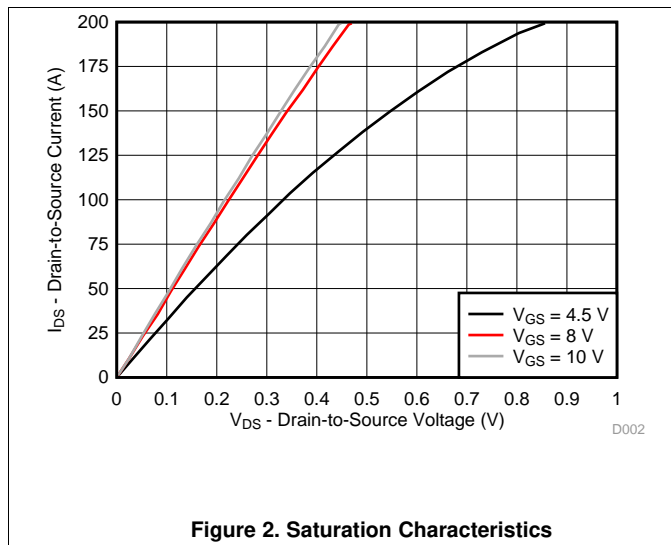
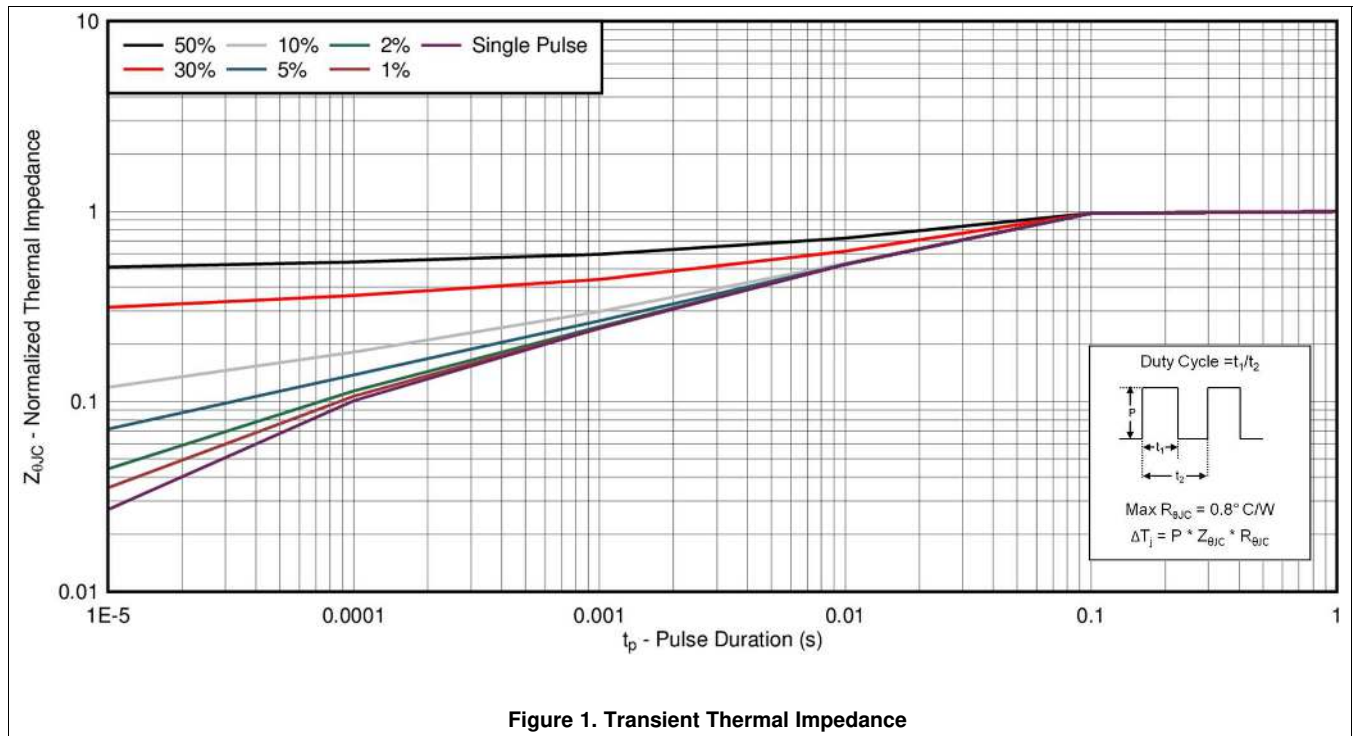
5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C}/\text{W}$

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)



Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

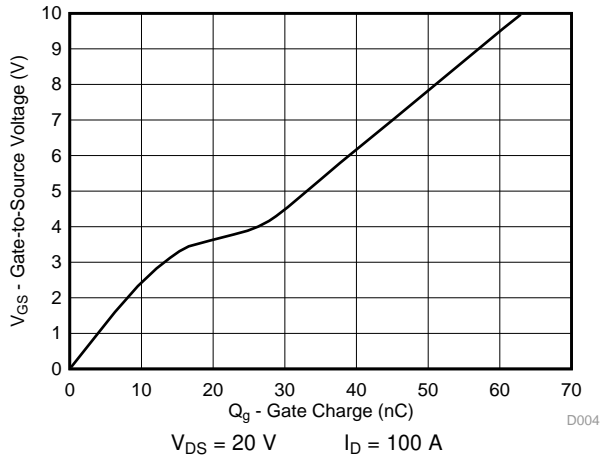


Figure 4. Gate Charge

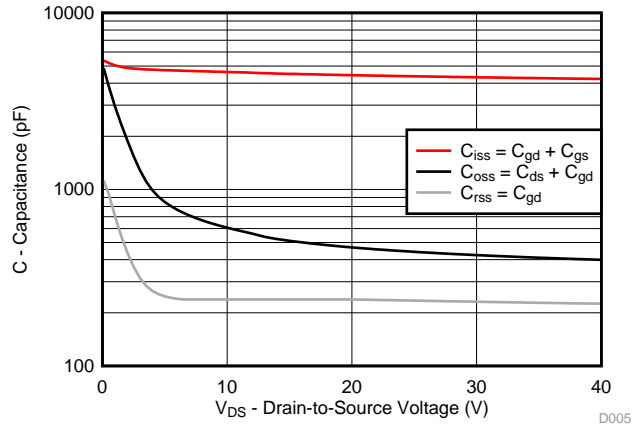


Figure 5. Capacitance

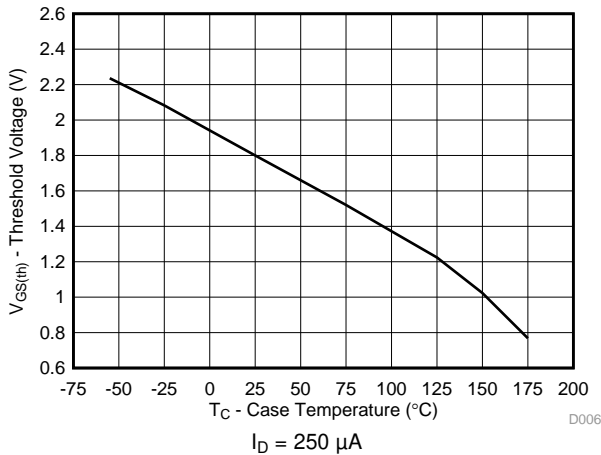


Figure 6. Threshold Voltage vs Temperature

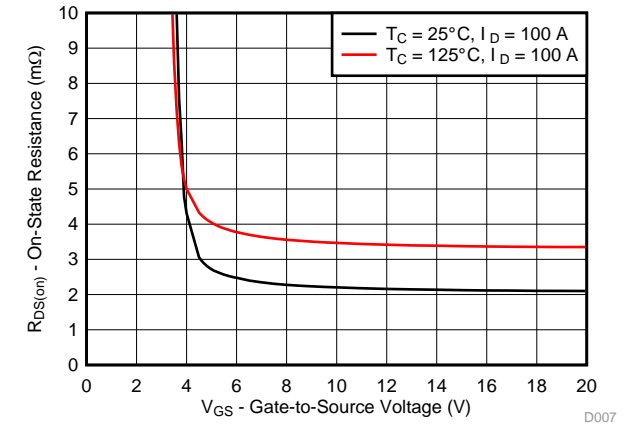


Figure 7. On-State Resistance vs Gate-to-Source Voltage

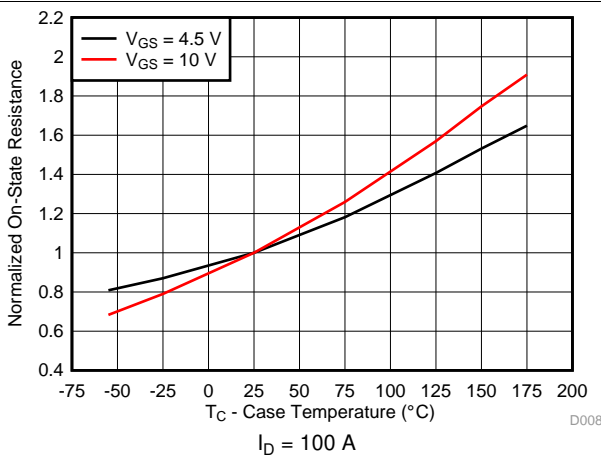


Figure 8. Normalized On-State Resistance vs Temperature

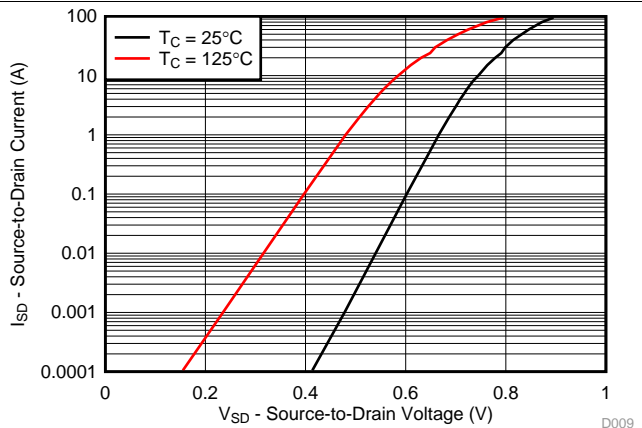
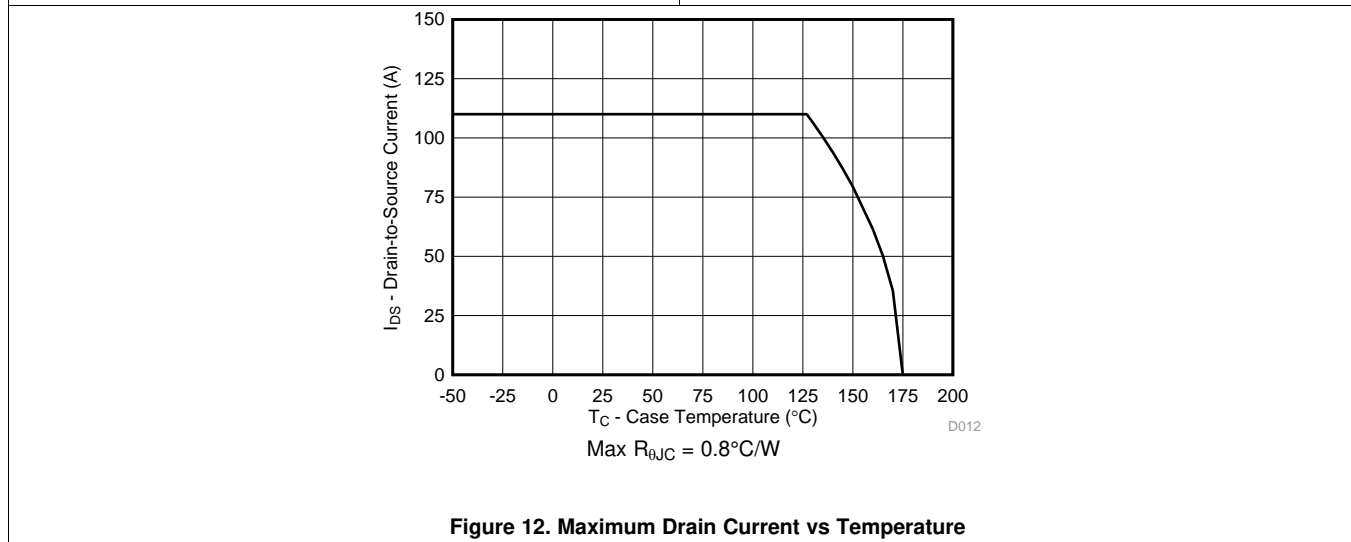
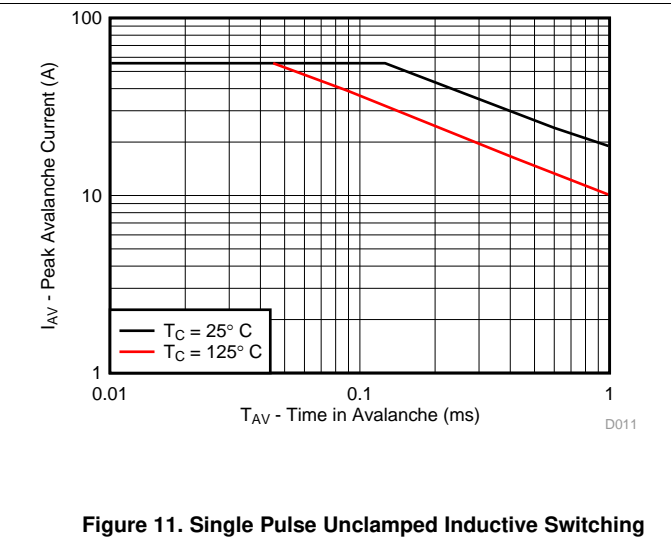
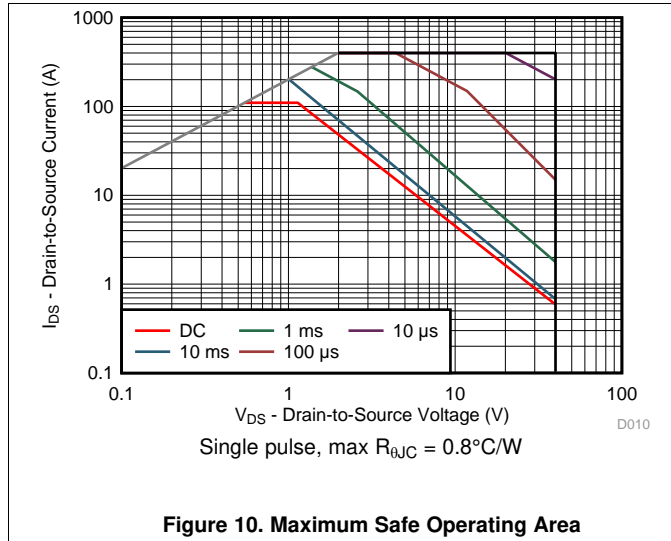


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)



6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
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6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

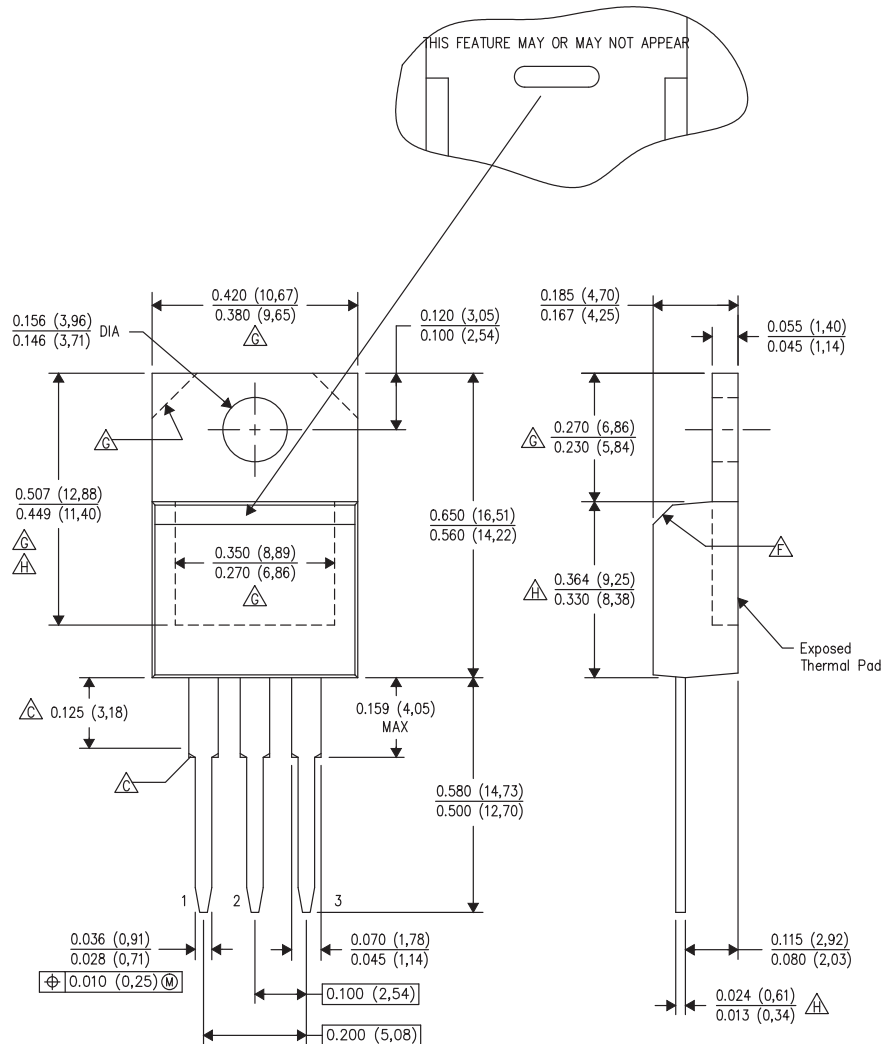
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions







- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Lead dimensions are not controlled within this area. Chamfer may or may not appear.
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 -  The chamfer is optional.
 -  Thermal pad contour optional within these dimensions.
 -  Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

Table 1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

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