

256K x 16 Static RAM

Features

- **High speed**
 - $t_{AA} = 12 \text{ ns}$
- **Low active power**
 - 612 mW (max.)
- **Low CMOS standby power (Commercial L version)**
 - 1.8 mW (max.)
- **2.0V Data Retention (660 μW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**

Functional Description

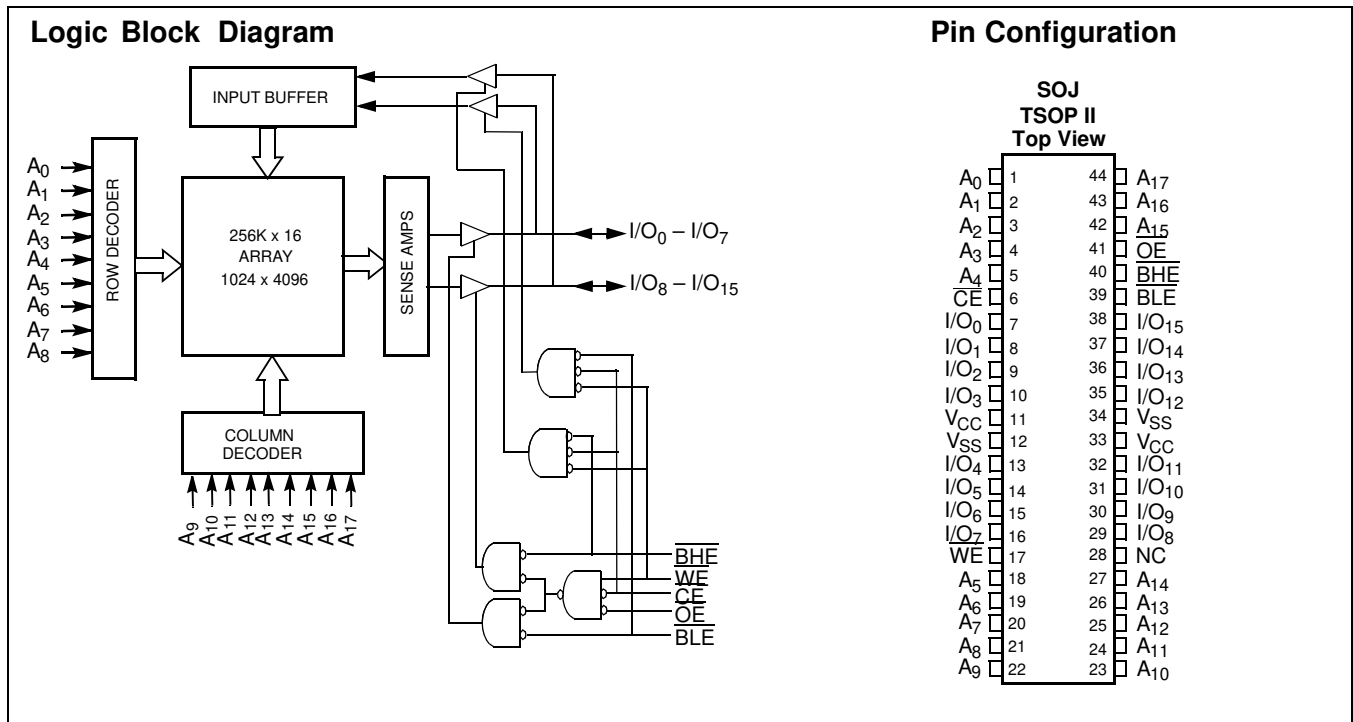
The CY7C1041BNV33 is a high-performance CMOS Static RAM organized as 262,144 words by 16 bits.

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), the BHE and $\overline{\text{BLE}}$ are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1041BNV33 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.



Selection Guide

			-12	-15
Maximum Access Time (ns)			12	15
Maximum Operating Current (mA)	Comm'l		190	170
	Ind'l		-	190
Maximum CMOS Standby Current (mA)	Com'l/Ind'l		8	8
	Com'l	L	0.5	0.5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V
 DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V
 Current into Outputs (LOW) 20 mA

Operating Range

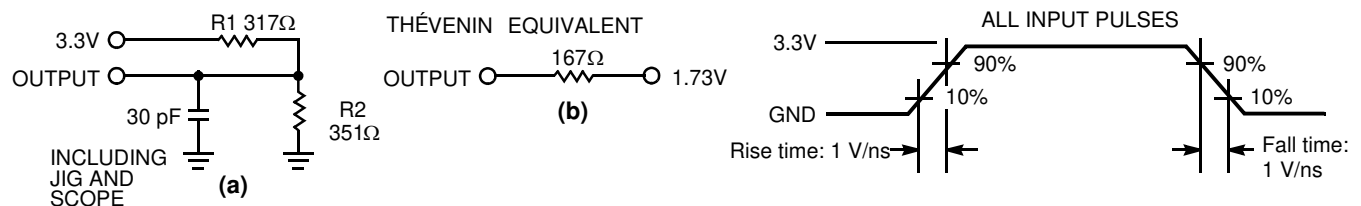
Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-12		-15		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.5	2.2	V _{CC} +0.5	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	mA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1	+1	-1	+1	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., f = f _{MAX} = 1/t _{RC}	Comm'l	190		170	mA
			Ind'l		-		190
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		40		40	mA
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	Com'l/Ind'l	8		8	mA
			Com'l L		0.5		0.5

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	8	pF
C _{OUT}	I/O Capacitance		8	pF

AC Test Loads and Waveforms

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[4] Over the Operating Range

Parameter	Description	-12		-15		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[5, 6]		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[5, 6]		6		7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		12		15	ns
t_{DBE}	Byte Enable to Data Valid		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		ns
t_{HZBE}	Byte Disable to High Z		6		7	ns
WRITE CYCLE^[7, 8]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	10		12		ns
t_{AW}	Address Set-Up to Write End	10		12		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	10		12		ns
t_{SD}	Data Set-Up to Write End	7		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[5, 6]		6		7	ns
t_{BW}	Byte Enable to End of Write	10		12		ns

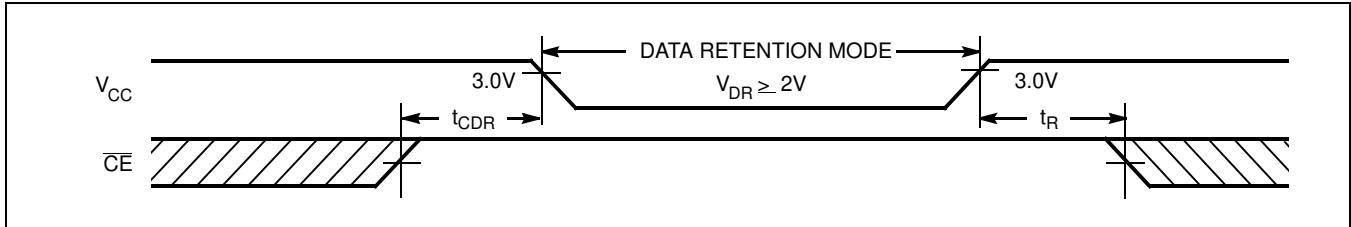
Data Retention Characteristics Over the Operating Range (For L version only)

Parameter	Description	Conditions ^[10]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V,$ $CE \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		330	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[9]}$	Operation Recovery Time		t_{RC}		ns

Notes:

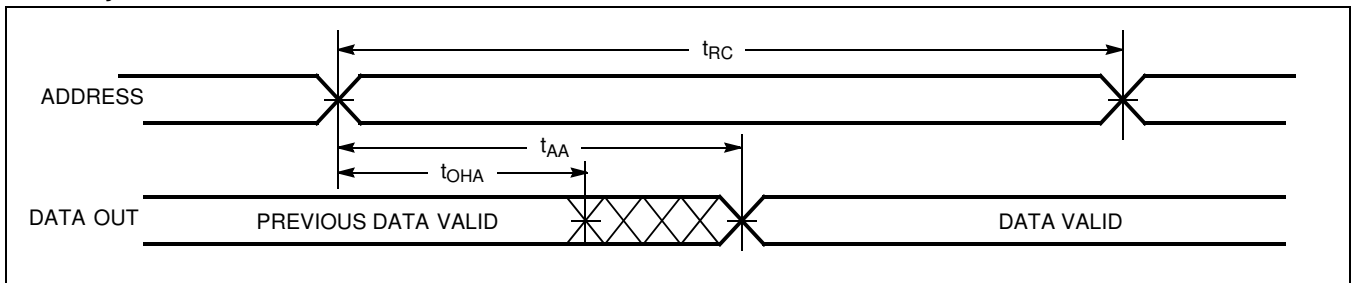
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .
- $t_r \leq 3$ ns for the -12 and -15 speeds.
- No input may exceed $V_{CC} + 0.5V$.

Data Retention Waveform

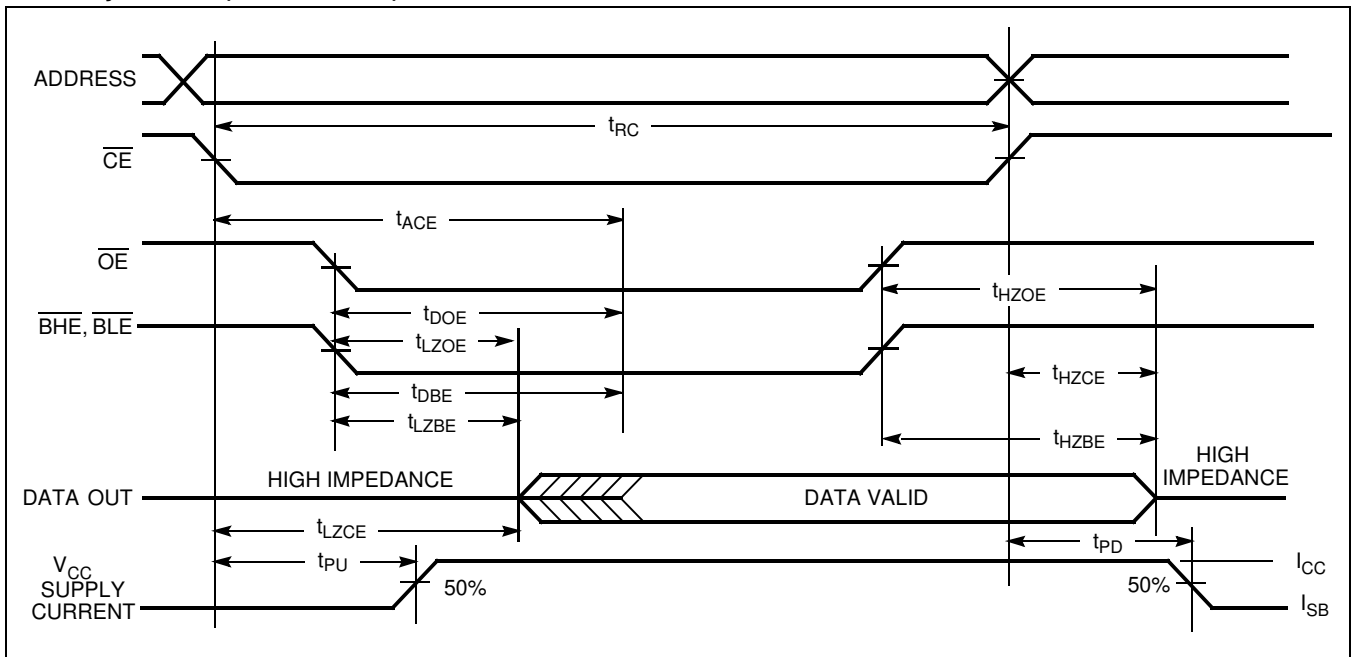


Switching Waveforms

Read Cycle No. 1^[11, 12]



Read Cycle No. 2 (OE Controlled)^[12, 13]

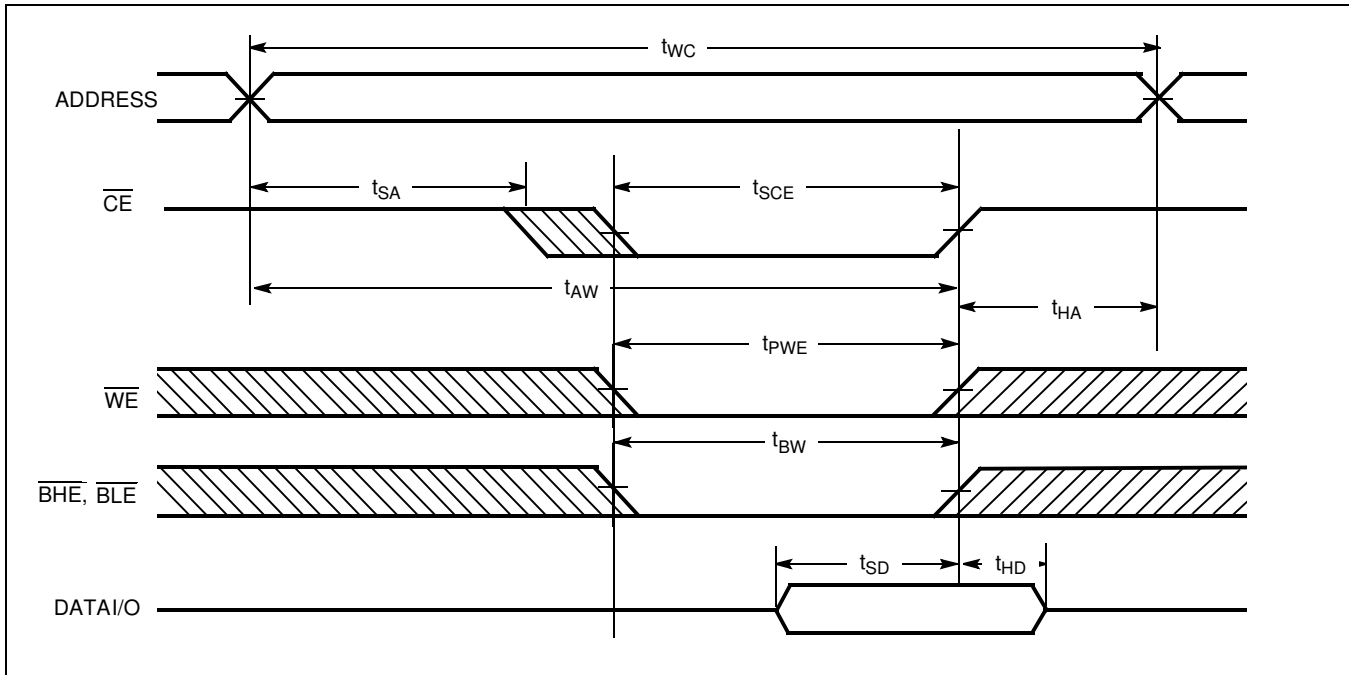


Notes:

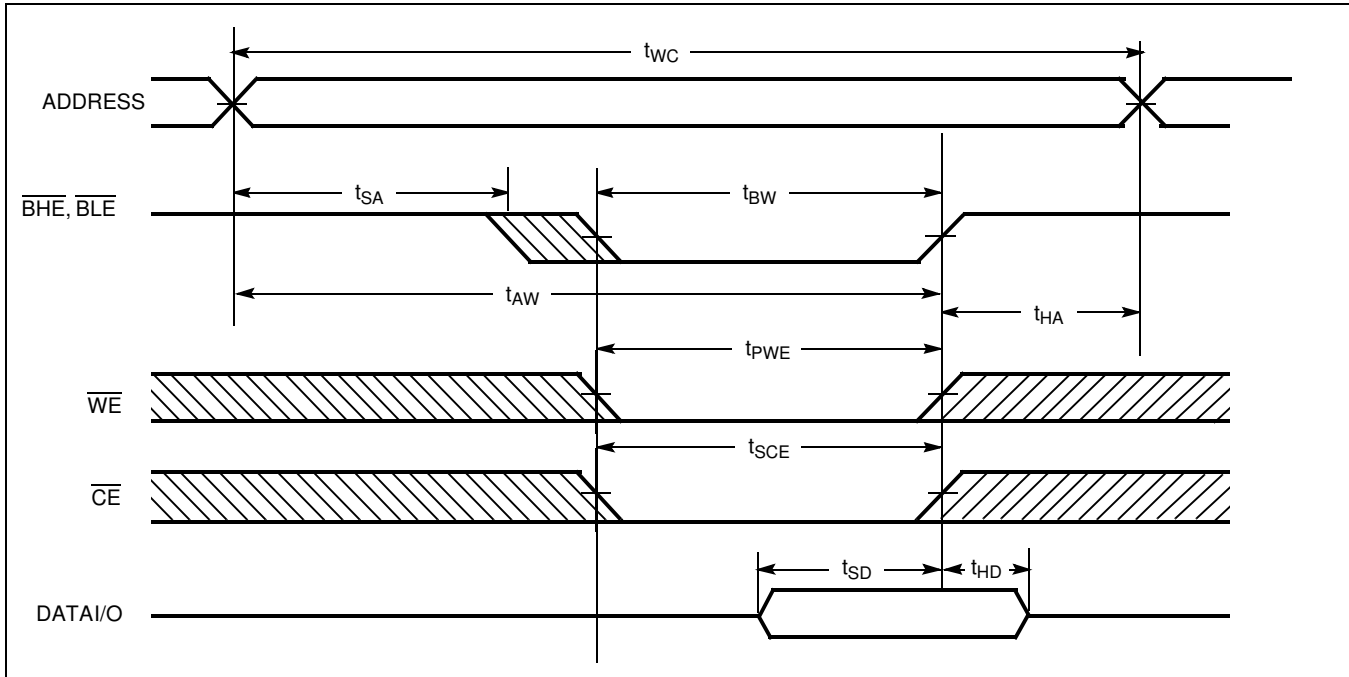
- 11. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
- 12. \overline{WE} is HIGH for read cycle.
- 13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{CE} Controlled)^[14, 15]



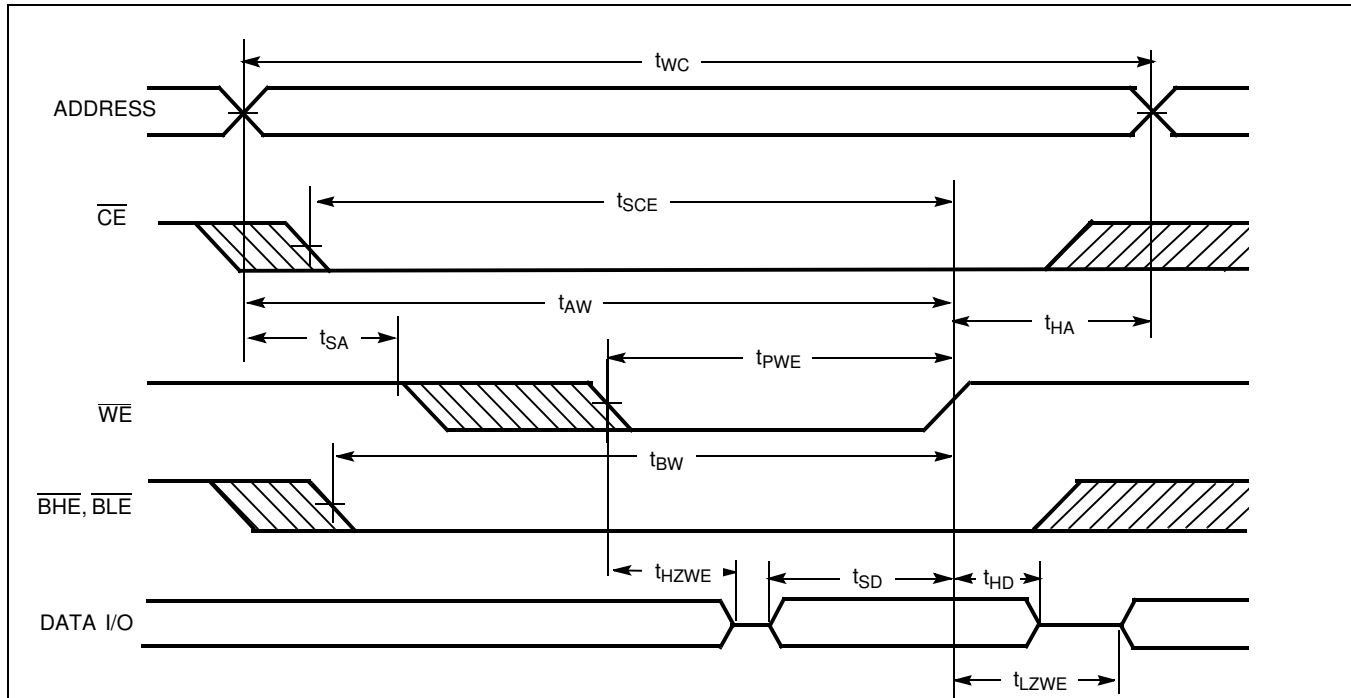
Write Cycle No. 2 (\overline{BLE} or \overline{BHE} Controlled)



Notes:

- 14. Data I/O is high-impedance if \overline{OE} or \overline{BHE} and/or $\overline{BLE} = V_{IH}$.
- 15. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)

Truth Table

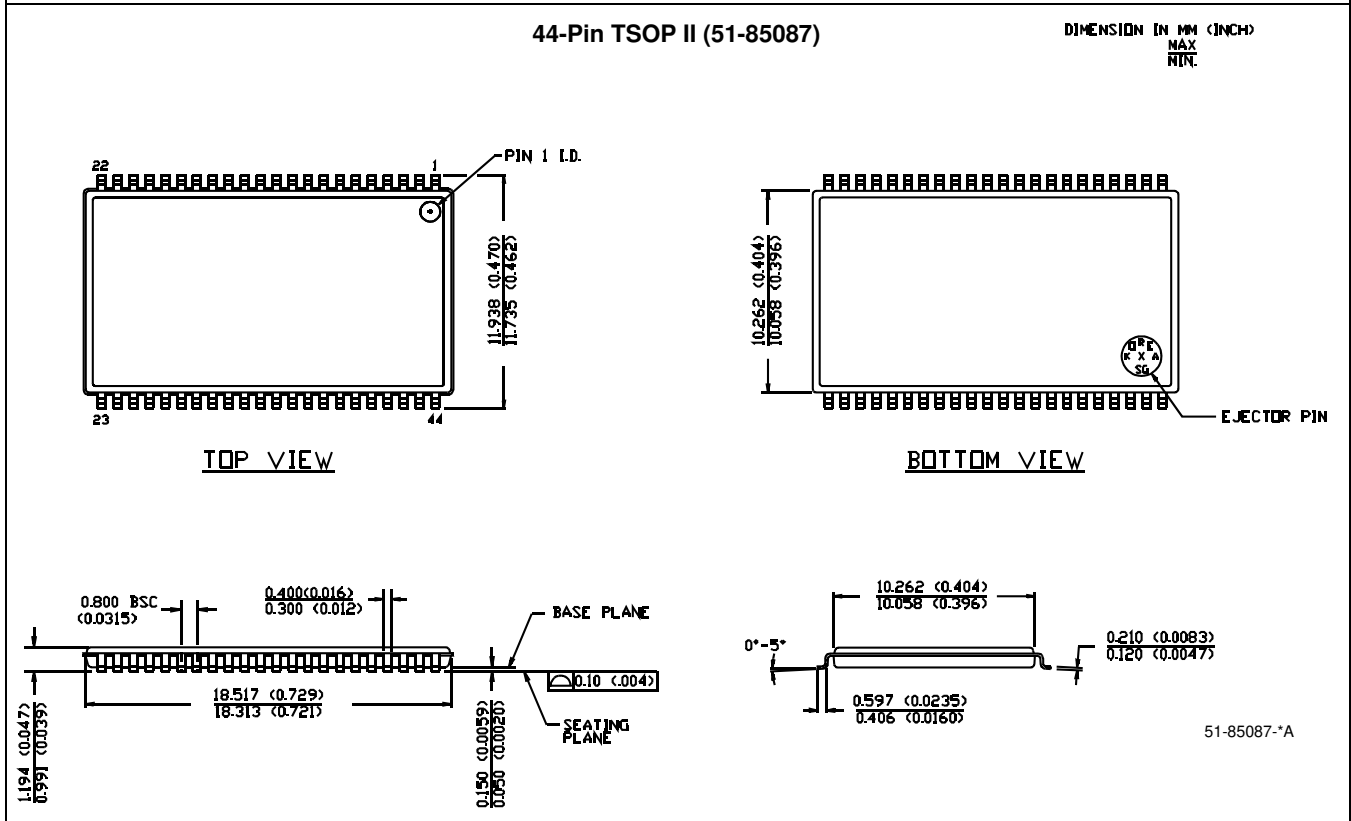
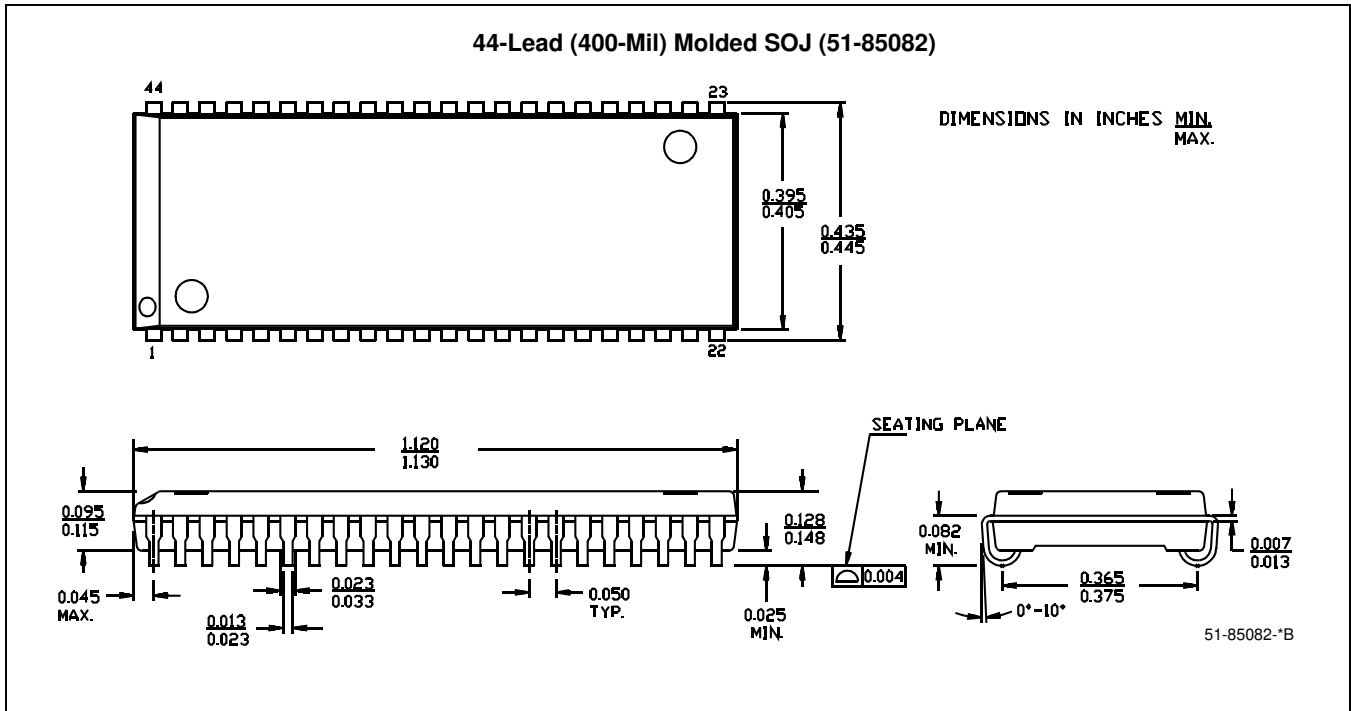
\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1041BNV33-12VXC	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	Commercial
	CY7C1041BNV33L-12VXC	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1041BNV33L-12VC	51-85082	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BNV33L-12ZC	51-85087	44-Pin TSOP II Z44	
	CY7C1041BNV33L-12ZXC	51-85087	44-Pin TSOP II Z44 (Pb-free)	
15	CY7C1041BNV33-15VXC	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	Commercial
	CY7C1041BNV33L-15VXC	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1041BNV33L-15ZXC	51-85087	44-Pin TSOP II Z44 (Pb-free)	
	CY7C1041BNV33-15VXI	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	Industrial

Please contact local sales representative regarding availability of these parts.

Package Diagrams



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Document History Page

Document Title: CY7C1041BNV33 256K x 16 Static RAM Document Number: 001-06434				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	423877	See ECN	NXR	New Data Sheet