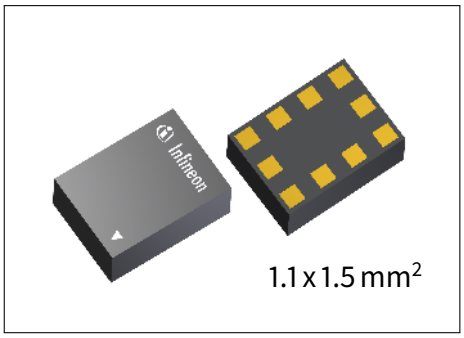
BGAU1A10

Low Noise Amplifier with Gain Control

Features

- Operating frequencies: 5.15 - 5.925 GHz
- Insertion power gain: 20.5 dB
- Gain dynamic range: 27 dB
- Low noise figure: 1.6 dB
- Low current consumption: 5.0 mA
- Multi-state control: Gain- and Bypass-Modes
- Small ATSLP leadless package



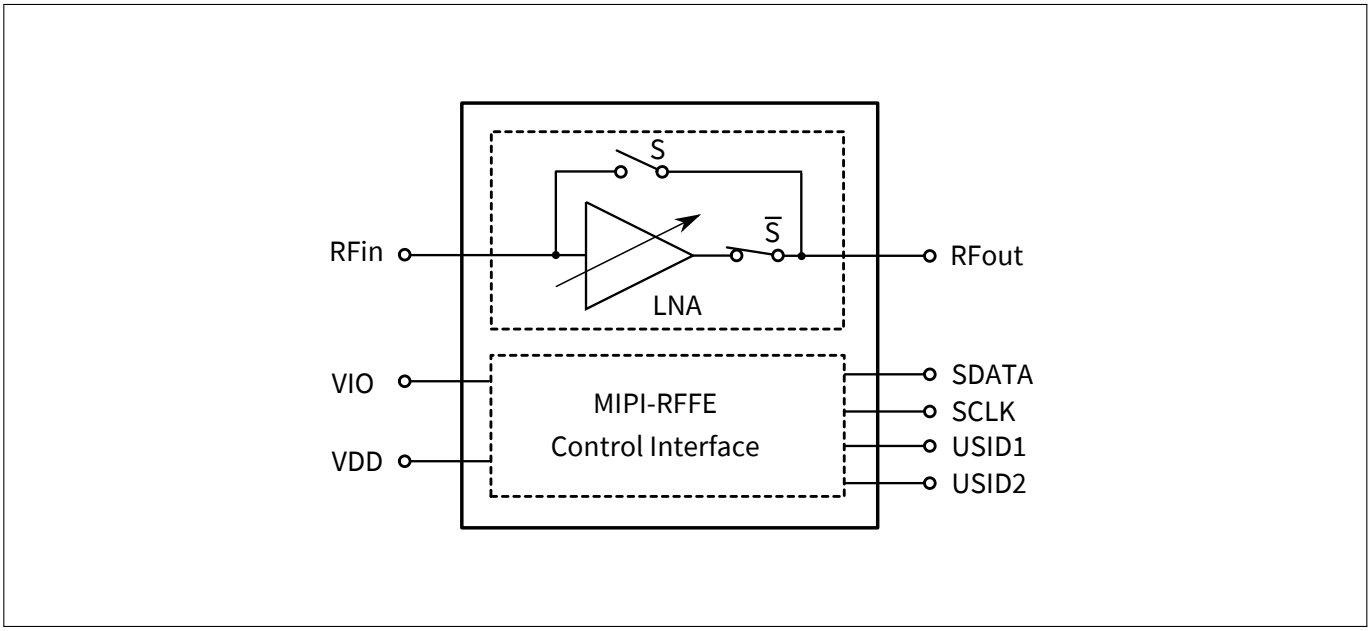
Application

The LTE data rate can be significantly improved by using the high gain LNA. The integrated gain control and bypass function increases the overall system dynamic range and leads to more flexibility in the front-end. In high gain mode the BGAU1A10 offers best Noise Figure to ensure high data rates even on the LTE cell edge. Closer to the basestation the bypass mode can be activated reducing current consumption. Thanks to the MIPI control interface, control lines are reduced to a minimum.

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



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1 Maximum Ratings

Table 1: Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage VDD	V_{DD}	-0.3	–	2.5	V	[1]
Voltage at RFin	V_{RFI}	-1	–	1	V	–
Voltage at RFout	V_{RFO}	-1	–	1	V	–
Current into pin VDD	I_{DD}	-30	–	–	mA	–
RF input power	P_{IN}	–	–	25	dBm	–
Total power dissipation	P_{tot}	–	–	90	mW	
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-30	–	85	°C	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
ESD capability, HBM	V_{ESD_HBM}	-1000	–	1000	V	[2]
RFFE Supply Voltage	V_{IO}	-0.5	–	2.7	V	–
RFFE Supply Voltage Levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO} + 0.7 (max. 2.7)	V	–

[1] All voltages refer to GND-Nodes unless otherwise noted
[2] Human Body Model ANSI/ESDA/JEDEC JS-001-2014 (R = 1.5 kΩ, C = 100 pF).

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

2 DC Characteristics

Table 3: DC Characteristics at T_A = 25 °C

Parameter [1]	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	1.7	1.8	1.9	V	–
Supply Current	I_{DD}	3.0	5.0	7.0	mA	G0-G3
		–	0.1	0.15	mA	G4
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[2]	V_{IH}	0.7 * V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[2]	V_{IL}	0	–	0.3 * V_{IO}	V	–
RFFE output high voltage[3]	V_{OH}	0.8 * V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[3]	V_{OL}	0	–	0.2 * V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	3	–	µA	Idle State

[1] Based on the application described in Chapter 5
[2] SCLK and SDATA
[3] SDATA

3 RF Characteristics

Table 4: RF Characteristics in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, I_{VDD} = 5.0 mA, f = 5.15– 5.925 GHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain f = 5500 MHz	$1/\lvert S_{21}\rvert^2$	18.5	20.5	22.5	dB	G0
		15.5	17.5	19.5	dB	G1
		7.0	9.0	11.0	dB	G2
		-2.3	-0.3	1.7	dB	G3
		-5.0	-3.0	-1.0	dB	G3 in Bias0 mode
		-8.0	-6.5	-5.0	dB	G4
Noise figure f = 5500 MHz	NF	–	1.7	2.2	dB	G0
		–	1.7	2.2	dB	G1
		–	1.6	2.1	dB	G2
		–	9.9	10.9	dB	G3
		–	6.5	8.0	dB	G4

Continued on next page

RF Characteristics

Table 4: RF Characteristics – Continued from previous page

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Return Loss[1] f = 5500 MHz	RL_{in}	4	7	–	dB	G0
		4	7	–	dB	G1
		10	20	–	dB	G2
		4	8	–	dB	G3
		6	10	–	dB	G4
Output Return Loss f = 5500 MHz	RL_{out}	10	18	–	dB	G0
		10	18	–	dB	G1
		4	7	–	dB	G2
		4	7	–	dB	G3
		7	12	–	dB	G4
Reverse Isolation f = 5500 MHz	$1/\lvert S_{12}\rvert^2$	28	33	–	dB	G0
		33	38	–	dB	G1
		24	29	–	dB	G2
		33	38	–	dB	G3
		5	6.5	–	dB	G4
Inband input 1dB-compression point f = 5500 MHz	IP_{1dB}	-22	-18	–	dBm	G0
		-21	-17	–	dBm	G1
		-10	-6	–	dBm	G2
		-1	+3	–	dBm	G3
Inband input 3rd-order intercept point[2]	$IIP3$	-13	-8	–	dBm	G0
		-13	-8	–	dBm	G1
		-7	-2	–	dBm	G2
		+1	+6	–	dBm	G3
		+25	+30	–	dBm	G4
Phase discontinuity between all Gain Mode combinations f = 5500 MHz		-12	–	12	°	Part to part variation after compensation in Base Band with constant value
Stability	k	> 1	–	–		f = 20 MHz - 10 GHz
MIPI to RF time	t_{INT}	–	1.5	2	µs	50 % last SCLK falling edge to 90 % ON, see Fig. 2
Power Up Settling Time	t_{BC}	–	10	25	µs	After power down mode

[1] For broadband matching, can be improved by using narrowband matching
[2] Input power = −30 dBm for each tone for modes G0-G3 / −15 dBm for mode G4, f_1 = 5500 MHz, $f_2 = f_1 + 1$ MHz

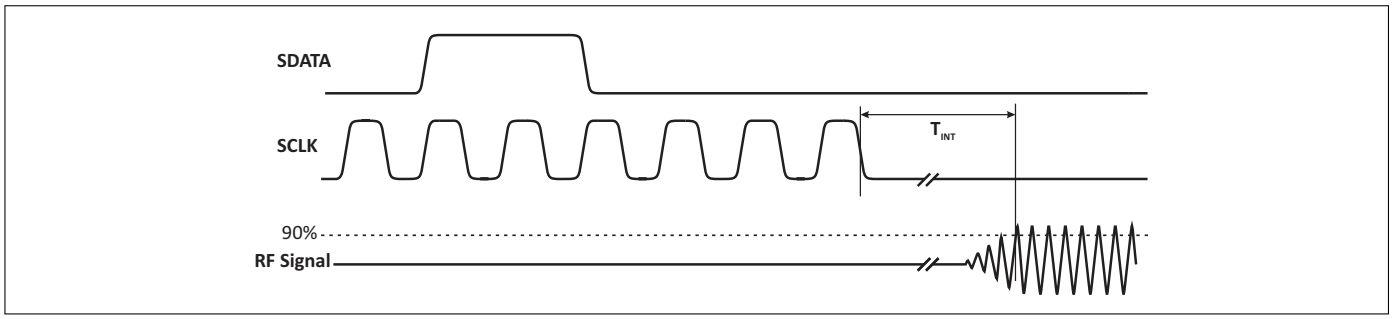

Figure 1: MIPI to RF Time

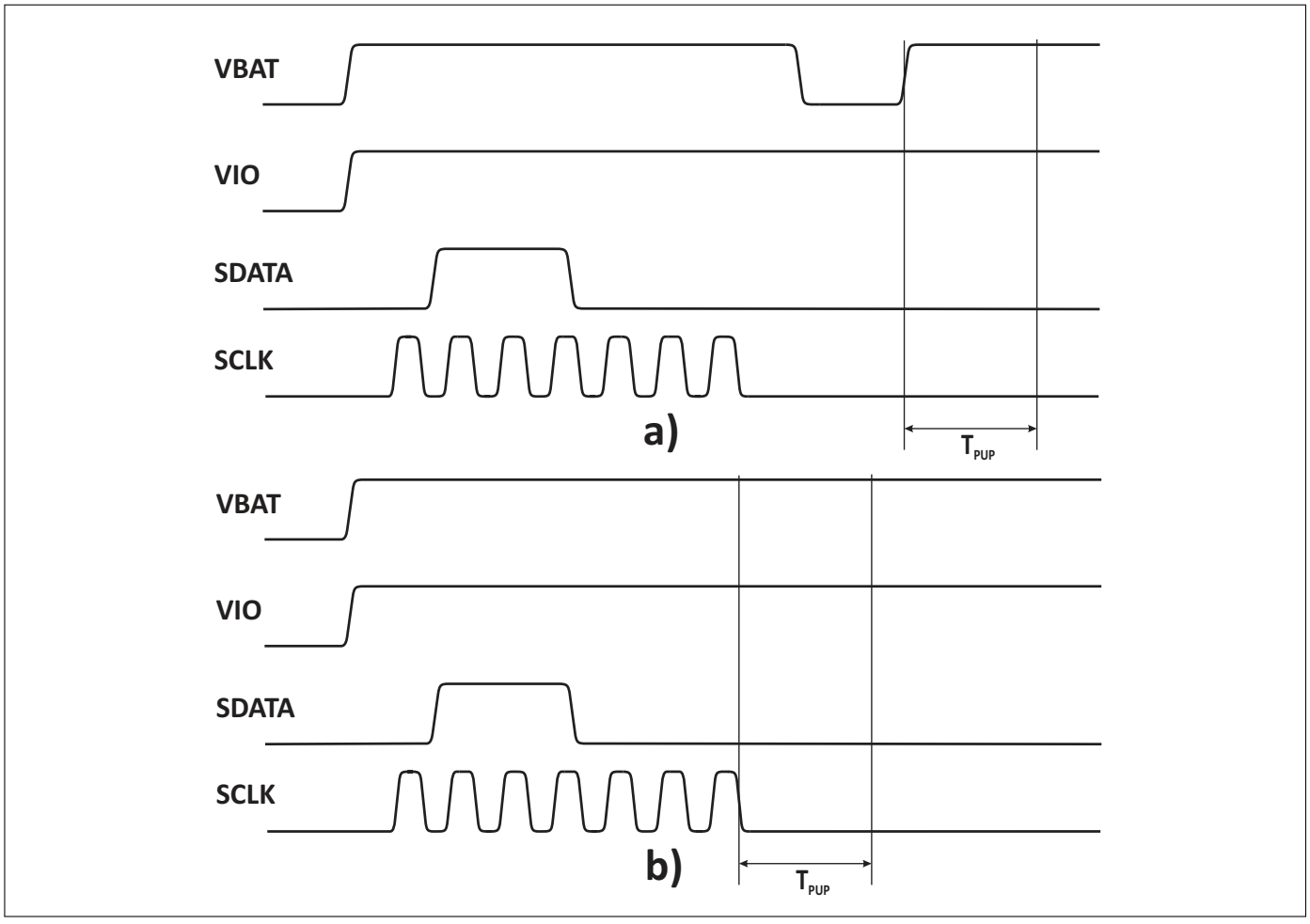

Figure 2: Power-Up Settling Time Definition: **a)** when the device is already in Active Mode. **b)** when changing from Low Power Mode to Active Mode.
After Power-Up of VIO the device is set to Low Power Mode. An additional MIPI instruction is necessary to set the device to Active Mode. This case is covered by **b)**.

4 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 2.0 - 25. September 2014.

Table 5: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.0 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID_Sel pin	Yes	External pin for changing USID: USID 12=00 → 1000, USID 12=10 → 1001, USID 12=01 → 1010, USID 12=11 → 1011
USID selection via SDATA / SCLK swap feature	No	

Table 6: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 7: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	REGISTER_0	7:0	MODE_CTRL	LNA control	00000000	No	Yes	R/W
0x1C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W
				1: Low Power Mode (LOW POWER)				
		6	PWR_MODE(0), State Bit Vector	0: No action (ACTIVE)	0			
				1: Powered Reset (STARTUP to ACTIVE to LOW POWER)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00001110	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:6	RESERVED	Reserved for future use	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 5	No	No	R/W

Table 8: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID		00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION		0001	No	No	R/W
		3:0	SUB_REVISION		0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x78	DFT	7:0	DESIGN_FOR_TEST	Do not use.	–	–	–	–

Table 9: Gain Modes of Operation (Truth Table, Register_0)

		REGISTER_0 Bits						
State	**Mode**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	Gain G0	1	0	0	1	x	x	x
2	Gain G1	1	0	1	1	x	x	x
3	Gain G2	1	1	0	1	x	x	x
4	Gain G3	1	1	1	0	x	x	x
5	Gain G4 (Bypass)	0	1	1	1	x	x	x

Table 10: Bias settings (Truth Table, Register_0)

		REGISTER_0 Bits						
State	**Mode**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
9	Bias0 (3.0 mA)	1	x	x	x	0	0	0
10	Bias1 (3.5 mA)	1	x	x	x	0	0	1
11	Bias2 (4.0 mA)	1	x	x	x	0	1	0
12	Bias3 (4.5 mA)	1	x	x	x	0	1	1
13	Bias4 (5.0 mA)[1]	1	x	x	x	1	0	0
14	Bias5 (5.5 mA)	1	x	x	x	1	0	1
15	Bias6 (6.0 mA)	1	x	x	x	1	1	0
16	Bias7 (6.5 mA)	1	x	x	x	1	1	1

[1]Target bias mode for Gain modes G0-G3

5 Application Information

Pin Configuration and Function

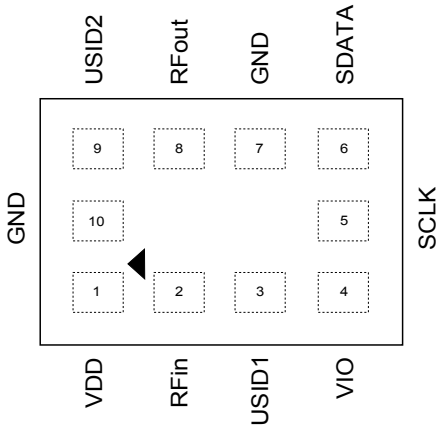

Figure 3: BGAU1A10 Pin Configuration (top view)

Table 11: Pin Definition and Function

Pin No.	Name	Function
1	VDD	Power supply
2	RFin	RF input port
3	USID1	USID select pin 1
4	VIO	MIPI RFFE supply
5	SCLK	MIPI RFFE clock
6	SDATA	MIPI RFFE data
7	GND	Ground
8	RFout	RF output port
9	USID2	USID select pin 2
10	GND	Ground

[1] Leave unconnected if not used (do NOT connect to GND)

Application Board Configuration

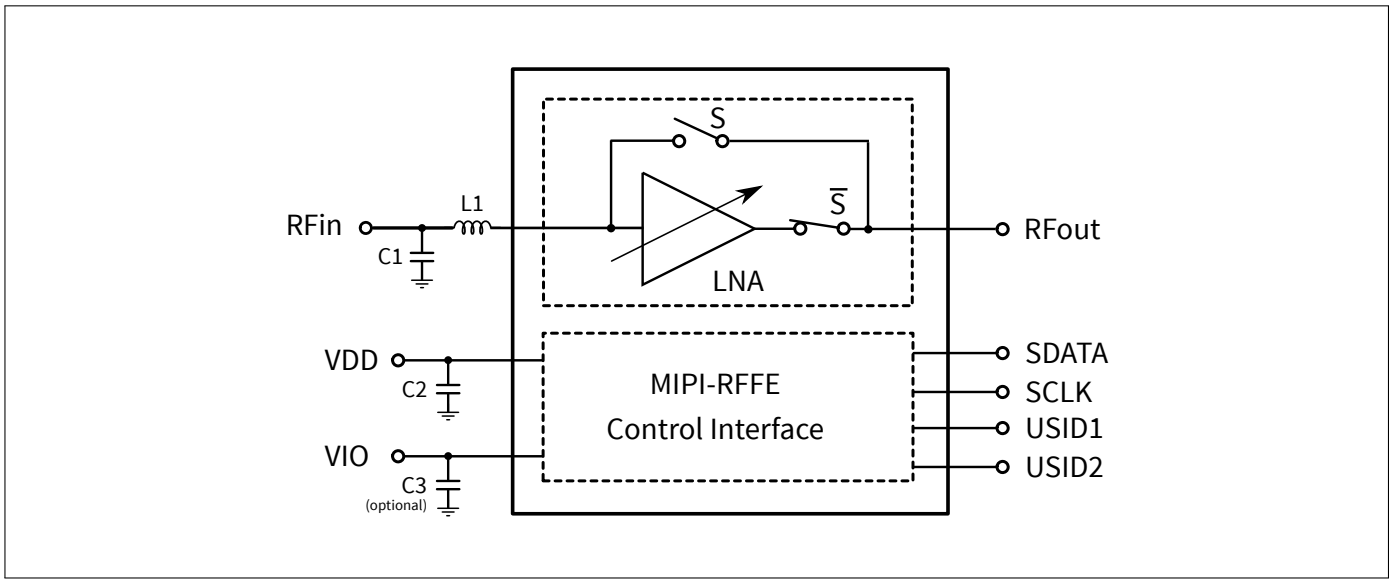

Figure 4: BGAU1A10 Application Schematic

Table 12: Bill of Materials Table

Name	Value	Package	Manufacturer	Function
C1	0.6 pF	0201	muRata GJM type	Input matching[1]
C2	10 nF	0201	Various	RF bypass[2]
C3 (optional)	10 nF	0201	Various	RF bypass[2]
L1	0.8 nH	0201	muRata LQP type	Input matching[1]
N1	BGAU1A10	ATSLP-10-3	Infineon	Variable gainstep LNA

[1]The matching elements must be optimized with reference to the frequency band of interest.
[2]RF bypass recommended to mitigate power supply noise.

6 Package Information

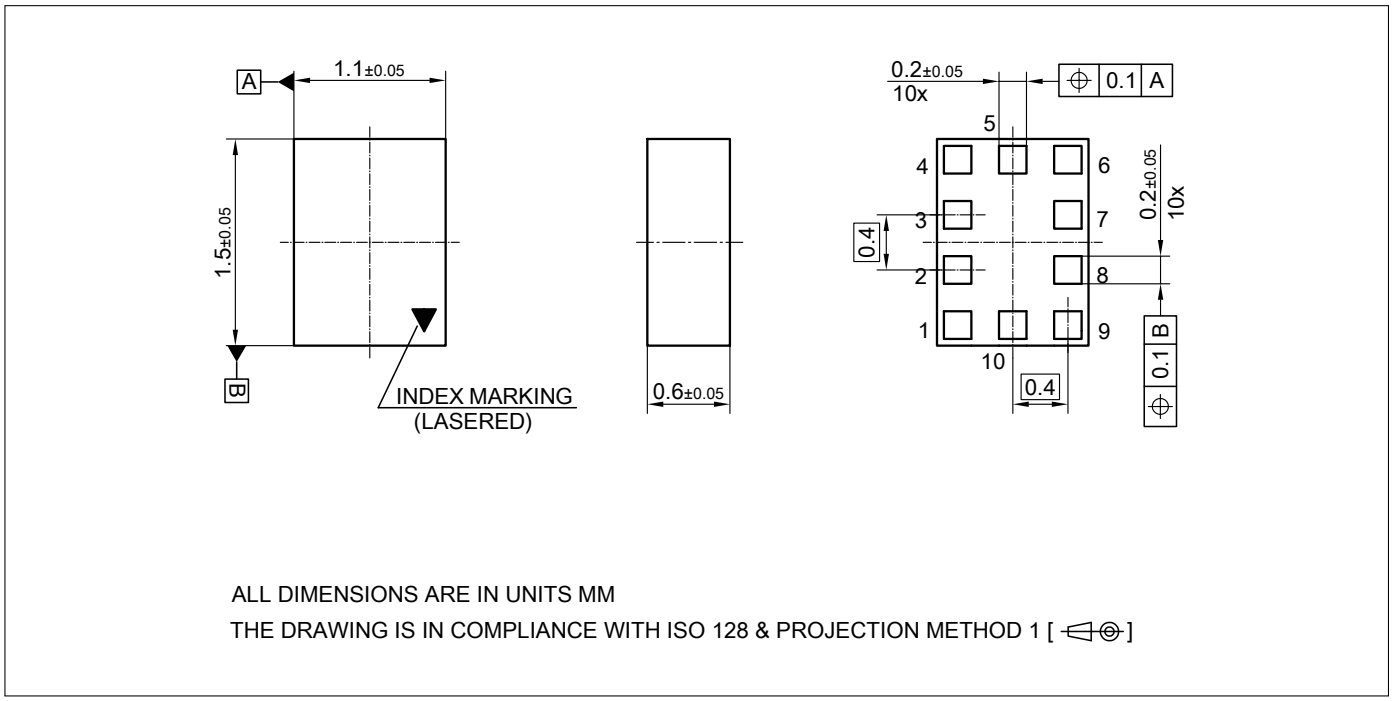

Figure 5: ATSLP-10-3 Package Outline (top, side and bottom views)

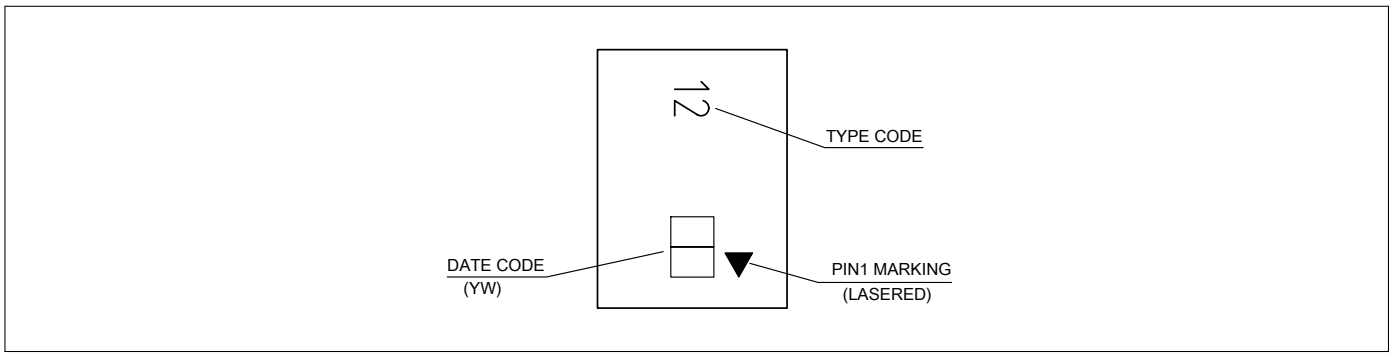

Figure 6: Marking Specification (top view)

Product Name	Marking	Package
BGAU1A10	U1	ATSLP-10-3

Table 13: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

Table 14: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

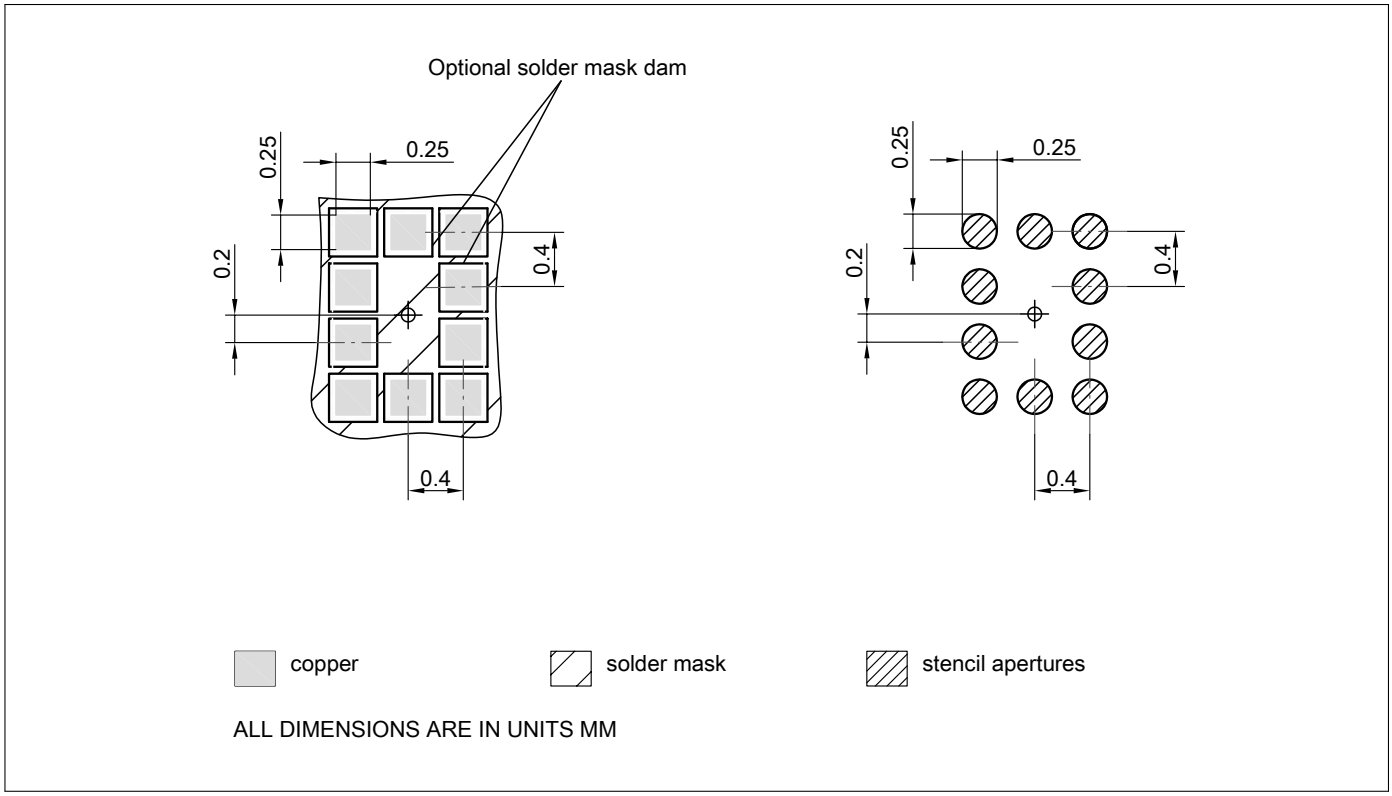

Figure 7: Footprint Recommendation

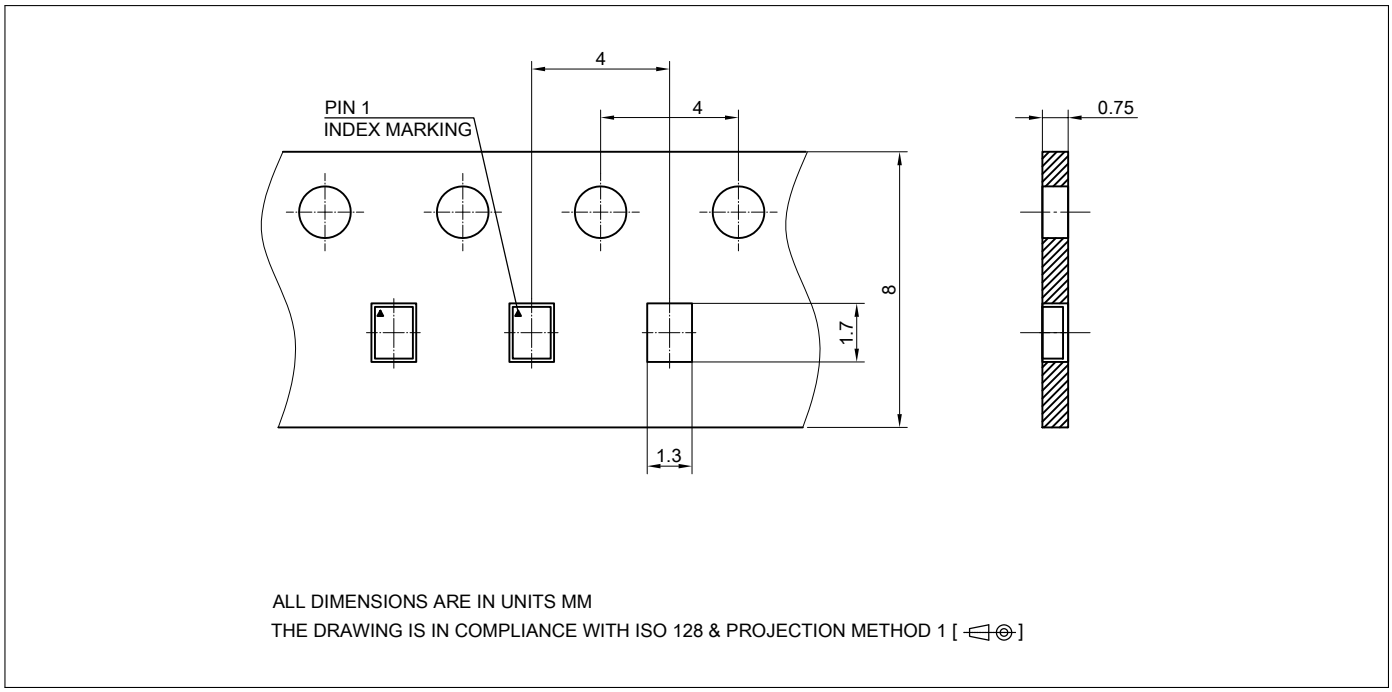

Figure 8: Carrier Tape

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 3.0, 2018-04-18	
all	"Preliminary" removed
2	Maximum current into pin VDD updated
2	Maximum RF input power updated
2	Maximum total power dissipation updated
9	Footnotes updated in Table 11 (Bias settings)
12	Package outline drawing updated
12	Marking specification drawing updated
13	Date code marking tables added
14	Footprint recommendation drawing added
14	Carrier tape drawing added
15	Trademarks updated

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