FAIRCHILD
SEMICONDUCTOR TM

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100328
Low Power Octal ECL/TTL Bi-Directional Translator with Latch

General Description

The 100328 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the 100328 transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

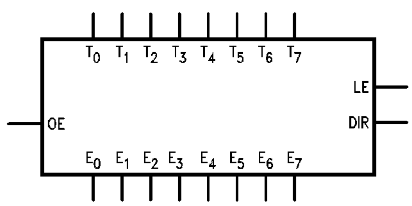
The 100328 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

Features

- Identical performance to the 100128 at 50% of the supply current
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- FAST TTL outputs
- 3-STATE outputs
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code:

Logic Symbol



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Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
LE	Latch Enable Input
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

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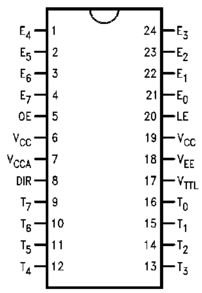
Connection Diagrams

24-Pin DIP/SOIC



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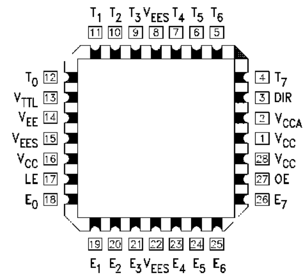
28-Pin PCC



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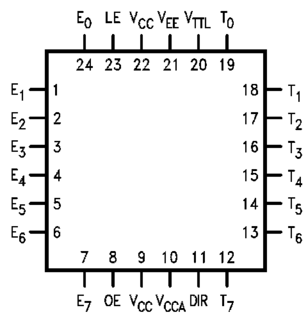
24-Pin Quad Cerpak



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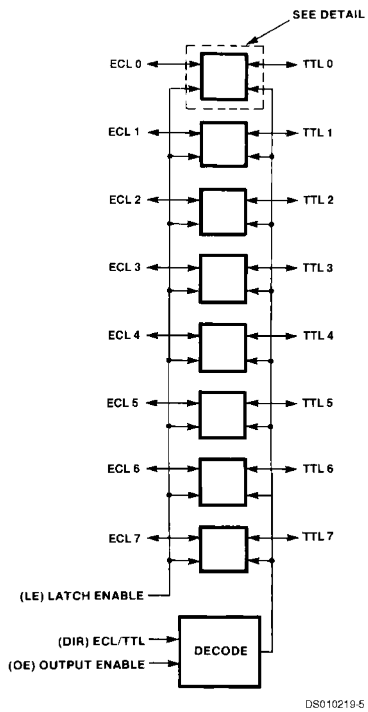
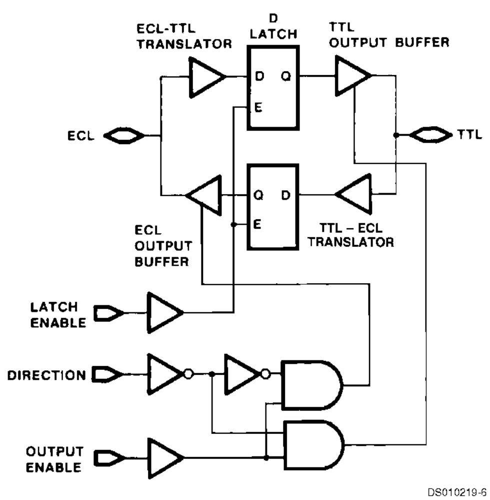
Functional Diagram



Note: LE, DIR, and OE use ECL logic levels

Detail



Truth Table

OE	DIR	LE	ECL Port	TTL Port	Notes
L	X	L	LOW (Cut-Off)	Z	
L	L	H	Input	Z	(Notes 1, 3)
L	H	H	LOW (Cut-Off)	Input	(Notes 2, 3)
H	L	L	L	L	(Notes 1, 4)
H	L	L	H	H	(Notes 1, 4)
H	L	H	X	Latched	(Notes 1, 3)
H	H	L	L	L	(Notes 2, 4)
H	H	L	H	H	(Notes 2, 4)
H	H	H	Latched	X	(Notes 2, 4)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

Absolute Maximum Ratings (Note 5)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 7)	−0.5V to +6.0V
TTL Input Current (Note 7)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State	
3-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD (Note 6)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
ECL Supply Voltage (V_{EE})	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	+4.5V to +5.5V

Note 5: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 6: ESD testing conforms to MIL-STD-883, Method 3015.

Note 7: Either voltage limit or current limit is sufficient to protect inputs.

Commercial Version TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 8)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	Loading with 50Ω to − 2V
	Cutoff Voltage		−2000	−1950	mV	OE or DIR Low, $V_{IN} = V_{IH(Max)}$ or V_{IL}(Min), Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1035			mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low			−1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			70	µA	V_{IN} = +2.7V
	Breakdown Test			1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700			µA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current					LE Low, OE and DIR High Inputs Open
		−159		−75	mA	V_{EE} = −4.2V to −4.8V
		−169		−75		V_{EE} = −4.2V to −5.7V

Note 8: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7	3.1		V	I_{OH} = −3 mA, V_{TTL} = 4.75V
		2.4	2.9		V	I_{OH} = −3 mA, V_{TTL} = 4.50V

Commercial Version
ECL-to-TTL DC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current			350	μA	V_{IN} = V_{IH} (Max)
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)
I_{OZHT}	3-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	3-STATE Current Output Low	−700			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−150		−60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current			74	mA	TTL Outputs LOW
				49	mA	TTL Outputs HIGH
				67	mA	TTL Outputs in 3-STATE

Commercial Version
DIP TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND (Note 9)

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_N to E_n (Transparent)	1.1	3.5	1.1	3.6	1.1	3.8	ns ns	*Figures 1, 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.6	1.7	3.7	1.9	3.9	ns ns	*Figures 1, 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.3	4.2	1.5	4.4	1.7	4.8	ns	*Figures 1, 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	*Figures 1, 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	*Figures 1, 2*
t_{set}	T_n to LE	1.1		1.1		1.1		ns	*Figures 1, 2*
t_{hold}	T_n to LE	1.1		1.1		1.1		ns	*Figures 1, 2*
t_{pw}(H)	Pulse Width LE	2.1		2.1		2.1		ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1, 2*

Note 9: The specified limits represent the "worst" case value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version
DIP ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.6	2.4	5.6	2.6	5.9	ns	*Figures 3, 4*

Commercial Version
DIP ECL-to-TTL AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	LE to T_n	3.1	7.2	3.1	7.2	3.3	7.7	ns	*Figures 3, 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	*Figures 3, 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	*Figures 3, 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	*Figures 3, 6*
t_{set}	E_n to LE	1.1		1.1		1.1		ns	*Figures 3, 6*
t_{hold}	E_n to LE	2.1		2.1		2.6		ns	*Figures 3, 4*
t_{pw}(H)	Pulse Width LE	4.1		4.1		4.1		ns	*Figures 3, 7*

Commercial Version
SOIC, PCC and Cerpak TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.1	3.3	1.1	3.4	1.1	3.6	ns ns	*Figures 1, 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns ns	*Figures 1, 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.3	4.0	1.5	4.2	1.7	4.6	ns	*Figures 1, 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	*Figures 1, 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	*Figures 1, 2*
t_{set}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1, 2*
t_{hold}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1, 2*
t_{pw}(H)	Pulse Width LE	2.0		2.0		2.0		ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1, 2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 10)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 10)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		650		650		650	ps	PCC Only (Note 10)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		650		650		650	ps	PCC Only (Note 10)

Commercial Version
SOIC, PCC and Cerpak TTL-to-ECL AC Electrical Characteristics (Continued)

Note 10: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Commercial Version
SOIC, PCC and Cerpak ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.4	2.4	5.4	2.6	5.7	ns	*Figures 3, 4*
t_{PLH} t_{PHL}	LE to T_n	3.1	7.0	3.1	7.0	3.3	7.5	ns	*Figures 3, 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	*Figures 3, 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	*Figures 3, 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	*Figures 3, 6*
t_{set}	E_n to LE	1.0		1.0		1.0		ns	*Figures 3, 4*
t_{hold}	E_n to LE	2.0		2.0		2.5		ns	*Figures 3, 4*
t_{pw}(H)	Pulse Width LE	4.0		4.0		4.0		ns	*Figures 3, 4*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		600		600		600	ps	PCC Only (Note 11)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		850		850		850	ps	PCC Only (Note 11)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		1350		1350		1350	ps	PCC Only (Note 11)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		950		950		950	ps	PCC Only (Note 11)

Note 11: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Industrial Version
PCC TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 12)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	Loading with 50Ω to −2V
	Cutoff Voltage		−1900		−1950	mV	OE or DIR Low, V_{IN}= $V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2V

Industrial Version
PCC TTL-to-ECL DC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 12)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OHC}	Output HIGH Voltage Corner Point High	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low		−1565		−1610	mV	
V_{IH}	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0	0.8	0	0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current		70		70	μA	V_{IN} = +2.7V
	Breakdown Test		1.0		1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700		−700		μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2		−1.2		V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current						LE Low, OE and DIR High Inputs Open
		−159	−70	−159	−75	mA	V_{EE} = −4.2V to −4.8V
		−169	−70	−169	−75		V_{EE} = −4.2V to −5.7V

Industrial Version
PCC ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note 12)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.7		2.7		V	I_{OH} = −3 mA, V_{TTL} = 4.75V
		2.4		2.4		V	I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.5		0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current		425		350	μA	V_{IN} = V_{IH} (Max)
I_{IH}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IH} (Min)
I_{OZHT}	3-STATE Current Output High		70		70	μA	V_{OUT} = +2.7V
I_{OZLT}	3-STATE Current Output Low	−700		−700		μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−150	−60	−150	−60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current		74		74	mA	TTL Outputs LOW
			49		49	mA	TTL Outputs HIGH
			67		67	mA	TTL Outputs in 3-STATE

Note 12: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version
PCC TTL-to-ECL AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = –40°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.0	3.3	1.1	3.4	1.1	3.6	ns ns	*Figures 1, 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns ns	*Figures 1, 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.2	4.0	1.5	4.2	1.7	4.6	ns	*Figures 1, 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.5	1.6	4.3	1.6	4.4	ns	*Figures 1, 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	*Figures 1, 2*
t_{set}	T_n to LE	2.5		1.0		1.0		ns	*Figures 1, 2*
t_{hold}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1, 2*
t_{pw}(H)	Pulse Width LE	2.5		2.0		2.0		ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.6	1.6	0.6	1.6	ns	*Figures 1, 2*

Industrial Version
PCC ECL-to-TTL AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.4	2.4	5.4	2.6	5.7	ns	*Figures 3, 4*
t_{PLH} t_{PHL}	LE to T_n	3.1	7.4	3.1	7.0	3.3	7.5	ns	*Figures 3, 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.7	8.3 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	*Figures 3, 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	9.0 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	*Figures 3, 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.0 7.3	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	*Figures 3, 5*
t_{set}	E_n to LE	2.5		1.0		1.0		ns	*Figures 3, 4*
t_{hold}	E_n to LE	2.3		2.0		2.5		ns	*Figures 3, 4*
t_{pw}(H)	Pulse Width LE	4.0		4.0		4.0		ns	*Figures 3, 4*

Military Version
TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	(Notes 13, 14, 15)
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
	Cutoff Voltage		−1950	mV	0°C to +125°C	OE or DIR Low		
			−1850	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω0 to −2.0V	(Notes 13, 14, 15)
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		(Notes 13, 14, 15, 16)
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		(Notes 13, 14, 15, 16)
I_{IH}	Input HIGH Current		70	μA	−55°C to 125°C	V_{IN} = +2.7V		(Notes 13, 14, 15)
	Breakdown Test		1.0	mA	−55°C to +125°C	V_{IN} = +5.5V		
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		(Notes 13, 14, 15)
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125° C	I_{IN} = −18 mA		(Notes 13, 14, 15)
I_{EE}	V_{EE} Supply Current				−55°C to +125°C	LE Low, OE and DIR High Inputs Open		(Notes 13, 14, 15)
		−165	−65	mA		V_{EE} = −4.2V to −4.8V		
		−175	−65			V_{EE} = −4.2V to −5.7V		

Military Version
ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to + 5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	2.5		mV	0°C to +125°C	I_{OH} = −1 mA, V_{TTL} = 4.50V	(Notes 13, 14, 15)
		2.4			−55°C	I_{OH} = −3 mA, V_{TTL} = 4.50V	
V_{OL}	Output LOW Voltage		0.5	mV	−55°C +125°C	I_{OL} = 24 mA, V_{TTL} = 4.50V	
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C +125°C	Guaranteed HIGH Signal for All Inputs	(Notes 13, 14, 15, 16)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	(Notes 13, 14, 15, 16)
I_{IH}	Input HIGH Current		350	μA	0°C to	V_{EE} = −5.7V	(Notes 13, 14, 15)
			500		+125°C	V_{IN} = V_{IH} (Max)	

Military Version
ECL-to-TTL DC Electrical Characteristics (Continued)

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = –55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to + 5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
I_{IL}	Input LOW Current	0.50		µA	–55°C to +125°C	V_{EE} = –4.2V V_{IN} = V_{IL} (Min)	(Notes 13, 14, 15)
I_{OZHT}	3-STATE Current Output High		70	µA	–55°C to +125°C	V_{OUT} = +2.7V	(Notes 13, 14, 15)
I_{OZLT}	3-STATE Current Output Low	–1.0		mA	–55°C to +125°C	V_{OUT} = +0.5V	(Notes 13, 14, 15)
I_{OS}	Output Short-Circuit CURRENT	–150	–60	mA	–55°C to +125°C	V_{OUT} = 0.0V, V_{TTL} = +5.5V	(Notes 13, 14, 15)
I_{TTL}	V_{TTL} Supply Current		75 50 70	mA mA mA	–55°C to +125°C	TTL Outputs Low TTL Output High TTL Output in 3-STATE	(Notes 13, 14, 15)

Note 13: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 14: Screen tested 100% on each device at –55°C, +25°C, and +125°C, Subgroups, 1, 2 3, 7, and 8.

Note 15: Sample tested (Method 5005, Table I) on each manufactured lot at –55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 16: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version
TTL-to-ECL AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = –55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	T_N to E_n (Transparent)	0.8	3.4	1.1	3.6	0.8	3.7	ns ns	*Figures 1, 2*	(Notes 17, 18, 19)
t_{PLH} t_{PHL}	LE to E_n	1.2	3.8	1.4	3.7	1.1	3.8	ns ns	*Figures 1, 2*	
t_{PZH}	OE to E_n (Cutoff to HIGH)	0.8	3.6	1.5	4.0	2.0	5.2	ns	*Figures 1, 2*	(Notes 17, 18, 19)
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	4.6	1.6	4.2	1.6	4.3	ns	*Figures 1, 2*	
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.3	ns	*Figures 1, 2*	
t_{set}	T_n to LE	2.5		2.0		2.5		ns	*Figures 1, 2*	(Note 20)
t_{hold}	T_n to LE	2.5		2.0		2.5		ns	*Figures 1, 2*	
t_{pw}(H)	Pulse Width LE	2.5		2.0		2.5		ns	*Figures 1, 2*	(Note 20)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1, 2*	(Note 20)

Military Version
ECL-to-TTL AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = –55˚C		T_C = 25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.1	6.0	2.0	5.6	2.2	6.3	ns	*Figures 1, 2*	(Notes 17, 18, 19)
t_{PLH} t_{PHL}	LE to T_n	3.1	7.0	3.1	6.5	3.3	7.5	ns	*Figures 3, 4*	
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.2 3.6	8.0 8.0	3.7 4.0	8.0 8.5	4.0 4.3	9.2 9.6	ns	*Figures 3, 4*	(Notes 17, 18, 19)
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.5 8.0	3.3 3.4	8.0 7.5	3.5 4.1	8.4 10.0	ns	*Figures 3, 5*	
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.6 2.7	7.0 7.0	2.6 3.1	7.0 7.0	2.9 4.0	8.0 10.0	ns	*Figures 3, 6*	
t_{set}	E_n to LE	2.5		2.0		2.5		ns	*Figures 3, 4*	(Note 20)
t_{hold}	E_n to LE	3.0		2.5		3.0		ns	*Figures 3, 4*	
t_{pw}(H)	Pulse Width LE	2.5		2.0		5.0		ns	*Figures 3, 4*	(Note 20)

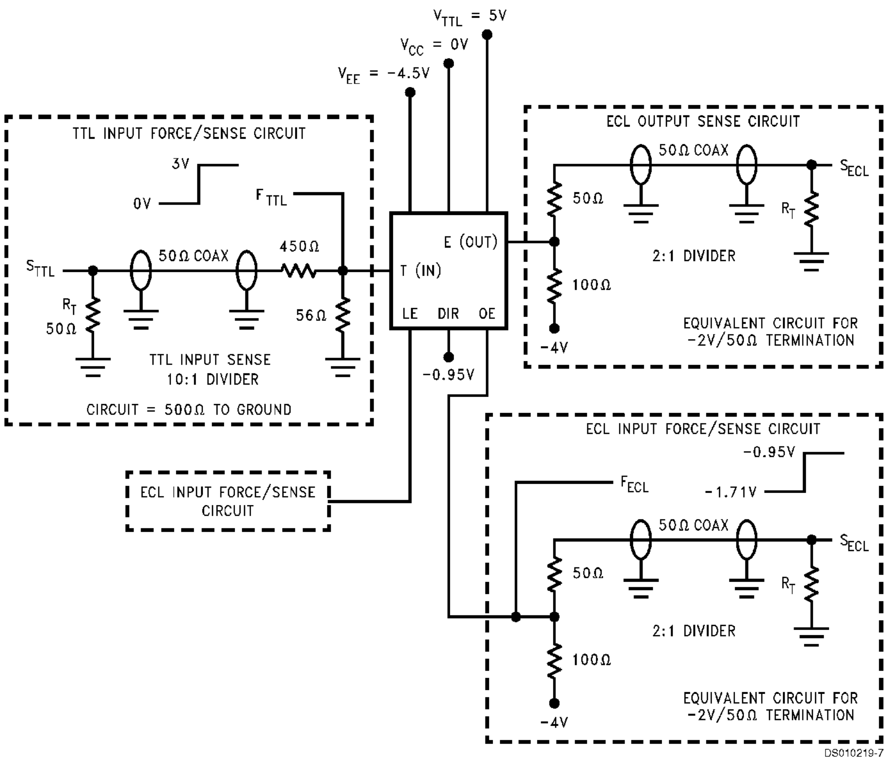
Note 17: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55˚C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 18: Screen tested 100% on each device at +25˚C, temperature only, Subgroup A9.

Note 19: Sample tested (Method 5005, Table I) on each mfg. lot at +25˚C, Subgroup A9, and at +125˚C and –55˚C temperatures, Subgroups A10 and A11.

Note 20: Not tested at +25˚C, +125˚C and –55˚C temperature (design characterization data).

Test Circuitry (TTL-to-ECL)



Note 21: R_t =50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.

Note 22: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 23: V_{TTL} is decoupled to ground with 0.1 µF to ground, V_{EE} is decoupled to ground with 0.01 µF and V_{CC} is connected to ground.

Note 24: For ECL input pins, the equivelent force/sense circuitry is optional.

FIGURE 1. TTL-to-ECL AC Test Circuit

Switching Waveforms (TTL-to-ECL)

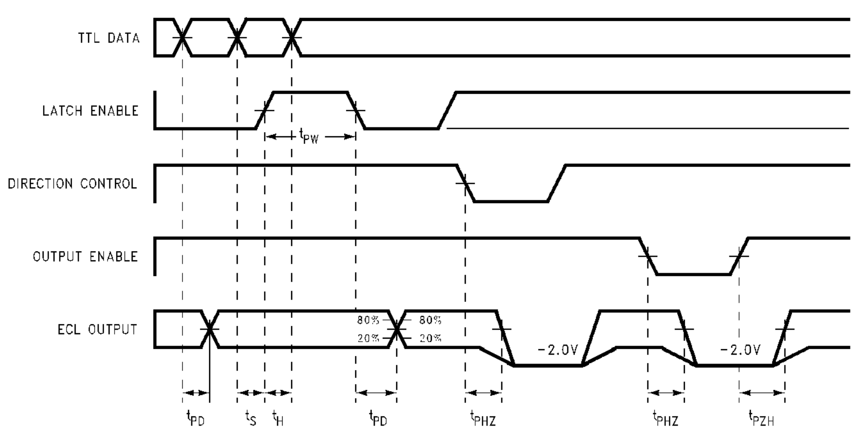
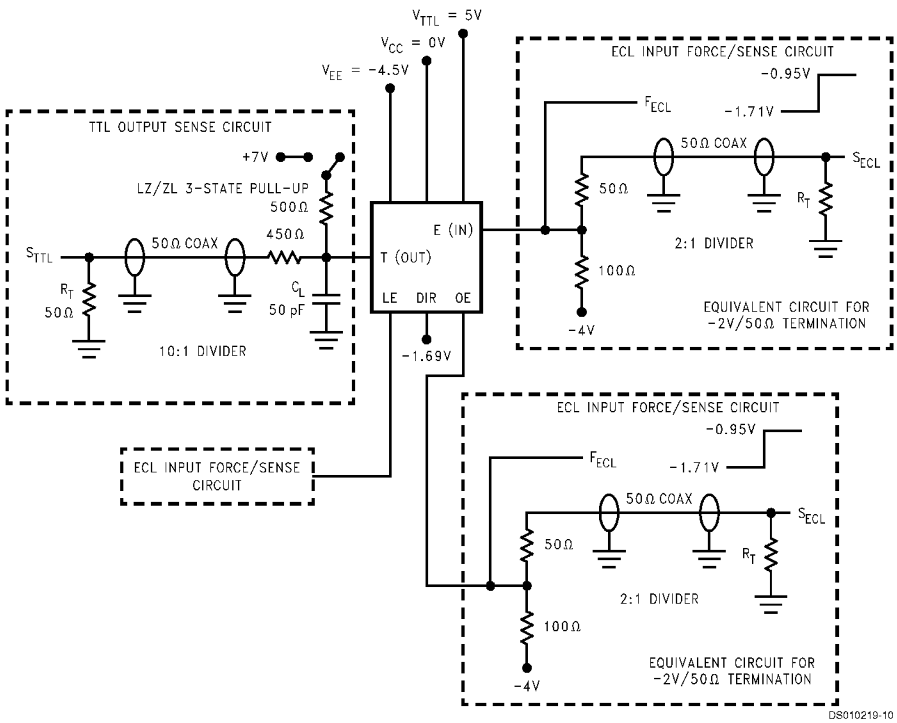


FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

Test Circuitry (ECL-to-TTL)



Note 25: R_t =50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.

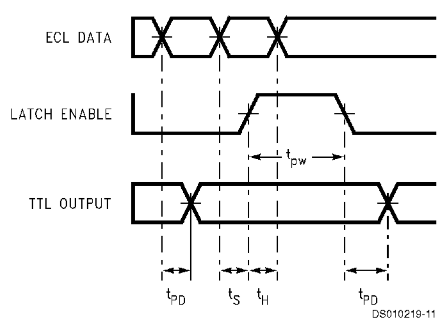
Note 26: The TTL 3-State pull up switch is connected to +7V only for ZL and LZ tests.

Note 27: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 28: V_{TTL} is decoupled to ground with 0.1 µF, V_{EE} is decoupled to ground with 0.01 µF and V_{CC} is connected to ground.

FIGURE 3. ECL-to-TTL AC Test Circuit

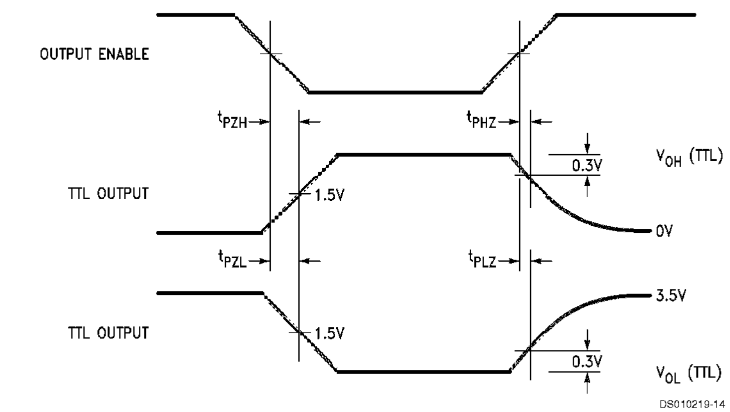
Switching Waveforms (ECL-to-TTL)



Note 29: DIR is LOW, and OE is HIGH

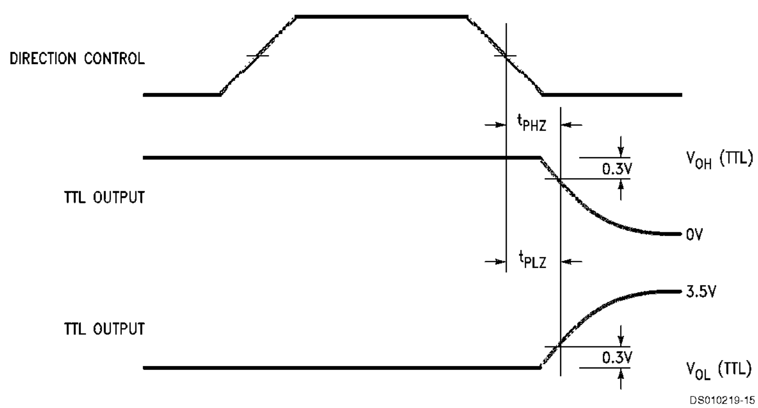
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times

Switching Waveforms (ECL-to-TTL) (Continued)



Note 30: DIR is LOW, LE is HIGH

FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times



Note 31: OE is HIGH, LE is HIGH

FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

Applications

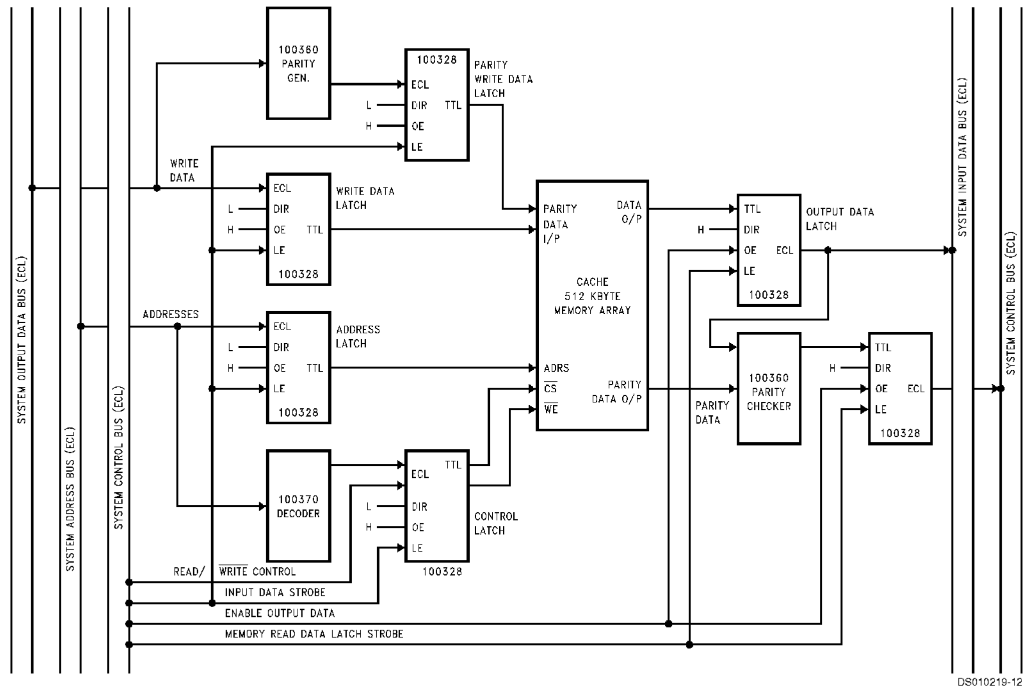


FIGURE 7. Applications Diagram—MOS/TTL SRAM Interface Using 100328 ECL–TTL Latched Translator

Ordering Information

The device number is used to form part of a simplified purchasing code where A package type and temperature range are defined as follows:

100328 D C QB

Device Type (Basic)

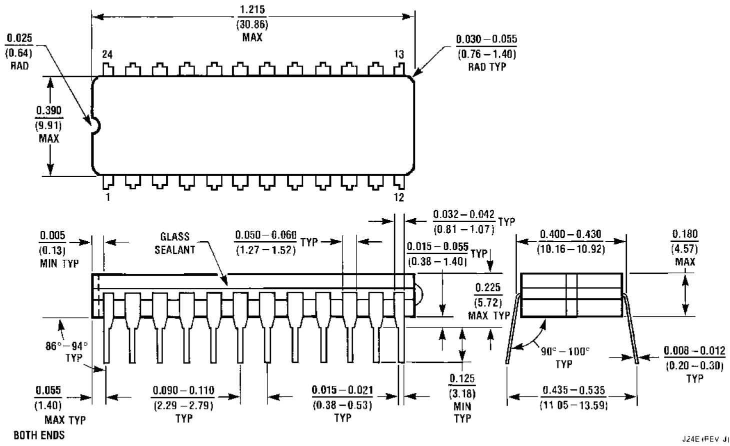
Package Code
- D = Ceramic DIP
- F = Quad Cerpak
- P = Plastic DIP
- Q = Plastic Leaded Chip Carrier (PCC)
- S = Small Outline (SOIC)

Special Variation
- QB = Military grade device with environmental and burn-in processing

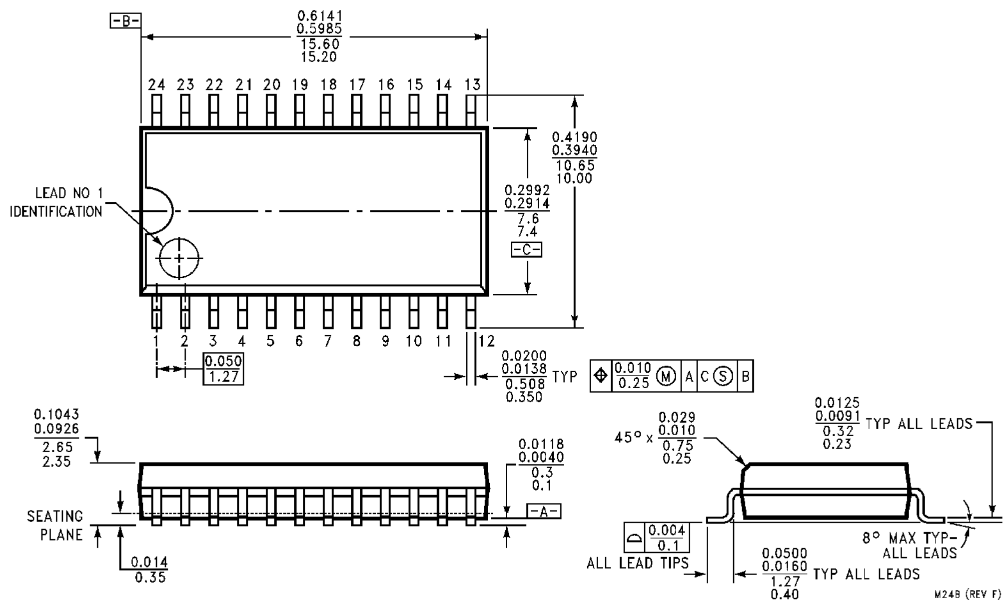
Temperature Range
- C = Commercial (0°C to +85°C)
- I = Industrial (−40°C to +85°C) (PCC Only)
- M = Military (−55°C to +125°C)

DS010219-16

Physical Dimensions inches (millimeters) unless otherwise noted

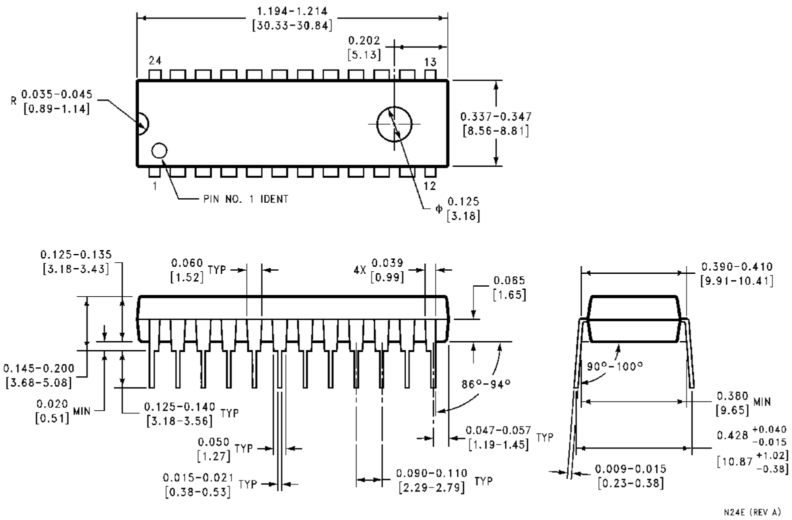


24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
Package Number J24E

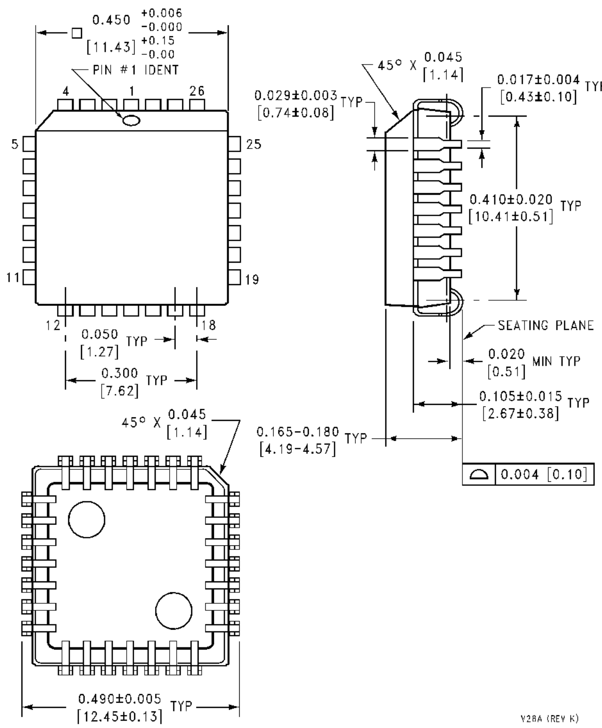


24-Lead Molded Package (0.300" Wide) (S)
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

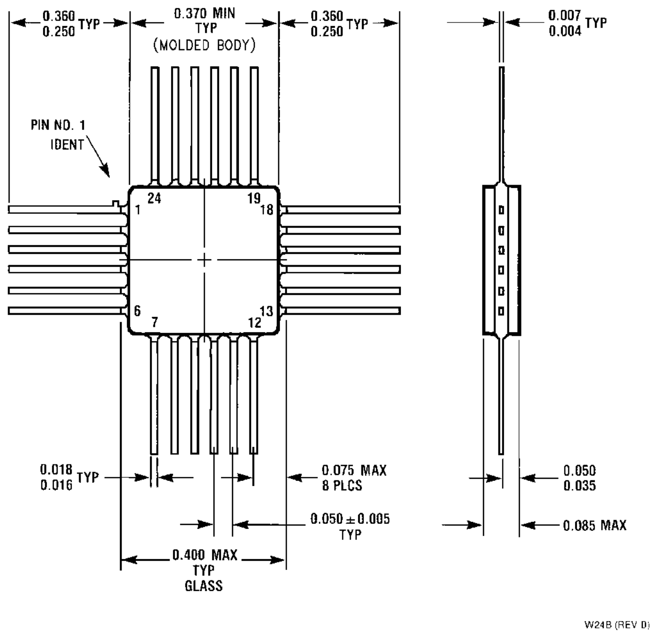


24-Lead Plastic Dual-In-Line Package (P)
Package Number N24E



28-Lead Plastic Chip Carrier (V)
Package Number V28A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Quad Cerpak (F)
Package Number W24B

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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