User's Guide

Universal Digital Isolator Evaluation Module

ABSTRACT

This user's guide describes the universal digital isolator evaluation module (EVM). This EVM lets designers evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the TI single-channel, dual-channel, triple-channel, quad-channel, or six-channels digital isolator devices in various packages: 8-pin SOIC (D), 8-pin WB SOIC (DWV), 16-pin QSOP (DBQ), 16-pin WB SOIC (DW), and 16-pin ultra WB SOIC (DWW).

CAUTION

This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the 0-V to 5.5-V recommended operating range.

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1 Introduction

This user's guide describes EVM operation with respect to most digital isolator devices that come in standard pin-compatible packages. The EVM can be used for evaluation of any of TI single-channel, dual-channel, triple-channel, quad-channel, or six-channels digital isolator devices in various packages: 8-pin SOIC (D), 8-pin WB SOIC (DWV), 16-pin QSOP (DBQ), 16-pin WB SOIC (DW), and 16-pin ultra WB SOIC (DWW). This guide also describes the standard pin configurations of devices for each package, bill of materials, EVM schematic, PCB layout, and typical laboratory test setup. A typical input and output waveform is also presented.

2 Pin Configurations of Digital Isolators in Different Packages

The DIGI-ISO-EVM has provision for multiple device footprints that are unoccupied to allow for testing of various digital isolator devices from various isolator families. Figure 2-1 through Figure 2-18 show all possible device pin configurations of digital isolators with different channel options in different packages that can be tested on this EVM. The figures also provide reference to device footprint designators (like U1) of the EVM where a given digital isolator for a given channel option in a given package can be tested on the EVM. Table 2-1 can be used as a quick reference table to identify the device footprint designator where a digital isolator can be tested for a given channel and package options.

Table 2-1. Digital Isolator Channel and Package Options and Their Respective Footprint Locations

Number of Channels	Digital Isolator Part Numbers That can be Tested	Example Part Number	Package	Location Where it can be Tested
1	ISOxx10	ISO7710	D-8	U2
			DWV-8	U1
			DW-16	U3
		ISO7810	DWW-16	U5
2	ISOxx2x	ISO7721	D-8	U2
			DWV-8	U1
			DW-16	U3
		ISO7821	DWW-16	U5
3	ISOxx3x	ISO7731	DBQ-16	U6
			DW-16	U4
		ISO7831	DWW-16	U5
4	ISOxx4x	ISO7741	DBQ-16	U6
			DW-16	U4
		ISO7841	DWW-16	U5
6	ISOxx6x	ISO7762	DBQ-16	U7
			DW-16	U8

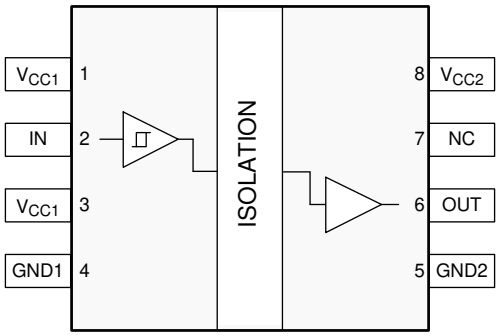

Figure 2-1. Single-Channel Digital Isolator Pin Configuration for D-8 Package on U2 and DWV-8 Package on U1

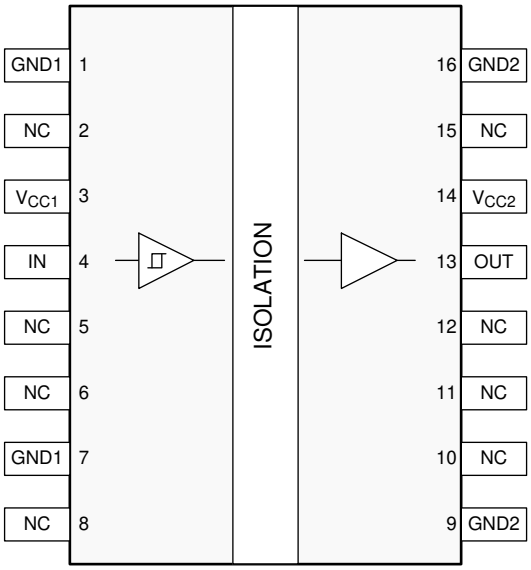

Figure 2-2. Single-Channel Digital Isolator Pin Configuration for DW-16 Package on U3

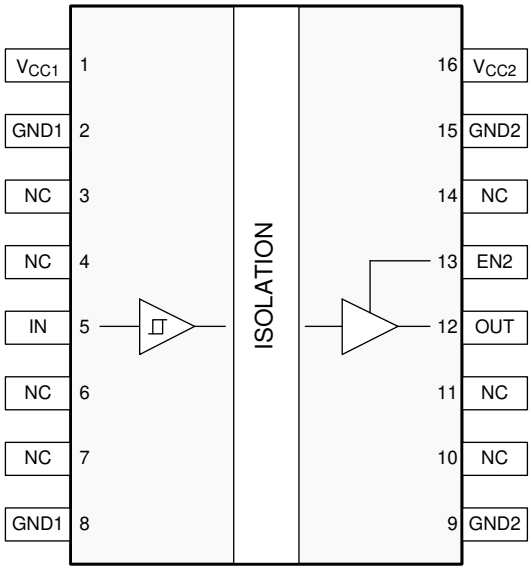

Figure 2-3. Single-Channel Digital Isolator Pin Configuration for DWW-16 Package on U5

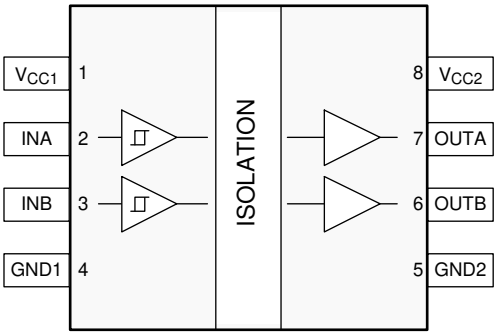

Figure 2-4. Dual-Channel (ISOxx20) Digital Isolator Pin Configurations for D-8 Package on U2 and DWV-8 Package on U1

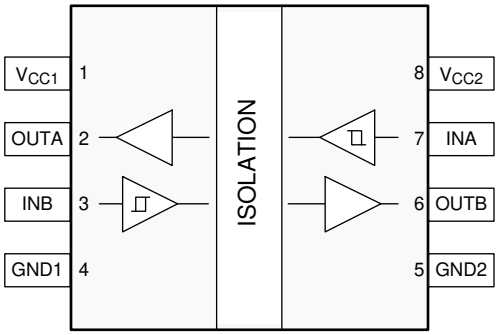

Figure 2-5. Dual-Channel (ISOxx21) Digital Isolator Pin Configurations for D-8 Package on U2 and DWV-8 Package on U1

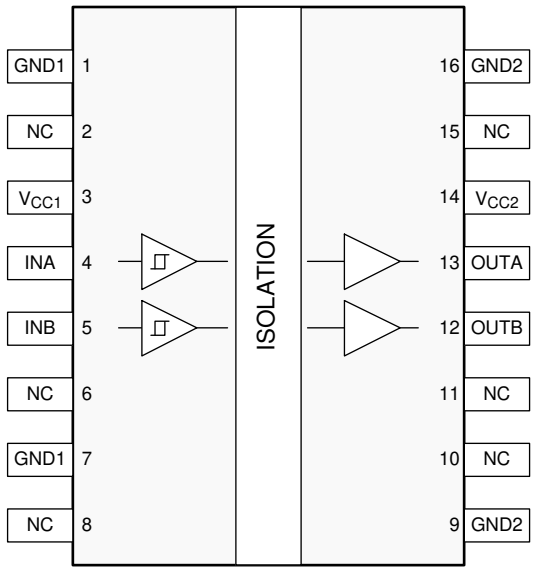

Figure 2-6. Dual-Channel (ISOxx20) Digital Isolator Pin Configurations for DW-16 Package on U3

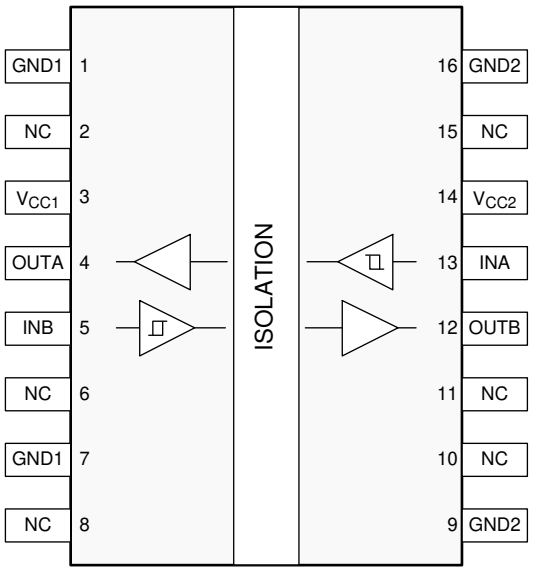

Figure 2-7. Dual-Channel (ISOxx21) Digital Isolator Pin Configurations for DW-16 Package on U3

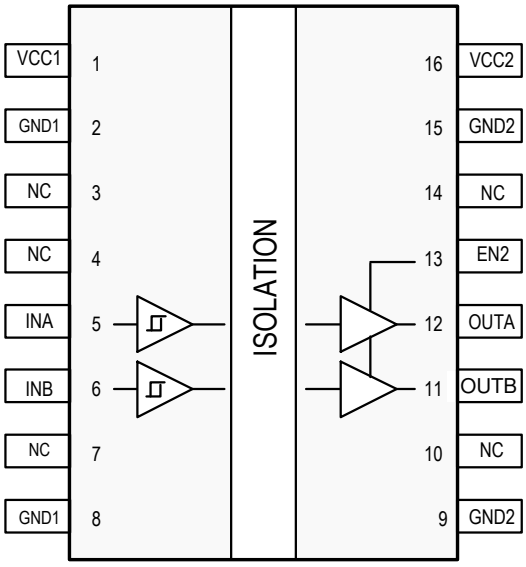

Figure 2-8. Dual-Channel (ISOxx20) Digital Isolator Pin Configurations for DWW-16 Package on U5

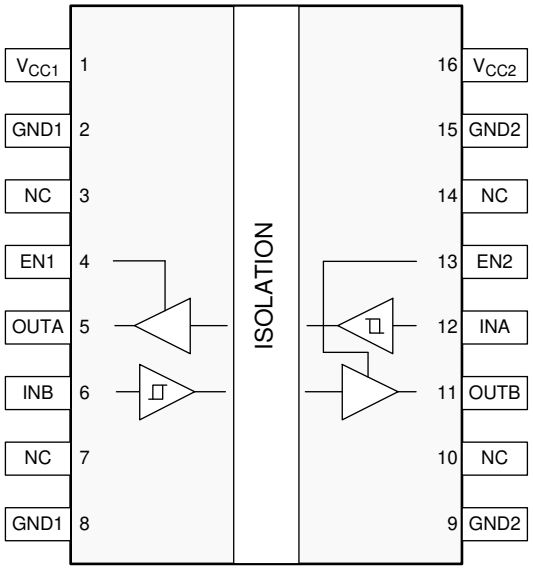

Figure 2-9. Dual-Channel (ISOxx21) Digital Isolator Pin Configurations for DWW-16 Package on U5

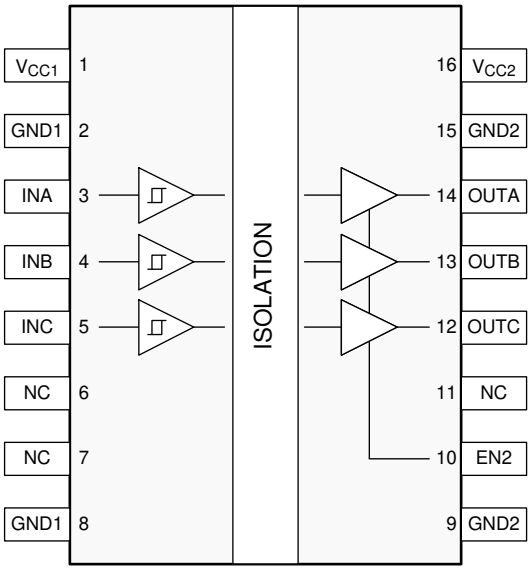

Figure 2-10. Triple-Channel (ISOxx30) Digital Isolator Pin Configurations for DBQ-16 Package on U6, DW-16 Package on U4, and DWW-16 Package on U5

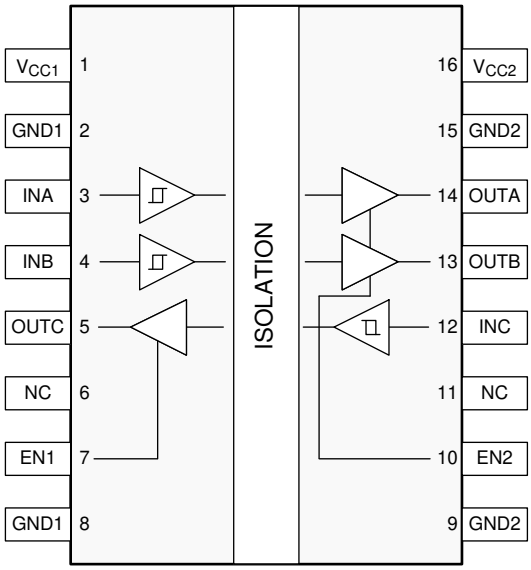

Figure 2-11. Triple-Channel (ISOxx31) Digital Isolator Pin Configurations for DBQ-16 Package on U6, DW-16 Package on U4, and DWW-16 Package on U5

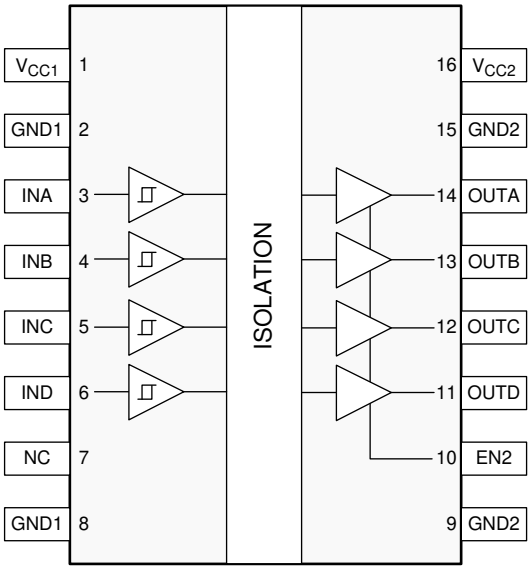

Figure 2-12. Quad-Channel (ISOxx40) Digital Isolator Pin Configurations for DBQ-16 Package on U6, DW-16 Package on U4, and DWW-16 Package on U5

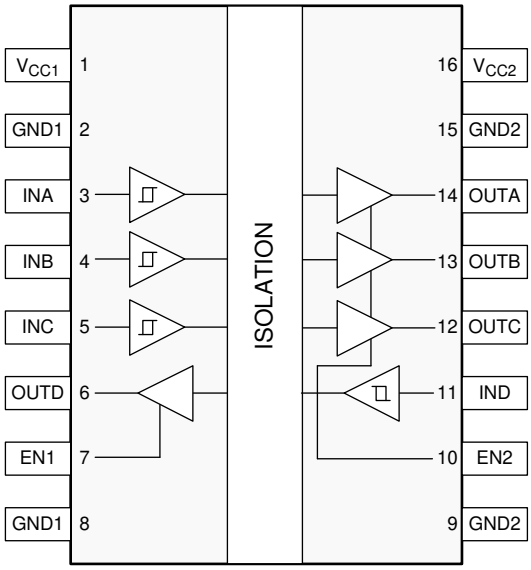

Figure 2-13. Quad-Channel (ISOxx41) Digital Isolator Pin Configurations for DBQ-16 Package on U6, DW-16 Package on U4, and DWW-16 Package on U5

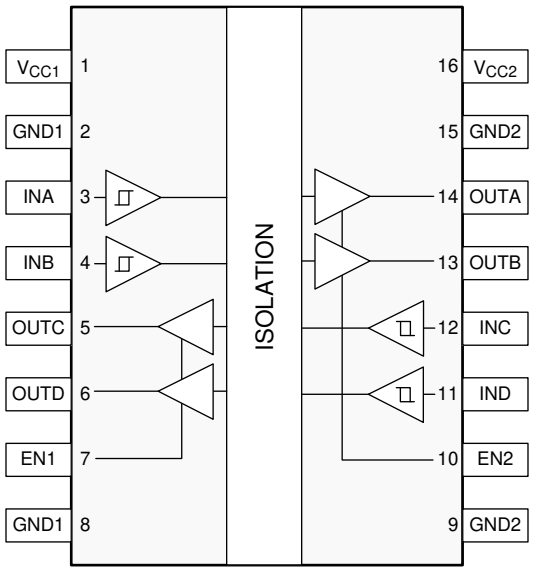

Figure 2-14. Quad-Channel (ISOxx42) Digital Isolator Pin Configurations for DBQ-16 Package on U6, DW-16 Package on U4, and DWW-16 Package on U5

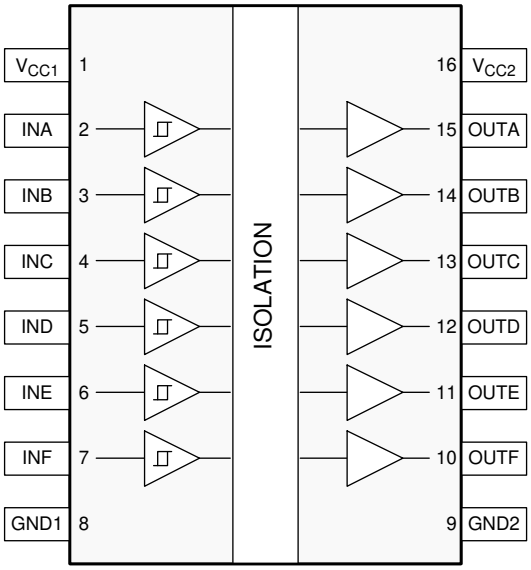

Figure 2-15. Six-Channel (ISOxx60) Digital Isolator Pin Configurations for DBQ-16 Package on U7 and DW-16 Package on U8

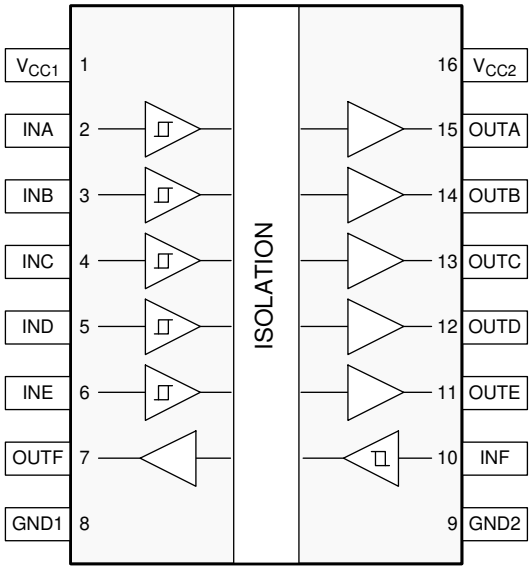

Figure 2-16. Six-Channel (ISOxx61) Digital Isolator Pin Configurations for DBQ-16 Package on U7 and DW-16 Package on U8

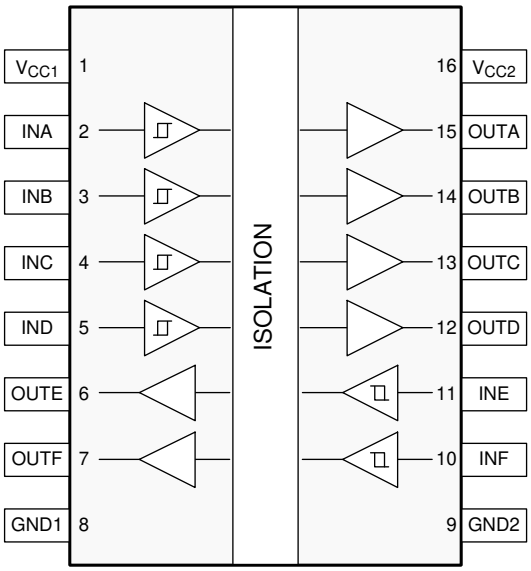

Figure 2-17. Six-Channel (ISOxx62) Digital Isolator Pin Configurations for DBQ-16 Package on U7 and DW-16 Package on U8

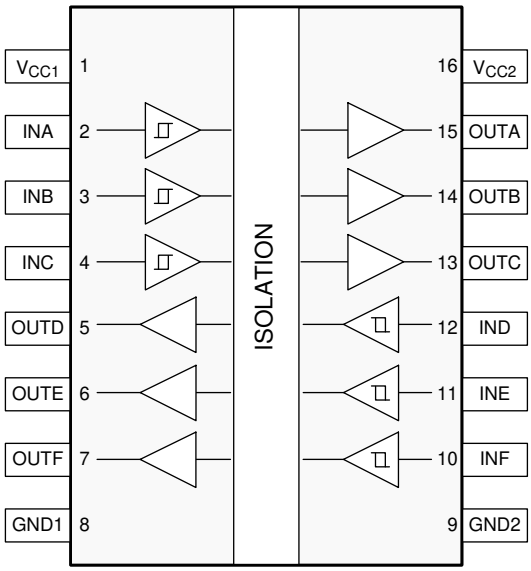

Figure 2-18. Six-Channel (ISOxx63) Digital Isolator Pin Configurations for DBQ-16 Package on U7 and DW-16 Package on U8

3 Universal Digital Isolator EVM Image

Figure 3-1 shows the 3D diagram of the EVM.

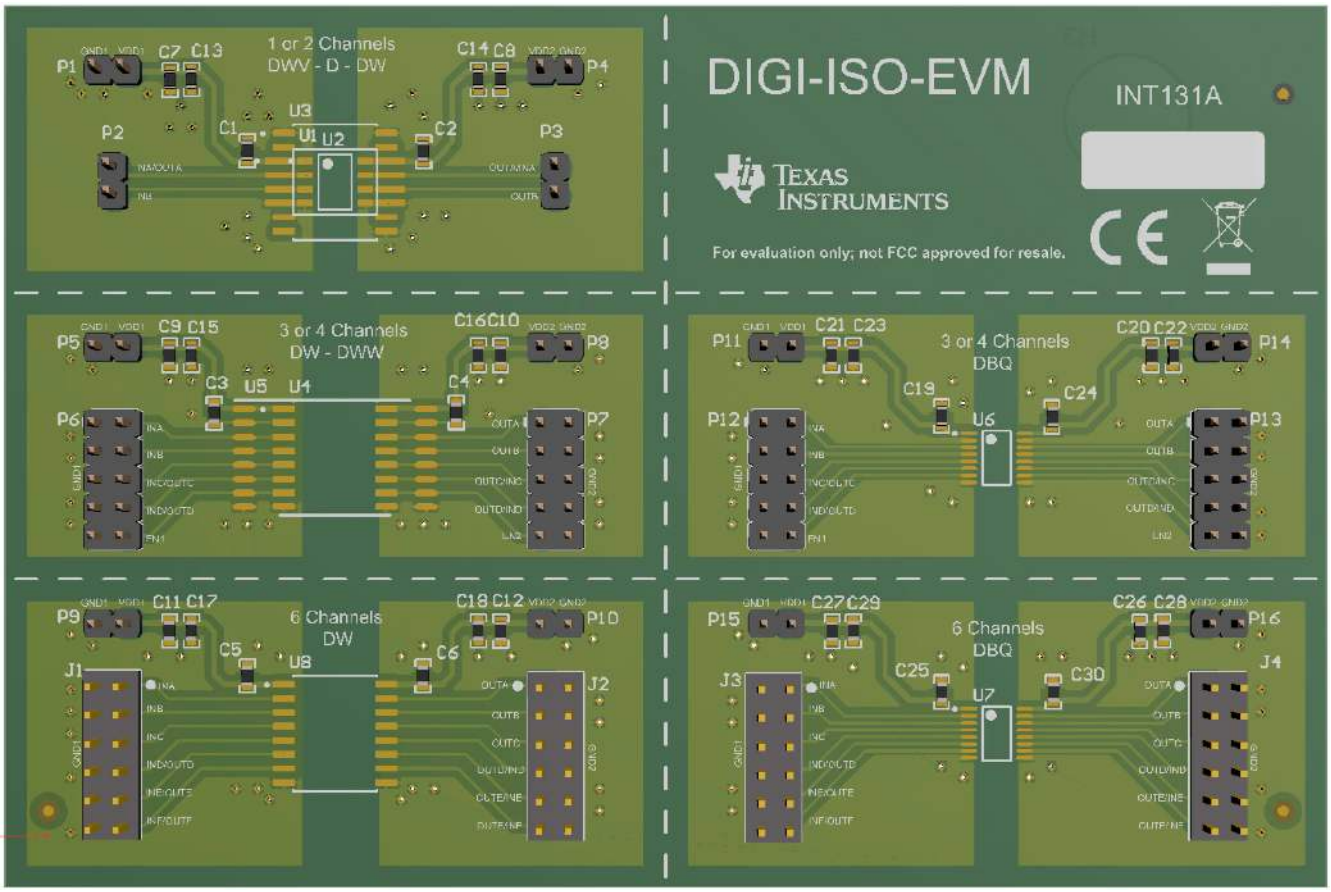

Figure 3-1. DIGI-ISO-EVM 3D Diagram

4 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 4-1 shows the configuration for operating the universal digital isolator EVM for one device footprint using two power supplies.

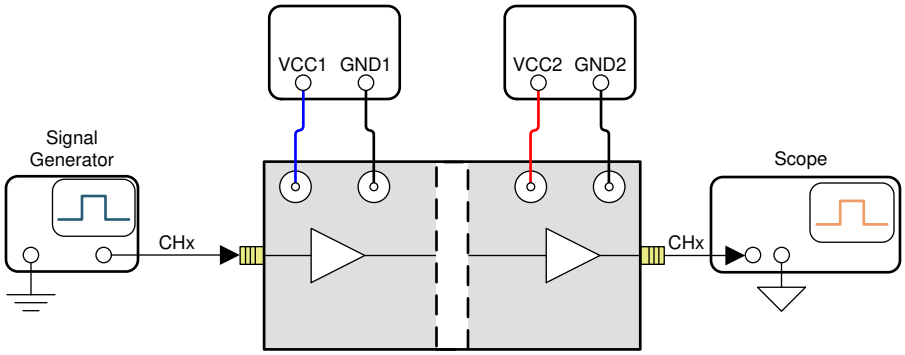

Figure 4-1. Basic EVM Operation

Figure 4-2 shows typical input and output waveforms of the EVM for a 1-MHz clock. The input is shown as channel 1, and the output is shown as channel 2.

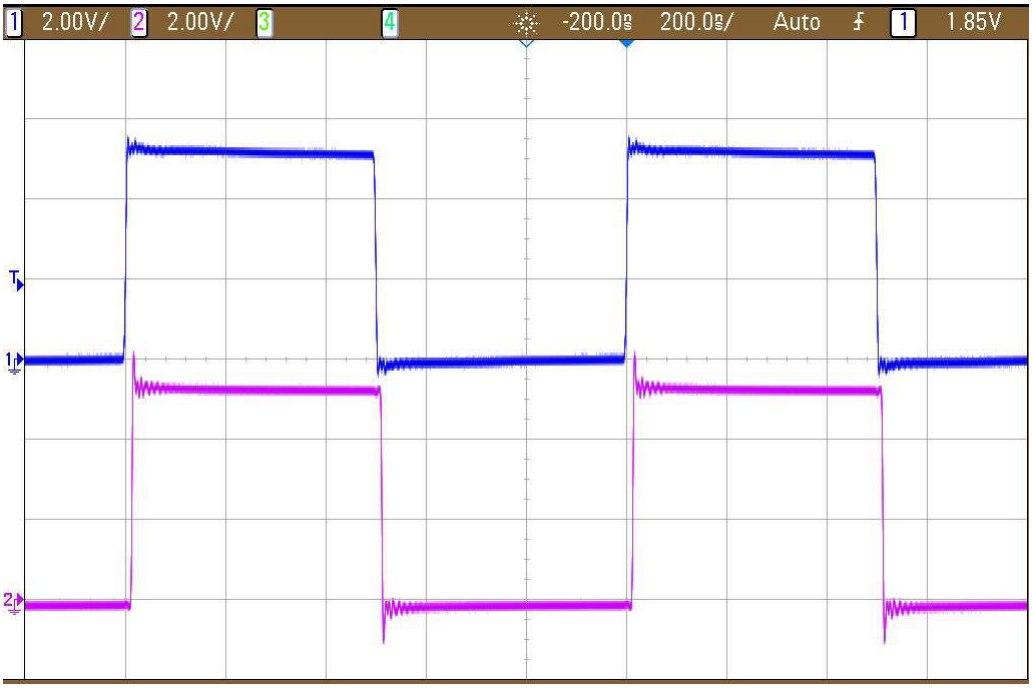

Figure 4-2. Typical Input and Output Waveform

5 Bill of Materials

Table 5-1 shows the bill of materials (BOM) for this EVM.

Table 5-1. Bill of Materials

Item	Designator	Description	Manufacturer	Part Number	Quantity
1	C1, C2, C3, C4, C5, C6, C19, C24, C25, C30	CAP, CERM, 0.1 uF, 25 V, ±5%, X7R, 0603	AVX	06033C104JAT2A	10
2	C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C20, C21, C22, C23, C26, C27, C28, C29	CAP, CERM, 1 uF, 25 V, ±10%, X5R, 0603	TDK	C1608X5R1E105K080AC	20
3	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
4	J1, J2, J3, J4	Header, 100mil, 6x2, Gold, TH	TE Connectivity	87227-6	4
5	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
6	P1, P2, P3, P4, P5, P8, P9, P10, P11, P14, P15, P16	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	12
7	P6, P7, P12, P13	Header, 2.54 mm, 5x2, Gold, TH	Wurth Elektronik	61301021121	4

6 EVM Schematic and PCB Layout

The universal digital isolator EVM is designed to accommodate various digital isolators with different channel options in different packages. To evaluate any of the digital isolator devices in a given package, populate the device of interest on the DIGI-ISO-EVM PCB according to the footprint positions suggested in section 2. No other component requires any modification on the EVM. Figure 6-1 shows the DIGI-ISO-EVM schematic and Figure 6-2 shows the printed-circuit board (PCB) layout of the EVM.

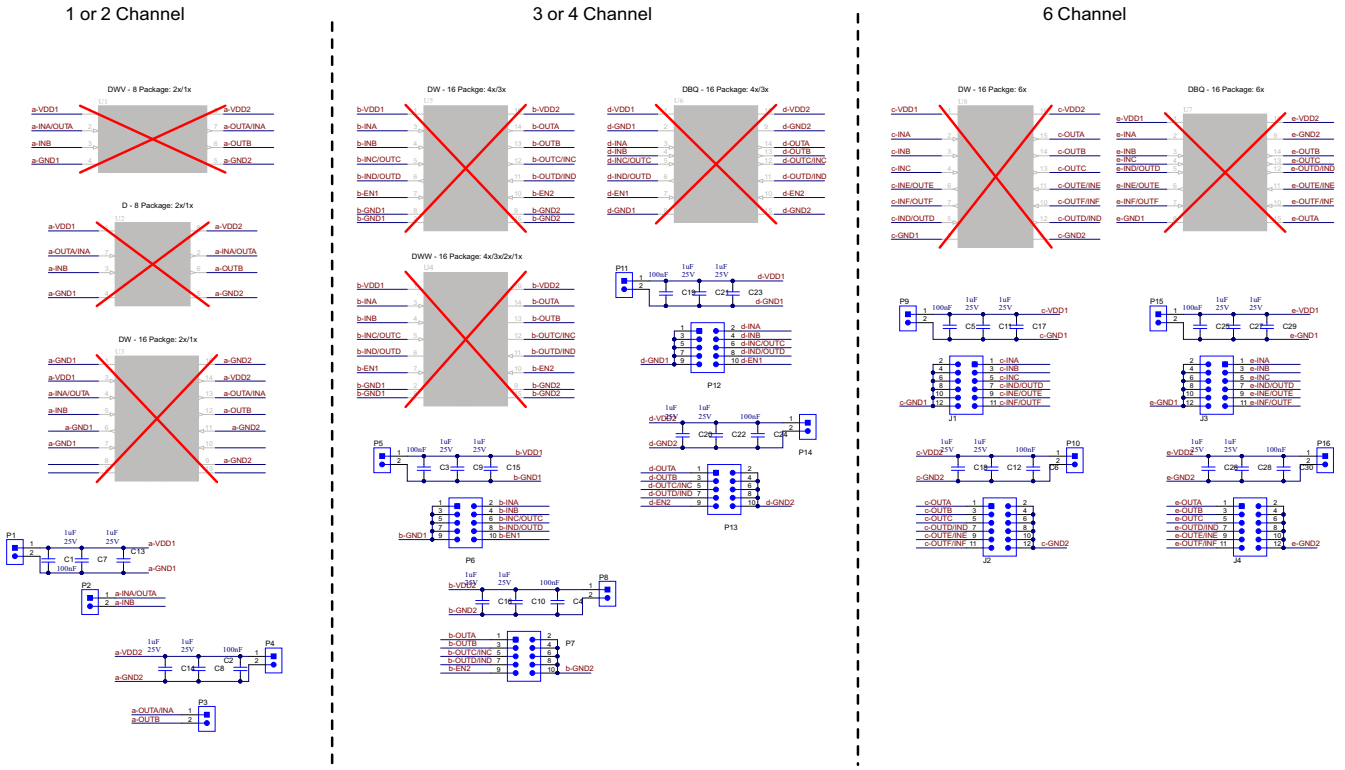

Figure 6-1. DIGI-ISO-EVM Schematic

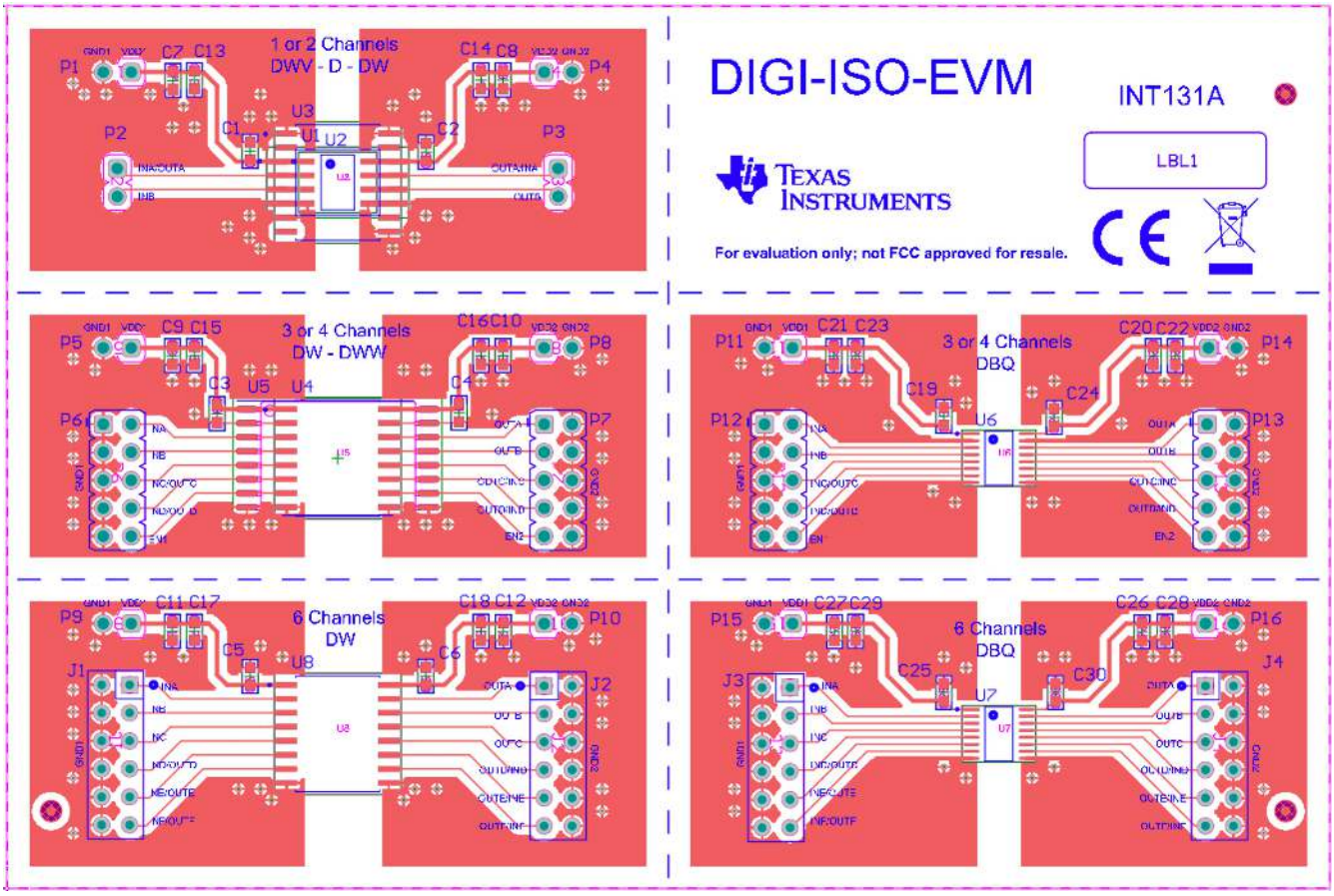

Figure 6-2. DIGI-ISO-EVM PCB Layout

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